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RESEARCH PAPER

Electrical modeling of packaged GaN HEMT dedicated to internal power matching in S-band

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The electrical modeling of power packages is a major issue for designers of high-efficiency hybrid power amplifiers. This paper reports the synthesis and the modeling of a packaged Gallium nitride (GaN) High electron mobility transistor (HEMT) associating a nonlinear model of the GaN HEMT die with an equivalent circuit model of the package. The extraction procedure is based on multi-bias S-parameter measurements of both packaged and unpackaged (on-wafer) configurations. Two different designs of 20 W packaged GaN HEMTs illustrate the modeling approach that is validated by time-domain load-pull measurements in S-band. The advantage of the electrical modeling dedicated to packaged GaN HEMTs is to enable a die-package co-design for power matching. Internal matching elements such as Metal oxide semiconductor (MOS) capacitors, Monolithic microwave integrated circuits (MMICs), and bond wires can be separately modeled to ensure an efficient optimization of the package for high power Radio frequency (RF) applications.

Keywords: Modelling, Simulation and characterizations of devices and circuits, Power Amplifiers and Linearizers

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I. INTRODUCTION

Packaging has a critical impact on high-efficiency high-power RF transistors as it greatly determines and limits the fundamental and harmonic loads of the internal transistor die. Therefore, scalability and reliability of the package modeling are essential issues that must be addressed during the design cycle of packaged GaN HEMTs.

Different modeling techniques of RF packages have already been published. Full-wave electromagnetic (EM) simulations are often used [1, 2], but they are very time consuming and not easily scalable. Other approaches consist of extracting an equivalent circuit model of the package from EM simulations [3] or S-parameter measurements of coplanar standards placed inside the package [4]. More recently, in the case of an RF package integrating a silicon LDMOS power transistor and its matching MOS capacitors, Aaen *et al.* [5, 6] proposed a modeling technique based on a combination of EM simulations with equivalent circuit extractions for the segmentation of the complex packaging environment into its constituent components. A complete insight into the topics of nonlinear transistor modeling, parameter extraction techniques, and package effects can be found in [7, 8]. In this paper, we propose a modeling method of packaged GaN HEMTs in S-band associating a nonlinear model of the GaN HEMT die with a lumped-element circuit model of the package. Despite the simplifying assumptions of lumped-element models compared with all possible EM interactions at high frequencies, the modeling time can be dramatically reduced thereby allowing the designers to optimize the package configuration since each of its physical constituents is linked to a lumped-element circuit. Our aim is to enable a rapid Computer aided design (CAD) synthesis of the optimum package for internally matched GaN HEMTs in S-band that can be compatible with the required nonlinear simulations to optimize power and efficiency performances.

Section II describes the modeling method and illustrates its scalability through the modeling of two different package configurations for the same 20 W GaN HEMT in S-band. Although both package models of Section II are validated by using conventional S-parameter measurements, Section III illustrates the most important validation step for power applications in the case of the second package configuration by using both frequency- and time-domain power measurements.

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II. EXTRACTION METHODOLOGY OF THE PACKAGE MODEL

A) On-wafer pulsed measurements of the GaN HEMT die

The modeling process starts with on-wafer pulsed-IV and pulsed-RF measurements of the GaN HEMT die which are

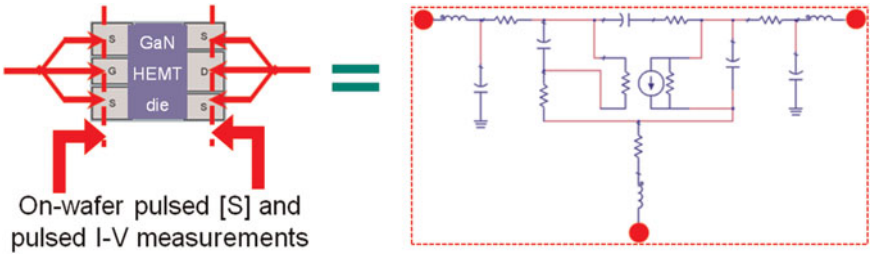

Fig. 1. On-wafer measurements and LM of the GaN die.

performed at different bias points (Fig. 1) to extract the nonlinear model of the transistor [9]. Such a nonlinear model is crucial for the validation step under large-signal operating conditions that will be presented in the last section. In addition, a linear model (LM) of the transistor chip is extracted at each bias point to be used during the modeling/synthesis procedures of its dedicated package. During this classical procedure for extracting the linear HEMT model, the cut-off bias is one of the multi-bias conditions, which is used at low frequencies for assessing the values of intrinsic capacitances Cgs, Cds, and Cgd of the transistor die. It should be noted that the proposed modeling method assumes that the designer can measure both the transistor die and the packaged transistor, which is not always the case.

B) S-parameter measurements of the packaged device

S-parameter measurements of packaged devices require the design of specific test fixtures. Consequently, a dedicated 50 Ω test fixture was designed to measure the packaged GaN HEMT (Fig. 2(a)). A 1.6-mm-thick duroïd substrate with a low dielectric constant ($\varepsilon_r = 2.2$) was selected so as to minimize the width discontinuity between 50 Ω lines (4.8 mm wide) and the package leads (5.5 mm wide). Afterwards, multi-bias S-parameter measurements were performed on the packaged transistor mounted in the test fixture, using the same bias points as those previously used for the nonlinear modeling of the transistor die. In order to remove the effects of the test fixture for determining the de-embedded measurements of the packaged device [10], a Thru-Reflect-Line (TRL) calibration kit (Fig. 2(b)) was designed and optimized on duroïd substrate for applications up to 7 GHz.

C) Architecture of the lumped-element package model

In S-band, the primary elements of metal-ceramic packages influencing the power performances of the GaN HEMT die are the package capacitances, the self and mutual inductances of bond wires, the coupling between input and output ports of the package, and the internal matching circuits. As pointed out in the introduction, the requirement of carrying out time-domain simulations for optimizing high-efficiency performances of packaged power transistors led us to adopt a lumped-element modeling approach. The passive components and interconnects of the package are modeled by equivalent electrical models, which are connected to the LM of the internal GaN HEMT die. Fig. 3 shows an example of equivalent circuit model for an initial package configuration integrating the gate, drain, and source bond wires of the device. In this package example (Fig. 3), the gate bond wire, the two parallel drain bond wires, and the four source bond wires are modeled by the equivalent inductances Lg_1, Ld_1, and Ls, respectively. The mutual inductances M_1 and M_2 are used to model the coupling between gate and drain wires, and the coupling between both drain wires, respectively. The four source bond wires are far away so as to be only modeled by their equivalent inductance Ls.

The metal-ceramic input/output pads located on both sides of the package are modeled by a shunt–series–series C_1–R_1–L_1 circuit as shown in Fig. 3. The input/output capacitance C_1 is determined by the substrate thickness H and the surface area of the metal-ceramic pad. The resistance R_1 corresponds to the metallic losses of the leads while the inductance L_1 represents parasitic effects between the package leads and the 50 Ω lines of the test fixture. The capacitance C_2 represents the forward-coupling effect of the metal-ceramic package.

In S-band, the most critical elements are the package capacitance C_1 and the bond wires (Lg_1, Ld_1), while the other elements only have an impact on harmonic frequencies.

D) Extraction of the lumped-element package model

Before optimizing the values of each lumped element that make up the package model in order to achieve the best fit between measured and simulated multi-bias S-parameters, we need to define initial values for the lumped elements.

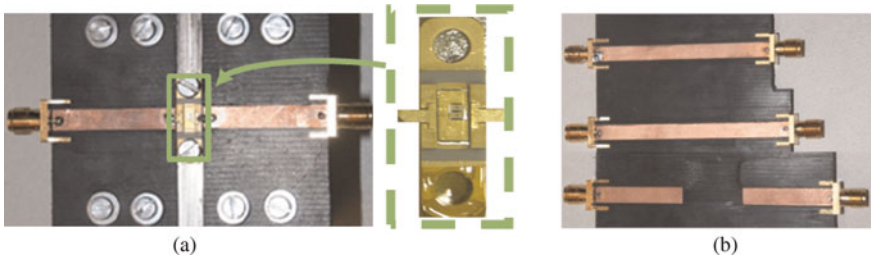

Fig. 2. (a) 50 Ω test fixture; (b) TRL calibration kit.

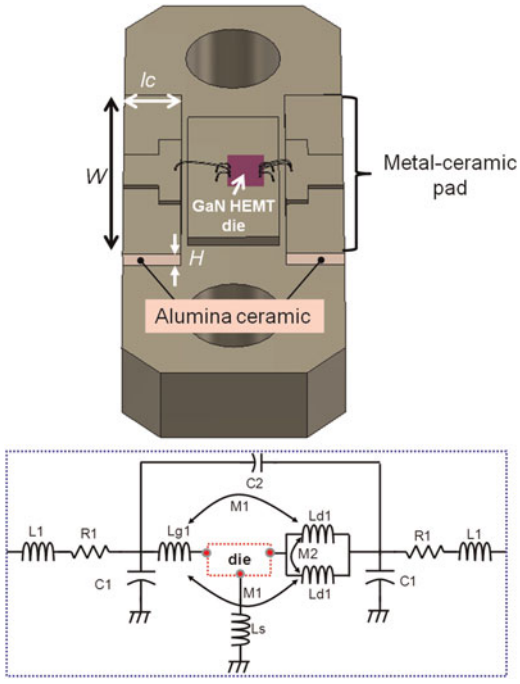

Fig. 3. Example of architecture of the lumped-element package model.

Assessing the values of the self and mutual inductances of bond wires is the most difficult step of the model initialization. However, specific calculation methods have already been published to estimate the equivalent self and mutual inductances of bond wires given their size and the distances between them. In the following equations [11] of self and mutual inductances, l and r are the length and radius of the bond wire in μm, and d is the distance between wires in μm.

$$L(\text{nH}) = 0.0002 \times l \times \left[\ln\left(\frac{2 \times l}{r}\right) - 0.75\right] \quad (1)$$

$$M(\text{nH}) = 0.0002 \times l \times \left[\ln\left(\frac{l}{d} + \sqrt{1 + \frac{l^2}{d^2}}\right) - \sqrt{1 + \frac{d^2}{l^2}} + \frac{d}{l}\right] \quad (2)$$

In order to take into account the wire shape and its height from the ground plane, the initial values of self and mutual inductances are adjusted using the Philips model [12] available in Agilent's Advanced Design System.

The value of C_1, which represents the package capacitance, is calculated using the following equation:

$$C_1 = \frac{1}{Zc} \times \frac{lc}{c/\sqrt{\varepsilon_{\text{eff}}}} \quad (3)$$

where c is the speed of light, ε_{eff} is the effective dielectric constant of the alumina substrate, while lc and Zc are the length and characteristic impedance of the metal-ceramic pad, respectively.

The values of Zc and ε_{eff} are calculated from the dielectric constant ε_r of the substrate and the aspect ratio (width/height) of the metal-ceramic pad using the equations reported in [13]. In the case of our package (Fig. 3), the characteristics of the metal-ceramic pads are ($lc = 1.5$ mm, $\varepsilon_r = 9.9$, $W/H = 12.5$) giving the following initial values ($Zc = 8\ \Omega$, $\varepsilon_{\text{eff}} = 8.7$, $C_1 = 2$ pF). Furthermore, given the cavity dimensions, EM simulations of the empty package were performed for determining the coupling capacitance C_2 between package ports, and checking that the internal cavity is free of any resonance in the frequency range of interest.

Then, using the set of bias-dependent LMs of the GaN HEMT die which were previously extracted from on-wafer measurements, the initial model of the packaged device at a given bias point is constructed by connecting the LM of the GaN HEMT die at this particular bias point to the lumped elements of the package model (Fig. 3). Therefore, we obtain a set of bias-dependent models of the packaged device which share the same values of passive-lumped elements for the package model which must be bias-independent. It can be noted that the cut-off bias, which is one of the multi-bias conditions of the measurement process, allows to assess the capacitance values of the package at low frequencies given that the intrinsic capacitances of the transistor die are already determined within the model of the transistor die.

Finally, by implementing all these bias-dependent models of the packaged GaN HEMT in the same simulation template, their identical lumped elements related to the package model are optimized to best fit the set of multi-bias S-parameter measurements performed on the packaged device (Fig. 4). Starting from the initial values of passive lumped elements for the package model, their optimized values are forced to remain within a limited range of variation so as to ensure that their final values remain closely linked to the nature and dimensions of the package constituents.

Such a constraint is very important as the physical constituents of the package (bond wires, metal-ceramic pads, etc.) have to be closely linked to their equivalent lumped elements in order to allow an efficient die-package co-design for power matching. Fig. 4 illustrates the extraction method of the package model in the case of the first package configuration.

III. PACKAGE MODELING RESULTS AND MEASUREMENTS

This modeling method was applied to a 20 W AlGaN/GaN HEMT die with 2.4 mm gate width from the GH50_10 GaN process available at UMS. A metal-ceramic power package suitable for use in S-band was selected with dimensions of 5.84×6.6 mm^2 so as to allow the integration of internal matching circuits.

Two different package configurations were realized in order to optimize power performances and highlight the scalability of this modeling method. Both package configurations are represented in Fig. 5.

In both cases, the input and output metal-ceramic pads were made of a metallic plate of Alloy-42 (6.3 mm wide, 1.5 mm long) on a 0.5-mm-thick alumina substrate. The surface area of the metal plate and the substrate thickness determine the value of the capacitance C_1. It should be noted that the output capacitance C_1 is of prime importance for the harmonic matching of the power GaN HEMT [14] because it allows the second-harmonic loads seen by the internal die to be confined to high-efficiency regions whatever the impedances presented outside the package. Therefore, in

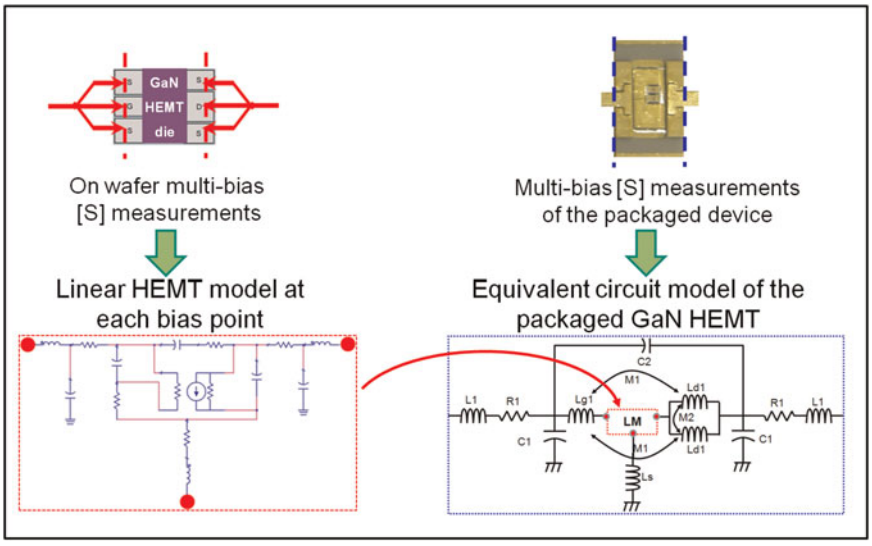

Fig. 4. Extraction procedure of package model (e.g. first package configuration).

the case of this GaN HEMT die, the required value of C_1 (~2 pF) was synthesized by realizing the suitable width (W = 6.3 mm) of the output metal-ceramic pad (lc = 1.5 mm, H = 0.5 mm).

In the case of the first package configuration (Fig. 5(a)), a single 1.8 mm long bond wire Lg_1 connects the input metal-ceramic pad to the gate pad, a pair of 1.3 mm long bond wires Ld_1 connects the drain pad to the output metal-ceramic pad, and four 0.6 mm long bond wires Ls connect the source pads to the flange. All connections use 38 μm diameter gold wires. Fig. 5(a) shows the equivalent circuit schematic of the first package configuration wherein the red box denotes the bias-dependent model of the GaN HEMT die.

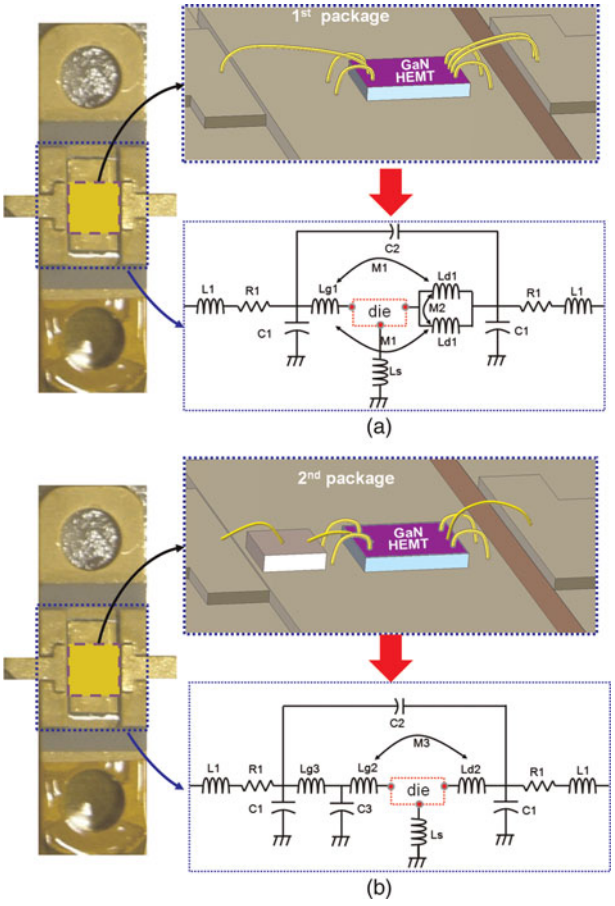

Fig. 5. (a) First and (b) second packages of the GaN HEMT and their lumped-element equivalent circuits.

Once a set of lumped-element values has been determined for the first package using the modeling method presented in the previous section, it becomes easier to design an internally matched packaged GaN HEMT by optimizing the package constituents (i.e. its lumped elements) to get the desired power characteristics in time and frequency domains. Hence, starting from the first package, an internally matched package was synthesized and fabricated to achieve improved power performances of the GaN HEMT die in S-band.

The second package structure and its equivalent circuit are shown in Fig. 5(b). The cavity dimensions, the GaN HEMT die, and the source bond wires are unchanged, while the second package integrates internal pre-matching circuits with optimized lengths of the gate and drain bond wires. The input pre-matching circuit consists of a shunt MOS capacitor (C_3 = 8.2 pF), which is connected to both the gate and the input pad by using optimized wire lengths of 0.7 mm and 1.2 mm for the inductances Lg_2 and Lg_3, respectively. The output pre-matching circuit integrates the required low-pass filter (Ld_2-C_1) for harmonic matching [14], wherein the optimum inductance Ld_2 is realized by a 2.2 mm long bond wire between the drain pad and the output metal-ceramic pad. The three bond wires Lg_2, Lg_3, and Ld_2 have a 17 μm diameter.

A) Small-signal validation of packaged GaN HEMTs

This section shows the comparison of measured and simulated S-parameters for both package configurations. Tables 1–3 list the values of equivalent circuit elements.

Figs 6 and 7 compare S-parameter measurements with electrical model simulations for the first and second package configurations, respectively.

Table 1. Lumped elements of metal-ceramic pads and source bond wires.

C_1 (pF)	R_1 (Ω)	L_1 (nH)	C_2 (pF)	Ls (nH)
2.0	0.2	0.1	0.001	0.09

Table 2. Lumped elements of the first package.

Ld_1 (nH)	M_2 (nH)	Lg_1 (nH)	M_1 (nH)
0.9	0.35	1.2	0.02

Table 3. Lumped elements of the second package.

Ld_2 (nH)	Lg_2 (nH)	M_3 (nH)	C_3 (pF)	Lg_3 (nH)
1.5	0.5	0.025	8.3	0.9

In both figures, measurements and simulations are illustrated at the optimum bias point ($Vds_o = 50$ V, $Ids_o =$ 40 mA) for maximum power added efficiency (PAE). In both cases, the equivalent circuit model achieved good agreement with measurements up to 7 GHz. In the case of high-efficiency power operation, it should be noted that the package model must remain valid up to the highest second harmonic frequency since the second harmonic load impedances have a great impact on power-added-efficiency.

The nonlinear model of the 2.4 mm GaN HEMT die has been extracted using on-wafer pulsed-IV and pulsed-RF measurements [9]. Finally, the nonlinear model of the packaged device associates the nonlinear model of the GaN HEMT die with the passive lumped elements of the second package configuration.

In order to check the reliability of this package model under large-signal operation for pulsed radar applications, pulsed load-pull measurements have been performed on the packaged GaN HEMT at the fundamental frequency of 3.2 GHz. The RF input power was pulsed using a 10 μs pulse width at a 10% duty cycle. Bias voltages were continuous with a gate bias voltage slightly above pinch-off and a drain bias voltage set to 50 V for maximizing PAE performances.

Figs 8 and 9 compare the power measurement results at 3.2 GHz with the nonlinear simulations of the packaged GaN HEMT under the same operating conditions. It should be noted that the choice of a lumped-element package model is of prime importance to enable such nonlinear simulations under pulsed conditions.

At 29 dBm input power, Fig. 8 shows a comparison between measured and simulated load-pull contours of constant PAE and constant output power in the ranges 50–70% and 40.5–42.5 dBm, respectively. A good agreement is achieved between simulations and measurements. These results are of prime importance for power amplifier design because they allow the designers to select the optimum load impedance providing the best trade-off between output power and PAE.

At 3.2 GHz, Fig. 9 shows the comparison between measured and simulated output power, PAE and gain versus input power when the packaged GaN HEMT is terminated

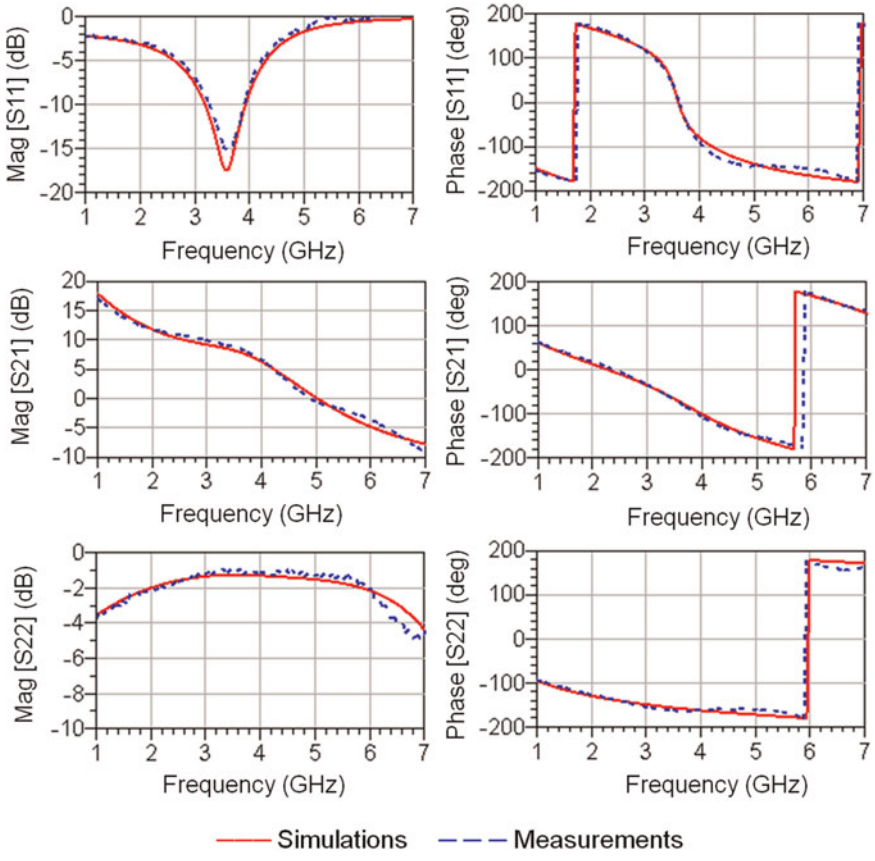

Fig. 6. Measured and simulated S-parameters of the packaged GaN HEMT (first package configuration) at ($Vdso = 50$ V, $Idso = 40$ mA) from 1 to 7 GHz.

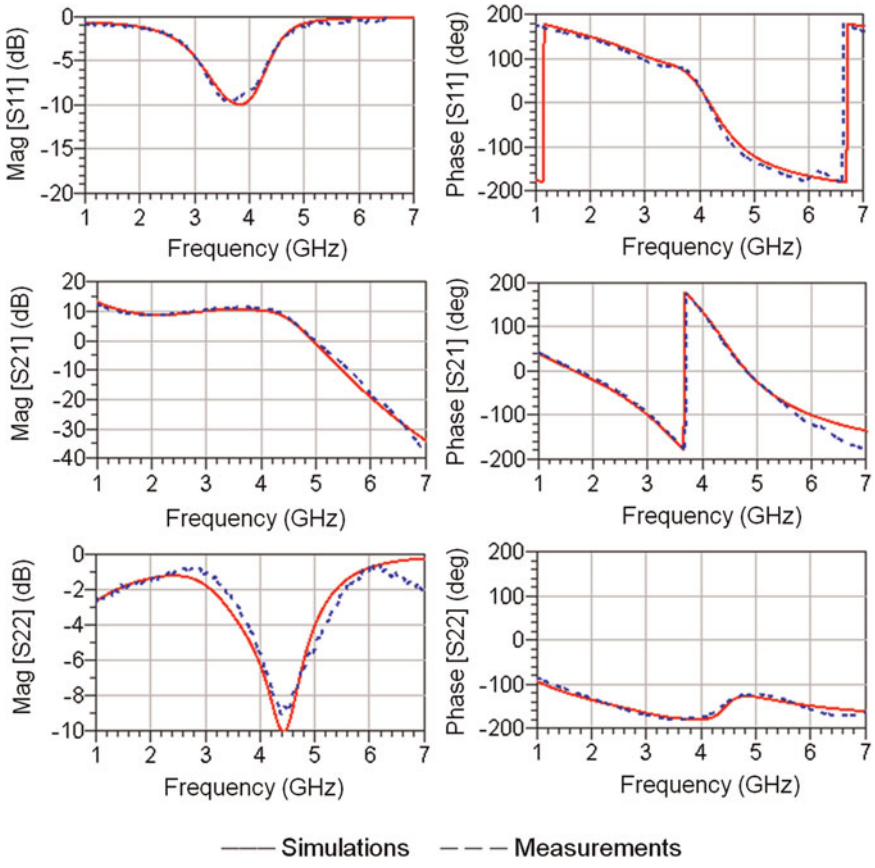

Fig. 7. Measured and simulated S-parameters of the packaged GaN HEMT (second package configuration) at ($Vdso = 50$ V, $Idso = 40$ mA) from 1 to 7 GHz.

by its optimum load impedance ($ZL_{Opt-PAE}$) for maximum PAE. The packaged GaN HEMT exhibited 70% PAE associated with 42.5 dBm output power and 13.5 dB gain at 29 dBm input power.

At the same time and under the same conditions, the output time-domain waveforms of the packaged GaN HEMT have been measured at 3.2 GHz with Agilent's PNA-X network analyzer. Using the lumped-element equivalent circuit of the package, the measurements at package plane were shifted to drain plane. Fig. 10 shows quite good agreement between measured and simulated time-domain waveforms of the drain voltage and current.

Indeed, when compared with frequency measurements, these time-domain waveforms are more visual to assess the operating mode of the internal GaN HEMT die, when placed inside the package. They also allow the designer to assess the voltage/current swings within the limits of the safe operating area. Such an insight into the intrinsic

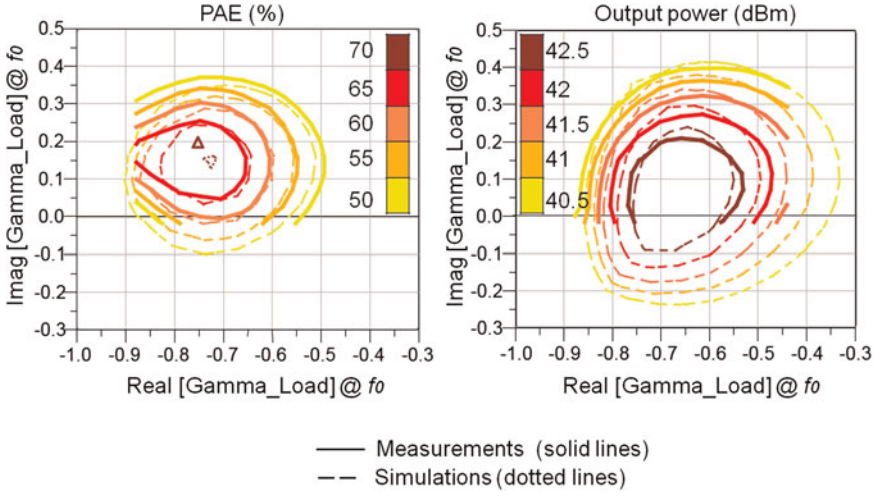

Fig. 8. Measured and simulated load-pull contours of constant PAE and constant output power in the complex plane of the load reflection coefficient (Gamma_Load) at 3.2 GHz and 29 dBm input power.

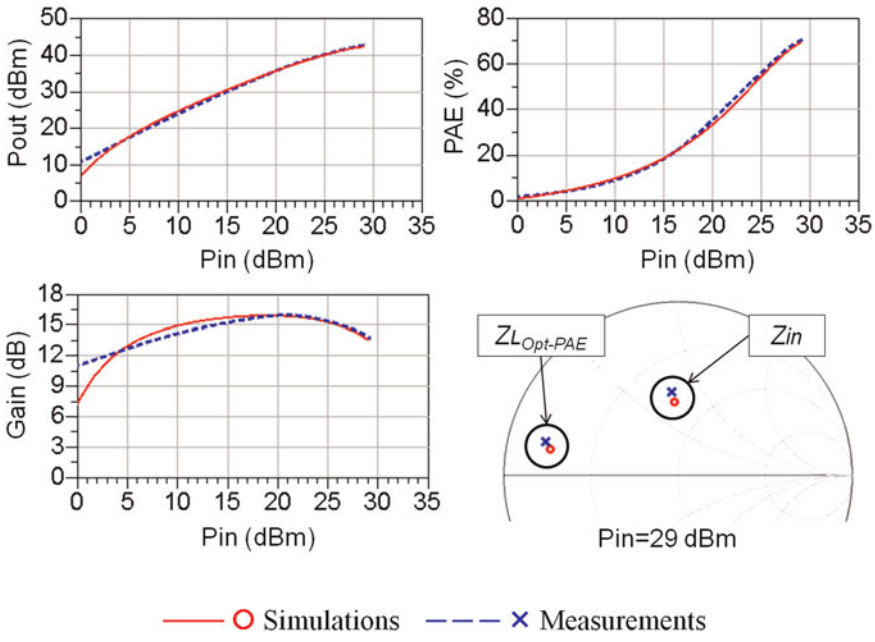

Fig. 9. Comparison between measured and simulated output power, PAE, gain and optimum loads when the packaged GaN HEMT is loaded on its optimum load impedance ($ZL_{Opt-PAE}$) for maximum PAE at 3.2 GHz.

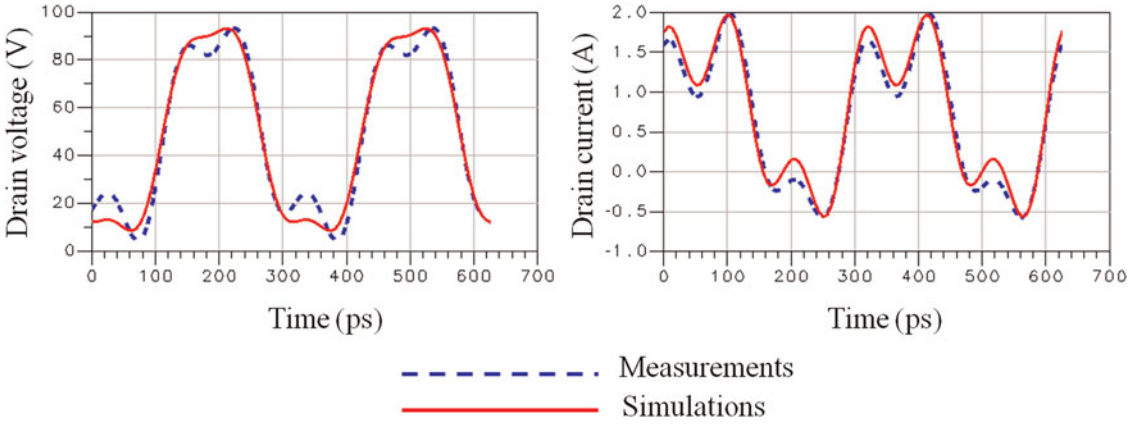

Fig. 10. Comparison of measured and simulated time-domain waveforms at the drain plane of the GaN die at 3.2 GHz and 29 dBm input power.

large-signal behavior of the packaged GaN HEMT die is made possible through the use of a lumped equivalent circuit model of the package.

IV. CONCLUSION

This study highlights the advantages of a lumped-element package model for designing high-efficiency hybrid power amplifiers in S-band. At first, the nonlinear model of the transistor die is extracted from on-wafer pulsed-IV and pulsed-RF measurements. Then, the passive components and interconnects that make up the package are modeled by equivalent lumped elements so that the final model of the packaged transistor associates the nonlinear model of the transistor die with the passive lumped-element model of the package. Finally, given the nonlinear model of the transistor die, the lumped-element package model is extracted from multi-bias S-parameter measurements of the packaged transistor. Starting from initial values of passive lumped elements for the package model, their optimized values are forced to remain within a limited range of variation so as to ensure that their final values remain closely linked to the nature and dimensions of the package constituents. Therefore, the package model presents scaling properties and allows designers to synthesize the internal components and interconnects of the package that will meet the impedance matching requirements of the transistor for power operation.

The modeling methodology is illustrated through two package examples of a 20 W GaN HEMT in S-band. Linear and nonlinear simulations of the packaged GaN HEMT model show a good agreement with measurements of S-parameters, load-pull contours and time-domain waveforms. This large-signal validation is critical for the efficient design of hybrid power amplifiers since the package has a considerable impact on the internal device capabilities. It should be noted

that the package modeling method with passive lumped elements is well suited in S-band, whereas EM modeling becomes more and more essential with increasing frequency.

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