

Design of an Integrated Cascode Cell for Compact Ku-Band Power Amplifiers

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Abstract—This paper reports on the design of a new power cell dedicated to Ku-band power amplifier (PA) applications. This cell called “integrated cascode” has been designed in order to propose a strong decrease in term of circuit size for Power Amplifier (PA). The technology used relies on 0.25- μm GaAs Pseudomorphic High Electron Mobility Transistors (PHEMT) of United Monolithic Semiconductors (UMS) foundry. A distributed approach is proposed in order to model this power cell. The challenge consists to obtain, with a better shape factor (ratio between the vertical and horizontal sizes of the transistor), the same performances than a single transistor with the same gate development. In order to design a 2W amplifier, we have used two 12x100 μm transistors. Cascode vertical size is 413 μm whereas a transistor with the same gate development exhibits a vertical size of 790 μm . Therefore the shape factor is nearly one as compared to a shape factor of 4 for a classical parallel architecture. This new device allows to decrease the MMIC amplifier area of 40 % compared with amplifier based on single transistors.

I. INTRODUCTION

The important demand of power amplifiers with high performances and low cost requires the development of more and more compact chips [1] [2]. To increase the compactness of these amplifiers, one solution consists in decreasing the size of its unitary cell, while increasing their gain and improving their shape factor which is defined as the ratio between the vertical size and the horizontal size. A shape factor close to one would reduce the total vertical size of the PA therefore would minimize the total area of the PA. To reach this objective a new topology of elementary power cells in MMIC technology must be designed. The keypoint of this design is to provide the same power performances than a single transistor with the same gate development and a shape factor of one. A new cell based on cascode theory appears to be a good candidate for this task.

II. MMIC TECHNOLOGY

The new cell reported in this paper is used for Ku band PA. It has been designed with 0.25 μm GaAs PHEMT [3]. The MMIC fabrication is based on double recess power PHEMT process, using 0.25 μm Aluminum T-gates. The MMIC has been realized on 70 μm substrate, 30 Ω/\square TaN thin film

resistor, 250 pF/mm² MIM capacitors, air bridges and 20 μm via holes. A 1.2 mm gate width transistor, with small via holes under each source is used to design this cell thus ensuring a high gain and a good thermal stability.

III. POWER CELL MMIC DESIGN

A. Cascode cell topology

Various amplifiers with cascode cells have been proposed in literature mainly in order to obtain either a wide band [4] [5] [6], or a high gain at very high frequencies, especially for GaN HEMT technology [7]. However no attempts have been made with integrated stability resistance and capacities between gate fingers. This new topology allows to decrease the shape factor of the transistors while maintaining the advantages of the cascode configuration. This new cell is made of two transistors in cascade as shown in Fig.1.

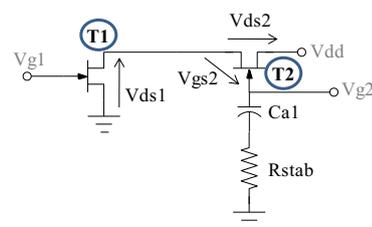


Fig. 1. Cascode cell topology schematic

The first one is in a common source configuration. Its drain is connected to the source of the second transistor which is in a common gate configuration. The goal of this topology is to add drain voltage of each transistor which are both conducting the same drain current. Therefore, output power and gain of cascode is twice bigger than for a single transistor. Other advantages of this cell rely also in the ability of doubling the drain bias voltage which leads to a higher output impedance and to a better input/output isolation. In order to add the drain source voltages of the transistors some care must be taken to adapt the levels of voltage applied to the gate of transistor (T2).

Indeed, in large signal, V_{ds1} voltage is applied directly to the gate of transistor in common gate configuration (T2). Without any precaution this transistor would be quickly saturated and would be destroyed. Therefore, a capacitance (C_{a1}) is added in series with the gate as shown in Fig.1. This capacitance (C_{a1}) and the input capacitance C_{gs2} act as a frequency independent voltage divider between V_{ds1} and V_{gs2} . The second transistor is biased through a 1000 Ω resistance. Cascode cell being sensitive to oscillations, a resistance R_{stab} is added in series with C_{a1} capacitance to limit all instability phenomena. Both values of C_{a1} and R_{stab} have been optimized in order to propose a trade-off between power performances and stability.

B. Integrated Cascode layout

The layout of the compact cell is shown in Fig.2.

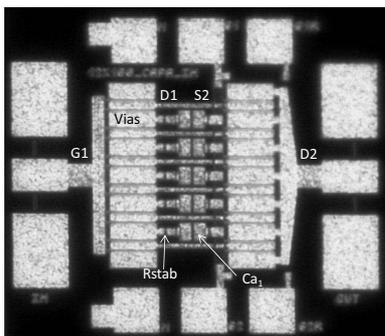


Fig. 2. Cascode cell layout

Drains of common source transistor are also sources of common gate transistor thanks to micro-strip line which crosses the gate bus through air bridges. This provides an integrated aspect to the cascode cell. Thanks to vias holes in sources of the first transistor, both C_{a1} capacitance and R_{stab} resistance are distributed between each two gate finger pairs. This configuration ensures a perfect symmetry in the topology of the power cell. The number of elementary cells of two gate fingers can be adjusted to the total power required. As mentioned previously, vertical size is 413 μm whereas the vertical size of a single transistor with the same gate development is 790 μm leading to an improvement of 48% in the vertical size and a shape factor which is nearly one. Fig.3 shows that integrated cascode exhibits a higher linear gain, a better output impedance and a better input/output isolation than a single transistor with the same gate development.

IV. MODELING AND REALIZATION

A. Distributed approach

The cascode design has been performed through a distributed approach. Firstly, we have extracted intrinsic and extrinsic circuit parameters of 12x125 μm transistor. As transistor model is scalable we have replaced 12x125 μm transistor by 6 transistors of two gate fingers and we have compared this simulation with 12x125 μm transistor measurements. Gate and drain buses are simulated with an electromagnetic software,

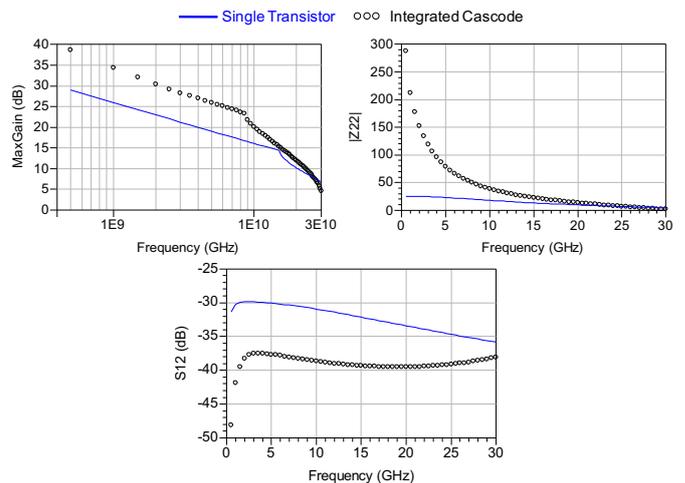


Fig. 3. Comparison of S_{12} , Z_{22} and Maximum Available Gain between an integrated cascode cell and a single transistor with the same gate development

ADS-Momentum. We have adjusted 2 gate fingers transistor model in order to have a good agreement between this model and measurements (Fig.4, Fig.5).

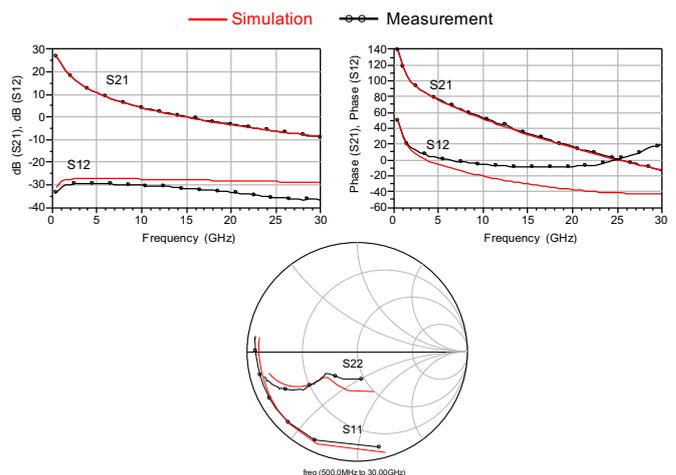


Fig. 4. [S] parameters measurements of 12x125 μm transistor compared with its distributed model composed by 6 transistors of two gate fingers

In the integrated cascode, the scalable model of transistor with 12 gate fingers of 100 μm width has been replaced by six transistors of two gate fingers with the same development. Fig.6 shows integrated cascode modeling. Passive elements have been simulated with ADS-Momentum [8]. Both C_{a1} and R_{stab} values have been optimized in order to obtain good power performances and to ensure stability of cascode cell. The total values found are $C_{a1} = 525$ fF and $R_{stab} = 3\Omega$ which are distributed in 5 elementary cells with $R_{stab} = 15\Omega$ and $C_{a1} = 105$ fF. In order to validate the power optimization of the cascode cell, Fig.7 shows the simulated intrinsic load lines for both transistor T1 and T2 at 12 GHz in the same load conditions as those used for the

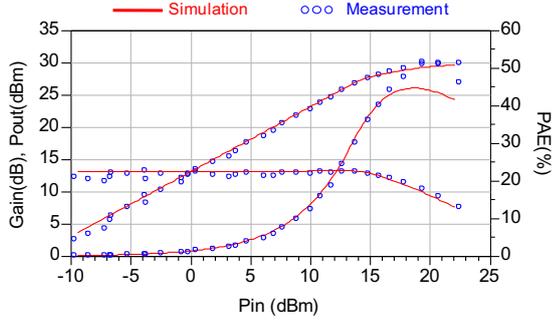


Fig. 5. Load pull measurements of $12 \times 125 \mu\text{m}$ transistor with its distributed model @ 12 GHz for $Z_{load} = 13.3 + j17.4 \Omega$

load pull power measurements presented in the next section (ie $Z_{load} = 16.5 + j20.2 \Omega$). One can observe the excellent optimization for T2. However T1 remains not fully optimized. Some approaches such as "self biased optimization" technique [9] have been tried, without convincing results. A trade-off between power optimization and shape factor has been done to give the topology shown in Fig.2.

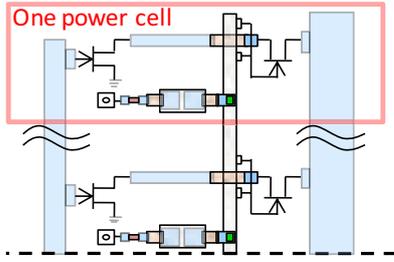


Fig. 6. Distributed model of integrated cascode

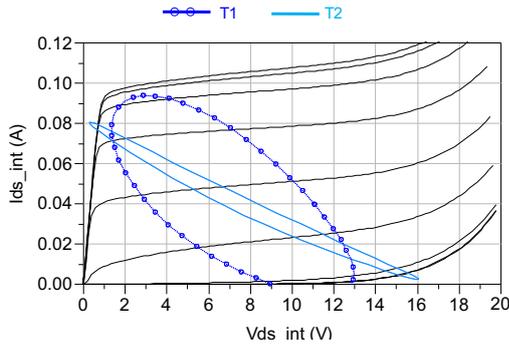


Fig. 7. Load cycles of each transistor

B. Stability analysis

Due to a high gain, cascode cell is sensitive to oscillations. That is why linear stability analysis must be performed [10]. Fig.8 shows the Rollet factor K and the determinant Δ of S matrix. K exhibits that cascode cell is unconditionally stable between 8 and 30 GHz. We can conclude that cascode cell

is stable for all loads in the Ku band. However, this study reveals that cascode cell is conditionally stable from 0 to 8 GHz. Therefore, the stability circles from 0 to 40 GHz have been examined. The design has been done to ensure the linear stability of the power cell on the whole frequency range. All output stability circles are out of the Smith chart. This confirms the linear stability of this device. During measurements, no oscillation appeared, validating the stability approach.

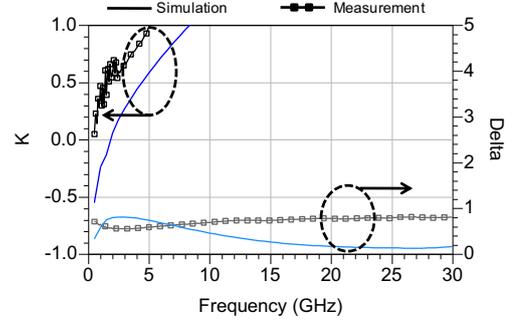


Fig. 8. Rollet factor and delta of $[S]$ parameters matrix

C. Thermal stability analysis

Cascode cell presents good power performances if both transistors are biased with the same voltage. As the two output current sources of transistors (T1) and (T2) are in series, one could suspect that the bias voltages V_{ds1} and V_{ds2} are prone to derive under the influence of temperature and lead to an over bias of one of the transistors. In fact as T2 is driven by the current of T1, this current imposes the value of the gate/source voltage of T2 maintaining T2 in its saturation region. Therefore $V_{ds1} = V_{g2} - V_{gs2} = V_{dd} - V_{ds2}$ and the voltage equilibrium between T1 and T2 is ensured by a correct choice of the T2 gate bias. This ensures thermal stability of the cascode. This has been confirmed through the use of an electro-thermal model specially developed for that study. A 3D thermal simulation revealing a poor coupling between T1 and T2 has been performed in ANSYS. The self thermal resistance of T1 is 10 % lower than T2 due to small via in sources.

V. MEASUREMENTS AND RESULTS

The on chip measurements of small signal gain and input/output return losses of the designed PHEMT integrated cascode cell are shown in Fig.9. We can observe a good agreement between measurements and the distributed model. The model has been validated with load pull power sweep at 12 GHz for the optimum load impedance (Fig.10).

VI. INTEGRATED CASCODE PHEMT PA MMIC

Using the distributed model of integrated cascode, a two stages 2W PA for Ku band has been designed (Fig.11). Its area is decreased of 40% compared with the initial amplifier.

A comparison between measurements and simulations for $[S]$ parameters and for power measurements is shown Fig.12. A good agreement is observed and this amplifier achieves a

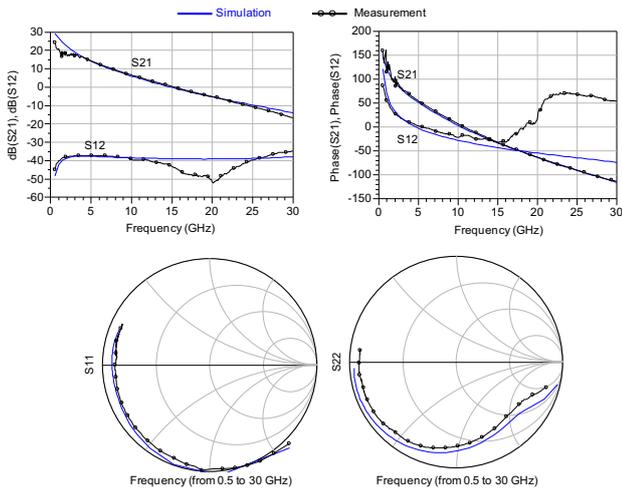


Fig. 9. Measured and distributed model [S] parameters of a cascode cell in the 0.5 to 30 GHz range ($V_{dd}=16V$, $I_{ds}=160mA$)

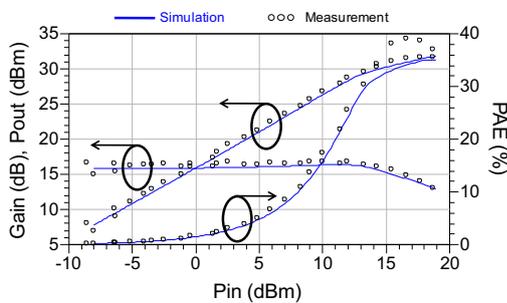


Fig. 10. Measured and modeled power sweep of cascode cell at 12GHz ($V_{dd}=16V$, $I_{ds}=160mA$)

linear gain of 22 dB on the whole frequency range 12 to 16 GHz. Moreover, we can observe an output power of 33 dBm and 21 % PAE on the frequency band 12.5 to 15.5 GHz for $P_{in}=10dBm$. So we have obtained the same performances than the first designed amplifier (the reference for this work).

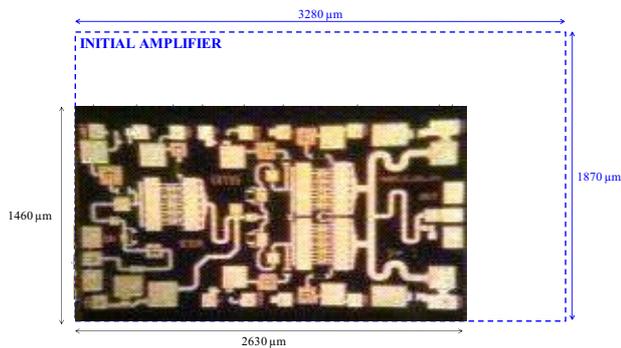


Fig. 11. 2W amplifier layout

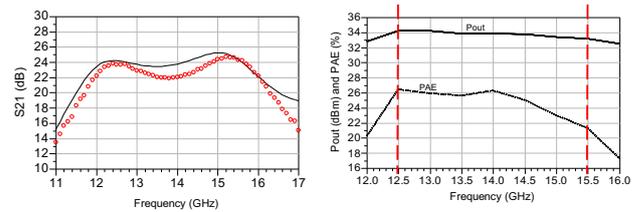


Fig. 12. Measured and distributed model [S] parameters of a cascode cell in the 11 to 17GHz range, measured output power and PAE from 12 to 16GHz ($V_{dd}=16V$, $I_{ds}=160mA$)

VII. CONCLUSION

This paper has reported the design modeling of a new integrated cascode cell. This new cell is more compact than a single transistor with the same gate development and exhibits the same power performances. The very good agreement between simulation results and measured data shows the accuracy of the non linear model and also the efficiency of the design approach. Thanks to these promising results a Ku-band compact amplifier has been designed. Its area has been decreased of 40%. Measurements are the same than the initial amplifier, so the area power density has increased, it is equal to $573 mW/mm^2$ ($326mW/mm^2$ for the initial amplifier).

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