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Published in

Electronics Letters, 6th December 2012 Vol. 48 No. 25, pp.1607-1608.

Crossref DOI: 10.1049/el.2012.3004

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Time-reversal duality of high-efficiency RF power amplifiers

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The similarity between RF power amplifiers and rectifiers is discussed. It is shown that the same high-efficiency harmonically-terminated power amplifier can be operated in a dual rectifier mode. Nonlinear simulations with a GaN HEMT transistor model show the time-reversal intrinsic voltage and current waveform relationship between a class-F amplifier and rectifier. Measurements on a class-F⁻¹ amplifier and rectifier at 2.14 GHz demonstrate over 80% efficiency in both cases.

Introduction: High-efficiency RF power amplifiers (PAs) are designed by presenting appropriate output impedances at the fundamental and harmonic frequencies, shaping the current and voltage waveforms across the current source of the device to minimise the power dissipation $v(t) \times i(t)$. In the past few years, PAs implemented in GaN technology have demonstrated power added efficiencies (PAEs) above 80% using a single transistor. In this Letter, we show that a harmonically-terminated transistor amplifier is a bidirectional device that exhibits high efficiency in both amplifier and rectifier modes. High power conversion efficiency of a power amplifier (DC to RF) and a rectifier obtained by operating the amplifier in reverse (RF to DC) is achieved with time-reversal duality [1] of the transistor's main current source. In other words, the power amplifier (PA) and rectifier (R) drain terminal voltage and current are related by $v_{PA}(t) = v_R(t)$ and $i_{PA}(t) = -i_R(t)$. The block diagram in Fig. 1 shows the main PA and rectifier parameters that are discussed here. The matching networks are designed to optimise PA efficiency for a 50 Ω load and are not changed for rectifier mode operation.

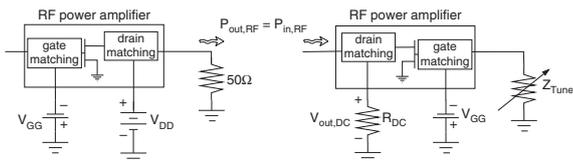


Fig. 1 Block diagram of power amplifier circuit operated in PA mode (left) and rectifier mode (right)

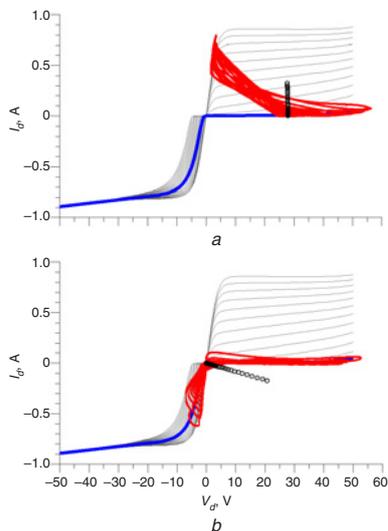


Fig. 2 Simulated GaN transistor $I-V$ curves (grey), dynamic load lines (red) and drain DC voltage and current (black) for PA of Fig. 2a and rectifier (Fig. 2b). Blue line is $V_{GS} = -4.9V$ transistor characteristic (gate bias point value for both cases). Time-reversal duality is seen as RF power at drain and is swept from 0 to 40 dBm at 2.14 GHz. PA case has drain bias of 28 V

In the remainder of the Letter, example simulations of a class-F amplifier based on a GaN HEMT illustrate the time-reversal duality of power amplifiers and rectifiers. Nonlinear simulations result in time-reversed dual current and voltage waveforms at the virtual drain of the PA and rectifier. After the principle is demonstrated through simulations of intrinsic waveforms, measurements on a class-F⁻¹ GaN power amplifier

using a TriQuint device are compared for PA and rectifier configurations, with the goal of demonstrating that this duality holds for various high-efficiency amplifier and rectifier circuits.

Simulations of PA and rectifier: Simulations have been performed with the $8 \times 75 \mu\text{m}$ GaN HEMT model described in [2] at 2.14 GHz. This nonlinear model includes: nonlinear capacitances C_{gs} , C_{gd} and C_{ds} ; gate-source and gate-drain diodes; and breakdown and trapping effects. This model reproduces the nonlinear transistor behaviour not only for positive but also for negative values of the drain voltage.

For the amplifier mode of operation, when an input RF signal is injected into the gate terminal, we consider the drain efficiency, or DC-to-RF conversion efficiency: $\eta_{PA} = P_{out,RF}/P_{DC}$. In class-F mode with five harmonics terminated, for $V_{ds} = 28V$ and $V_{gs} = -4.9V$, an amplifier efficiency $\eta_{PA} = 72\%$ is obtained. The simulated behaviour of the transistor is depicted on Figs. 2a and 3a, showing the $I-V$ curves and load-line, and intrinsic drain voltage and current waveforms, respectively.

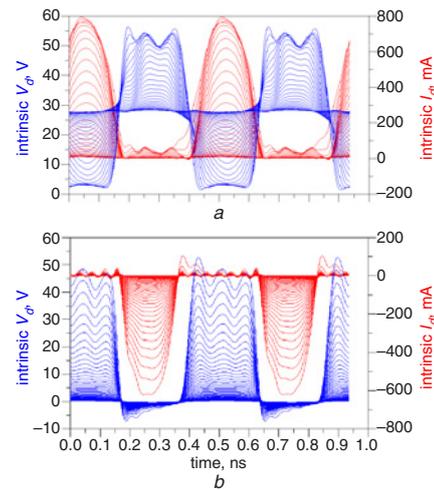


Fig. 3 Simulated time-domain intrinsic drain voltage (blue) and current (red) waveforms for varying RF power at drain for PA (Fig. 3a) and rectifier (Fig. 3b). In the case of PA, $V_{ds} = 28V$

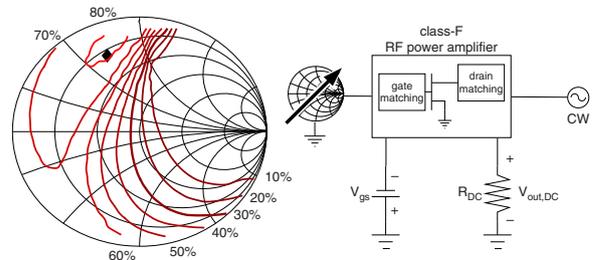


Fig. 4 Load-pull simulations for rectifier efficiency obtained at transistor terminals. Frequency is 2.45 GHz and RF drain input power is 40 dBm. Diamond symbol shows impedance for maximal efficiency

The same class-F PA circuit is next simulated in rectifier mode, where the drain DC power supply is replaced by a DC load R_{DC} . The input to the circuit is now RF power $P_{in,RF}$ equal to $P_{out,RF}$ of the amplifier, and injected at the drain port as illustrated in Fig. 4. Assuming the DC gate current is negligible, the rectifier RF-to-DC conversion efficiency is

$$\eta_R = \frac{P_{DC}}{P_{in,RF}} = \frac{2|V_{DC}|^2}{R_{DC} \Re\{V_{drain}(f_0)I_{drain}^*(f_0)\}} \quad (1)$$

An impedance tuner connected at the gate input of the PA allows load-pull at the gate resulting in $\eta_R = 80\%$ with $R_{DC} = 120\Omega$ ($f_{RF} = 2.14\text{GHz}$). Figs. 2b and 3b illustrate the behaviour of the transistor for RF gate load impedance that maximises rectifier efficiency. The waveforms at the intrinsic drain of the transistor correspond to time-reversed class-F waveforms. The gate-port load-pull contours are displayed in Fig. 4. The Figure also shows the optimal impedance for η_R at f_{RF} which is related to a dynamic load-line with a minimal enclosed area, and close to the $I-V$ characteristic given at constant V_{GS} .

