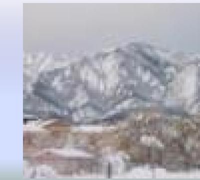
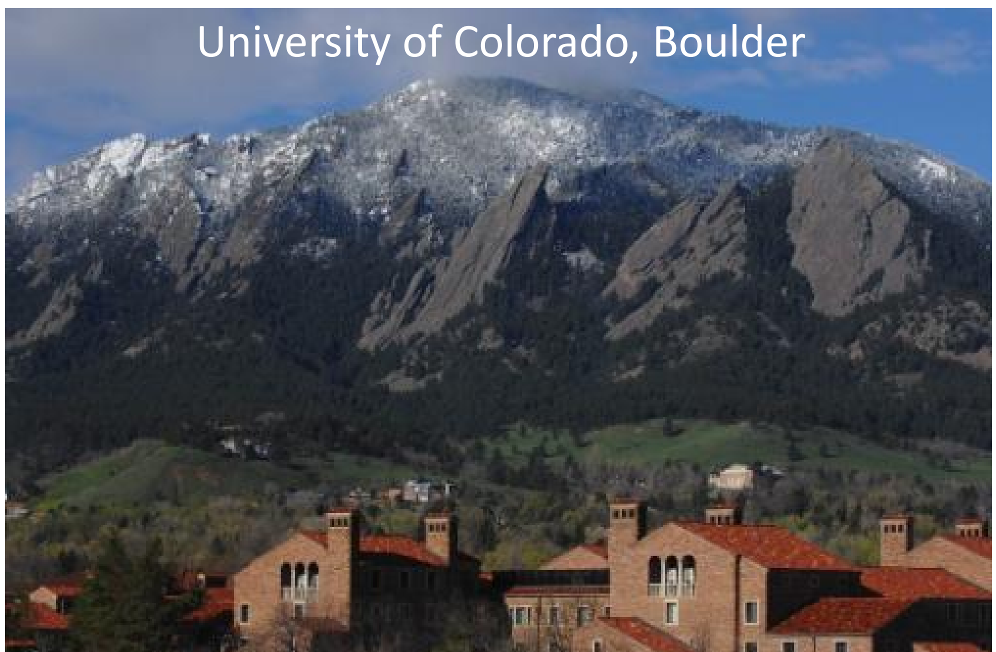


Design and measurements of high-efficiency PAs with high PAR signals

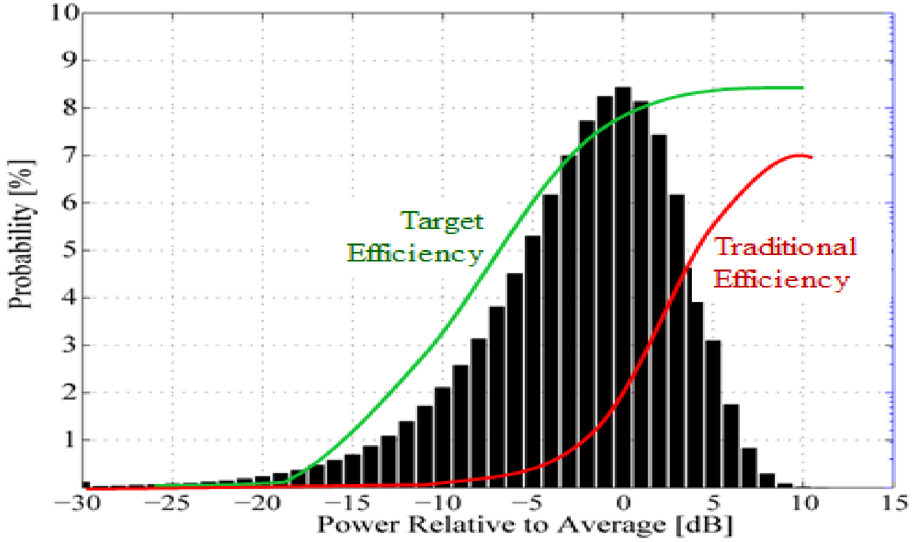
Zoya Popovic, Tibault Reveyrand, David Sardin, Mike Litchfield, Scott Schafer, Andrew Zai

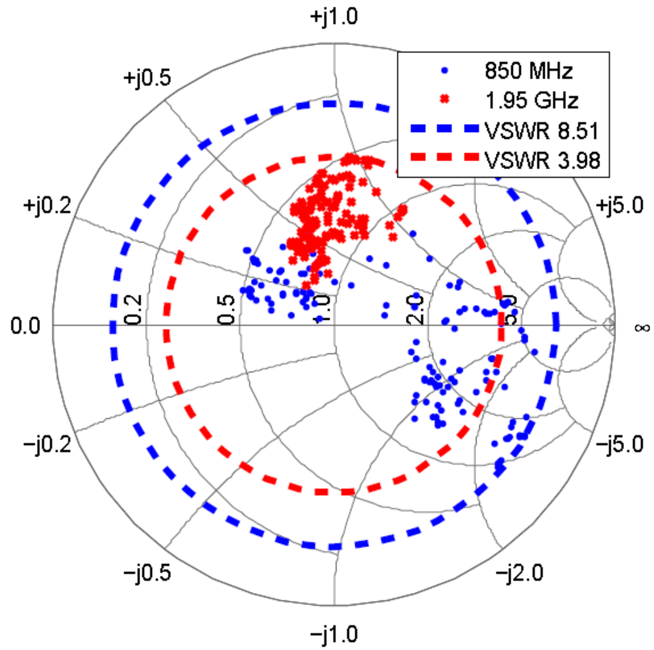
Department of Electrical, Computer and Energy Engineering

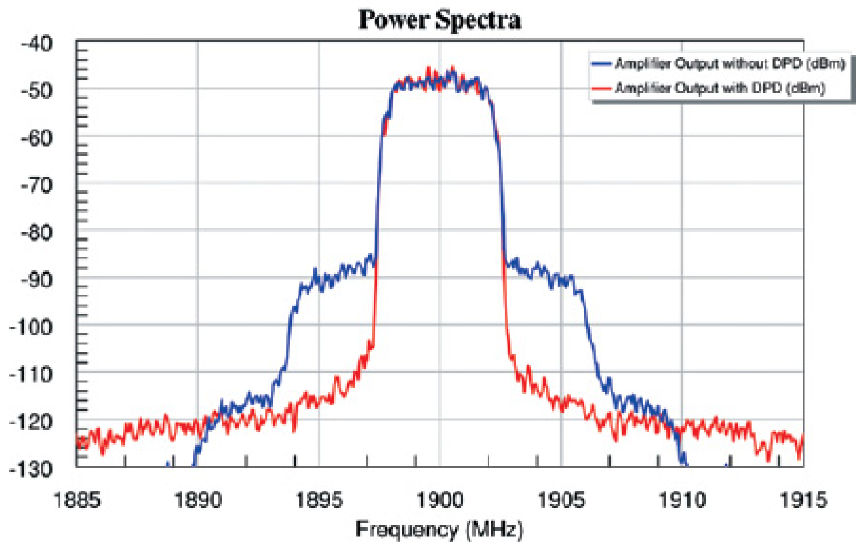


Main challenges in PA design

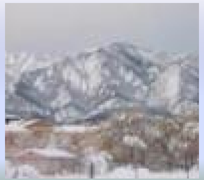
- Challenge 1: efficiency drops as output power drops
- Challenge 2: efficient PAs are nonlinear
- Challenge 3: load can vary





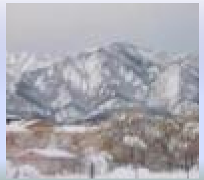


Outline

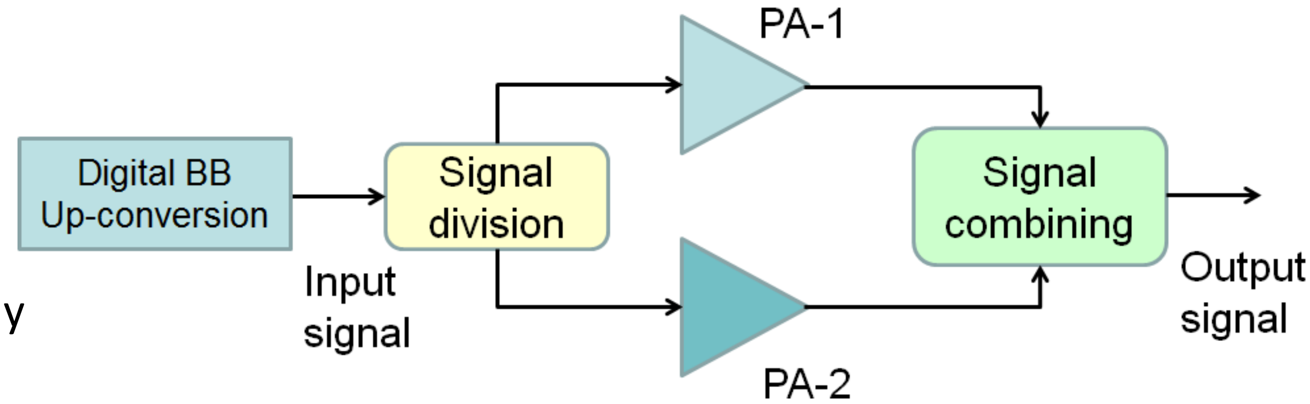


- **Overview of approaches for improving efficiency at power back-off**
- Supply modulation
  - GaN PA design (10GHz carrier)
  - Supply modulator (100MHz switching)
  - Integration and modeling
- Outphasing
  - Quasi-MMIC isolated and non-isolated
  - Measurements of load modulation internal to the PA
  - Outphasing with supply modulation
- Discussion and some other challenges

Transmitter architectures



- Doherty PAs
  - Main and peaking RFPAs
  - Digital drive
  - Combined with supply modulation
- Supply modulation (ET…)
  - Various methods
  - One RFPA, lower frequency PA, dc-dc converter(s)
- Outphasing (LINC, Chireix)
  - Two saturated RFPAs
  - Digital pre-processing
  - Combined with supply modulation

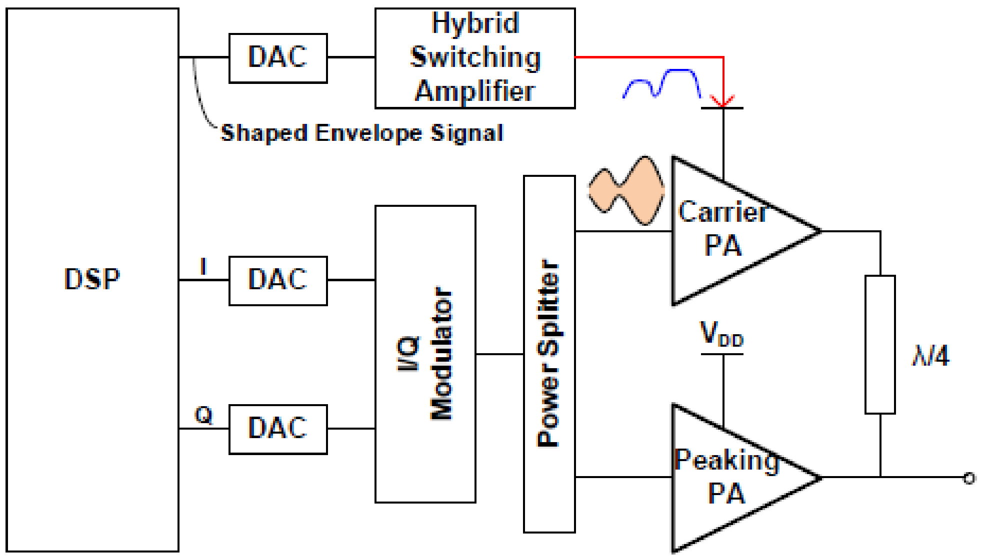


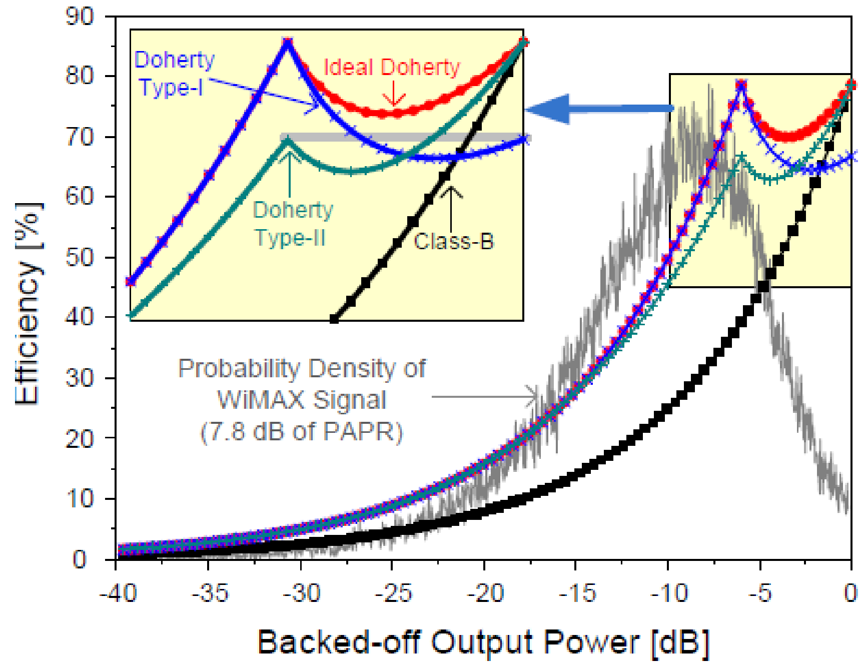
➢ Need second amplifier of some sort, complexity increases

➢ Is the added complexity worth it?

Doherty PAs

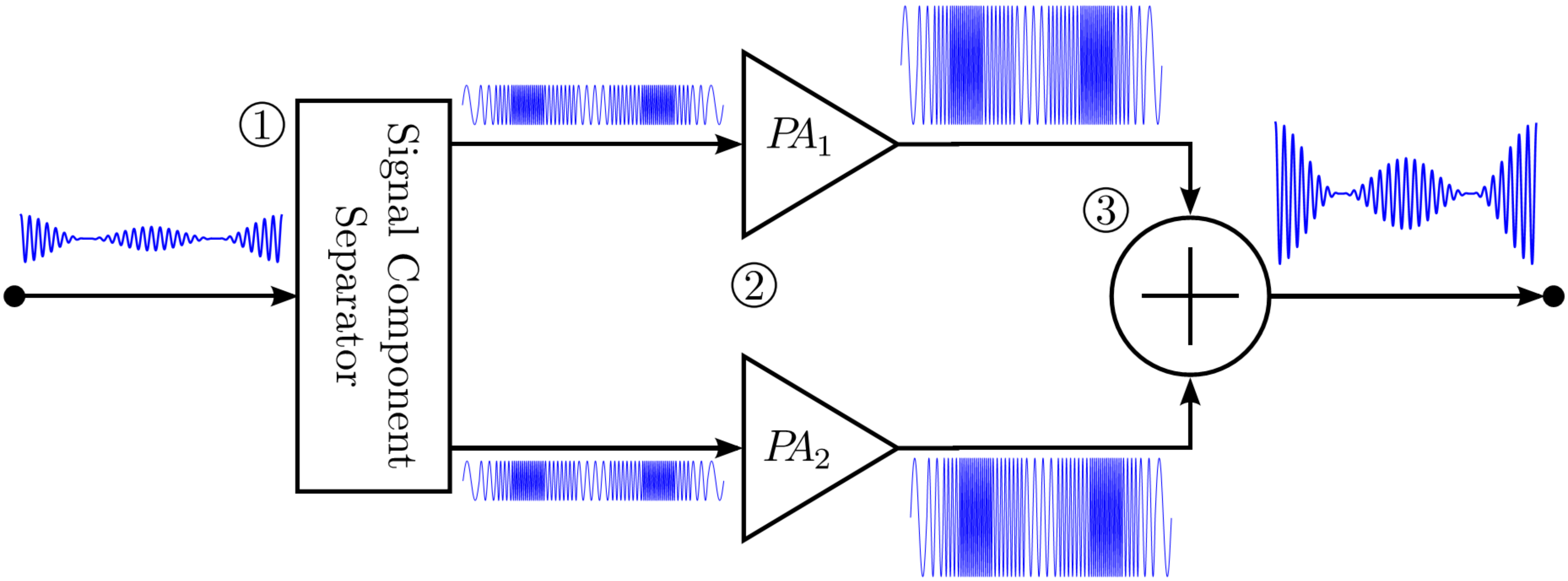
- Limitations: broadband signals; efficiency in back-off limited (class AB-B)
- Non-ideal peaking amplifier current turn-on characteristics
- Needs linearization although carrier PA is in principal linear
- Currently ~60% peak, 40% average for WCDMA and LTE, 2GHz





From B. Kim et al, 2010

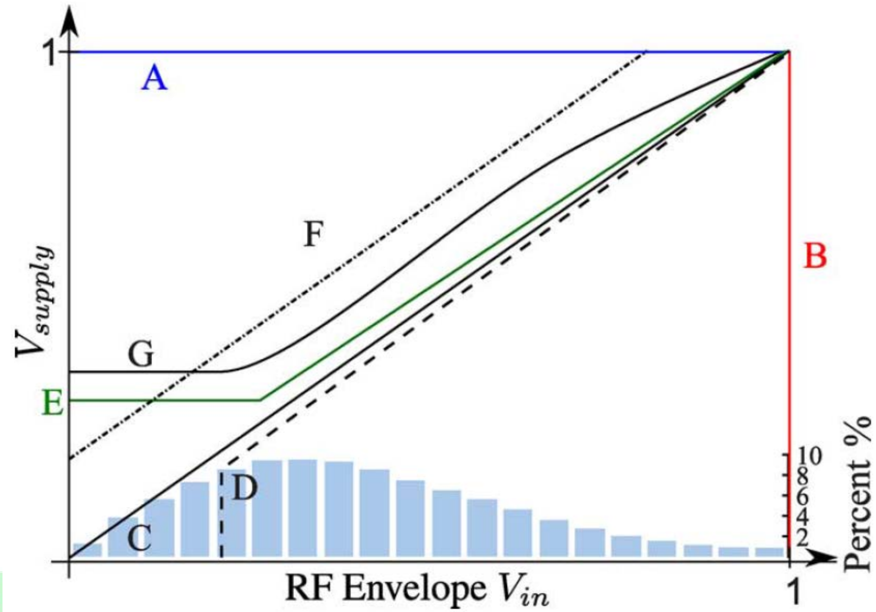
Outphasing (LINC) PAs

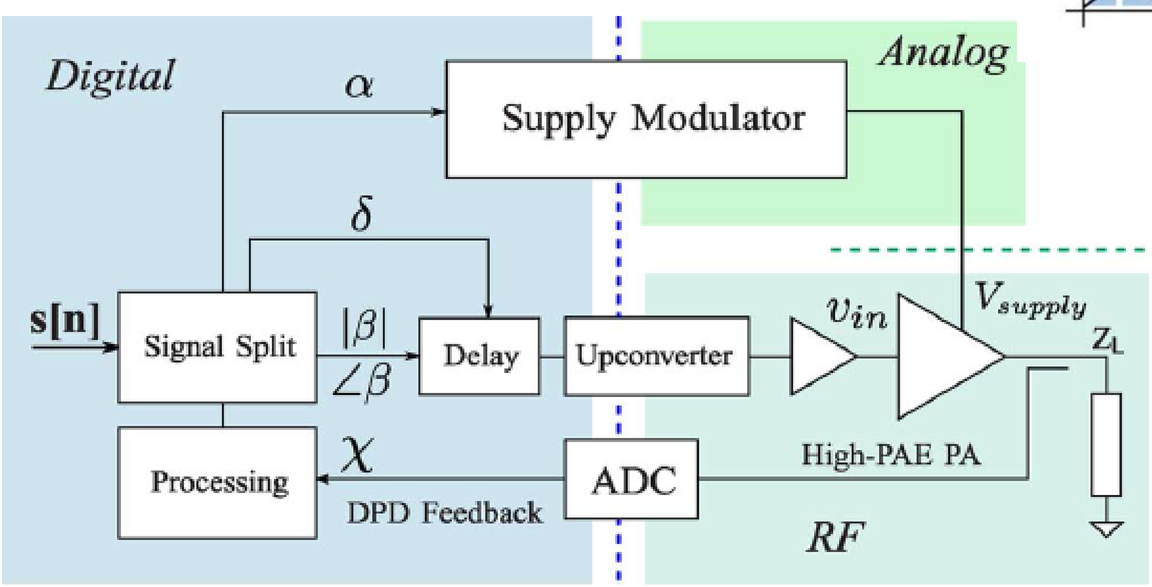


- Amplitude modulation converted to additional phase modulation
- High-efficiency PAs driven with constant envelope
- Combiner reconstructs envelope through vector addition
- Combiner can be isolated or non-isolated

Supply Modulation (ET)

- Various names used in the literature: EER, ET, polar, PDM, WBET, HQPM, HEER, DDVB…
- PAs designed as AB, E, F, F-1, C, J…





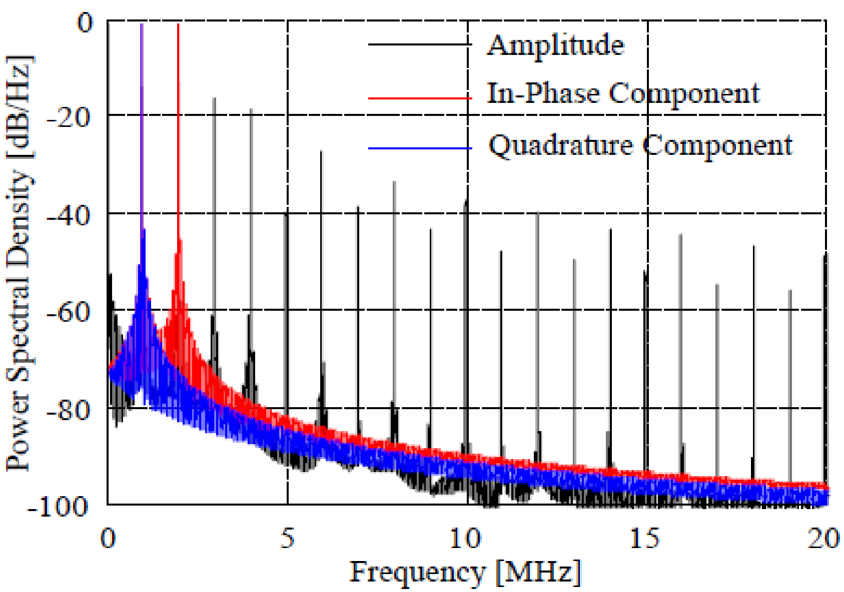
Need:
- Efficient RFPA
- Efficient supply modulator
- Linearization

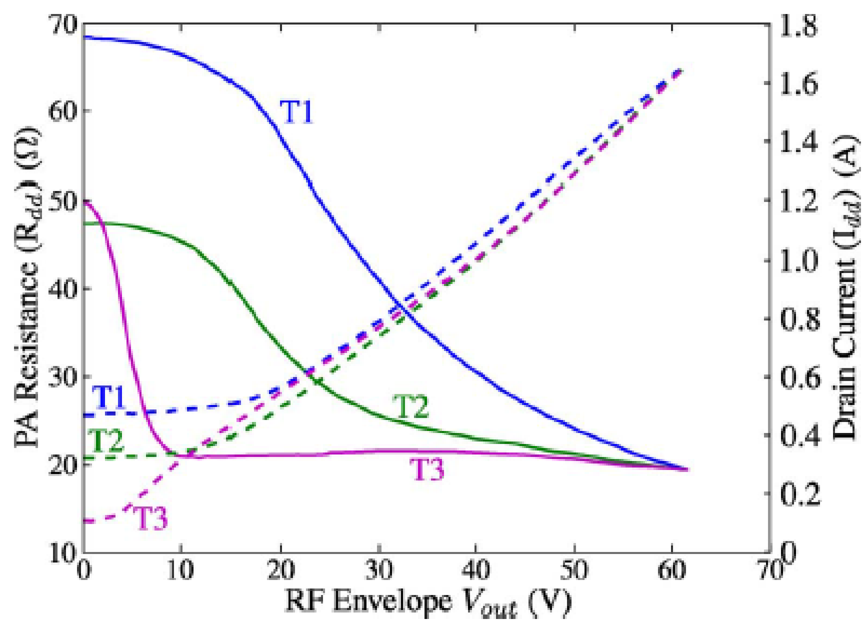
PAs with Supply Modulation

Challenges:

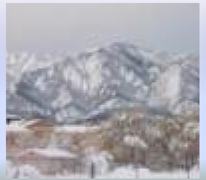
- High-efficiency PA design over large range of drain bias
- High-efficiency envelope-bandwidth supply modulator design
- Dynamic loading between PA and supply modulator
- Various forms of distortion

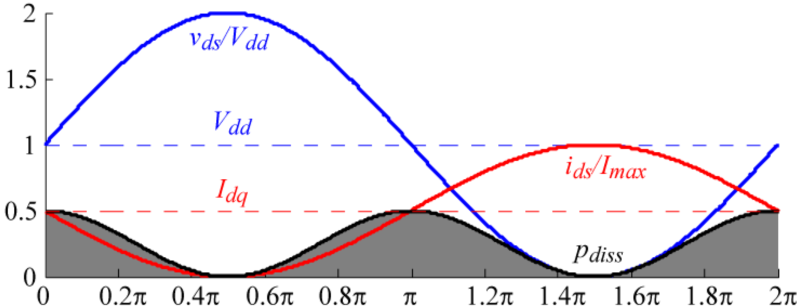
Benefit: heat distributed between PA and SM



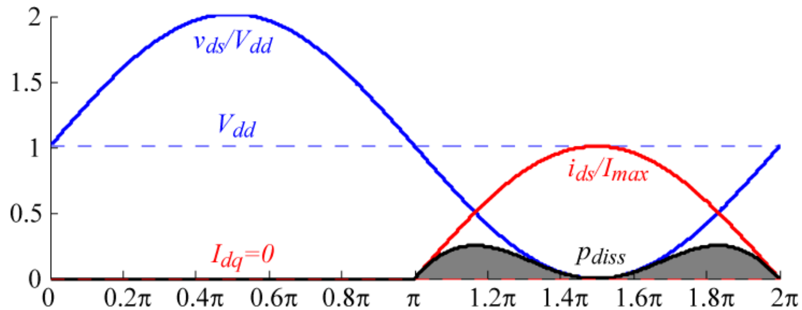


High-efficiency PA design

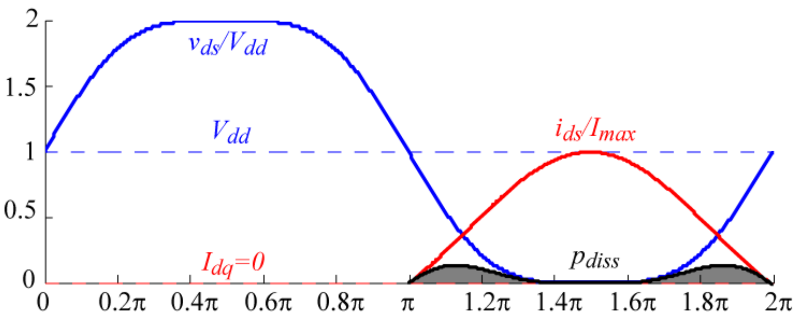




Ideal class-A drain waveforms



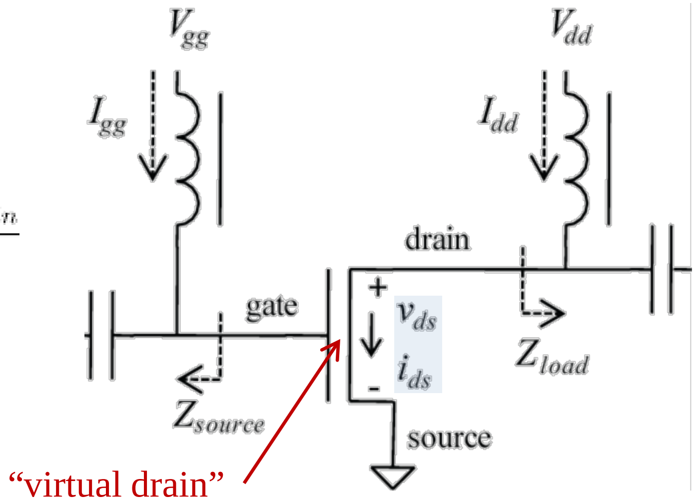
Ideal class-B drain waveforms



Ideal class F drain waveforms with only 3 harmonics

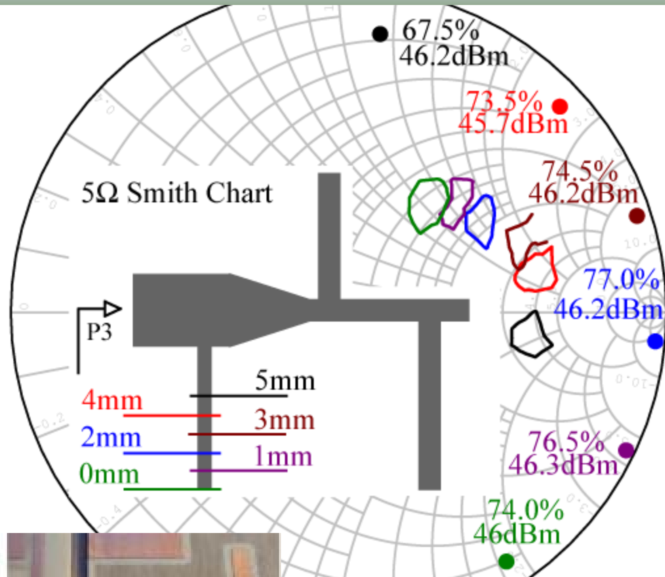
$$PAE = \frac{P_{out} - P_{in}}{P_{dd}}$$

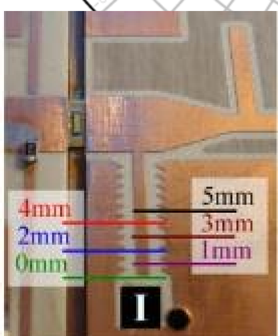
$$\eta_d = \frac{P_{out}}{P_{dd}}$$

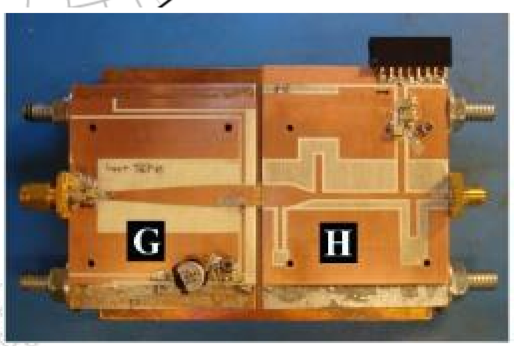


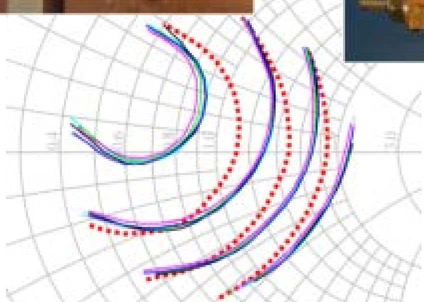
- Transistor power dissipation dominates
  - Reduced conduction angle
  - Avoids v_{ds}-i_{ds} overlap, power dissipation
- Waveform shaping (e.g. class F)
  - Voltage squaring, current peaking
  - 2nd harmonic short allows $2f_o$ current
  - 3rd harmonic open allows $3f_o$ voltage

Effects of 2nd and 3rd harmonic

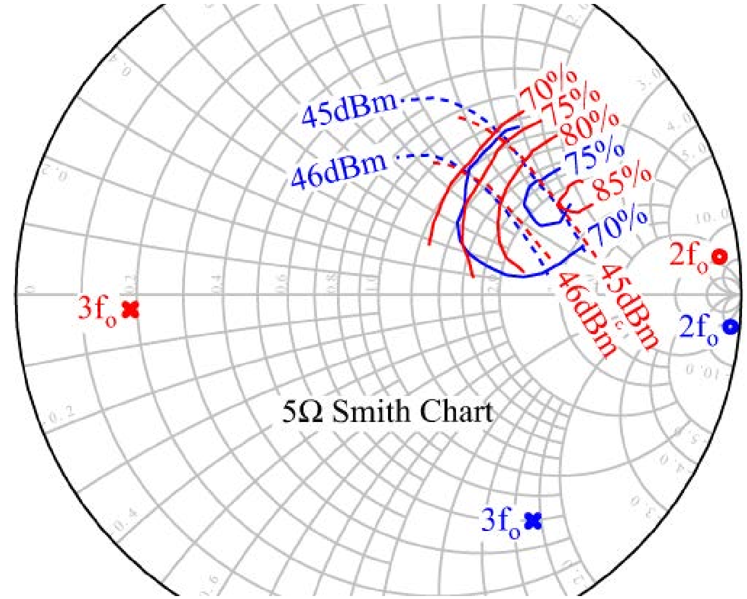








Consistent small-signal gain contours indicate that correct S-parameters were correctly de-embedded from load pull data after each cut.



2nd harmonic and 2nd/3rd harmonic load pull for the TGF2023-10 GaN HEMT in chip/wire configuration biased at 28V drain voltage and with 300mA quiescent current.

	2nd Harmonic	2nd/3rd Harmonic
Output Power	31.6W	31.6W
Drain Efficiency	77%	85%
Power Consumed	41.0W	37.2W
Power Dissipated	9.4W	5.6W

Outline

- Overview of approaches for improving efficiency at power back-off
- **Supply modulation**
  - GaN PA design (10GHz carrier)
  - Supply modulator (100MHz switching)
  - Integration and modeling
- Outphasing
  - Quasi-MMIC isolated and non-isolated
  - Measurements of load modulation internal to the PA
  - Outphasing with supply modulation
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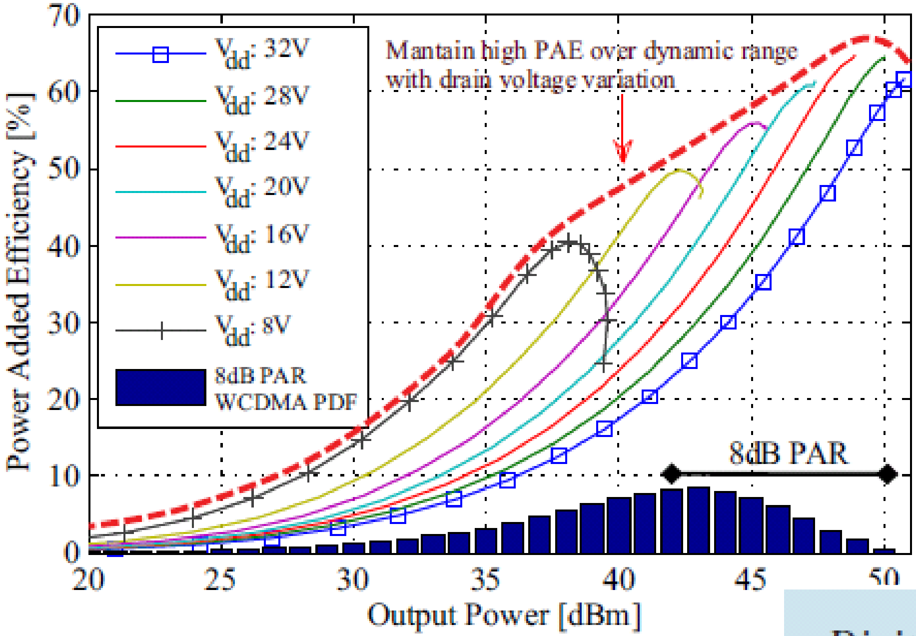
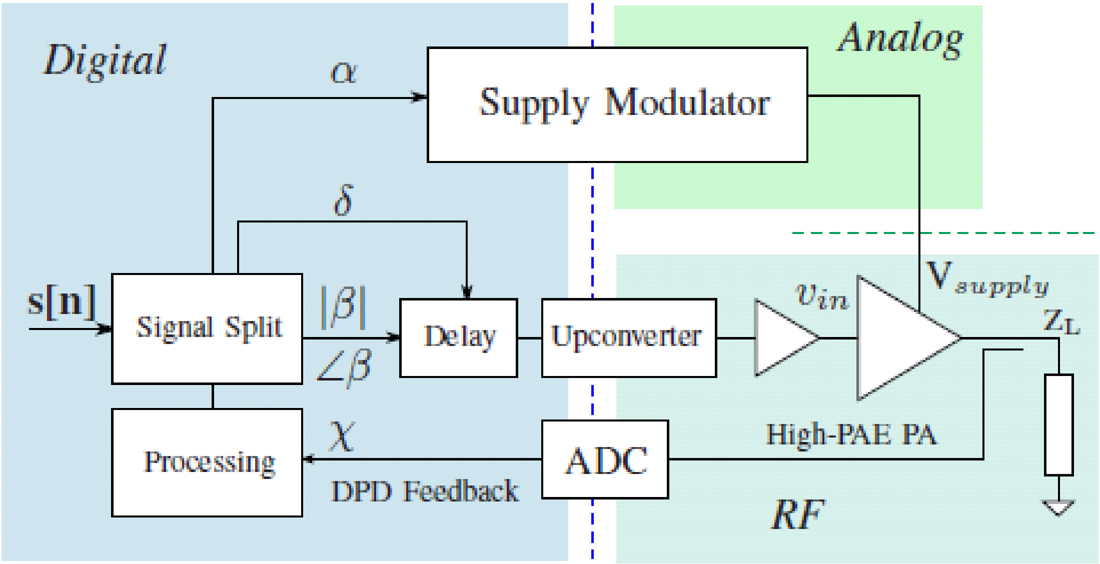
Supply-Modulated Transmitters



$$\text{PAE} = \frac{\int_0^{V_{max}} f_{PDF}(V) \cdot [P_{out}(V) - P_{in}(V)]\, dV}{\int_0^{V_{max}} f_{PDF}(V) \cdot P_{DC}(V) dV}$$

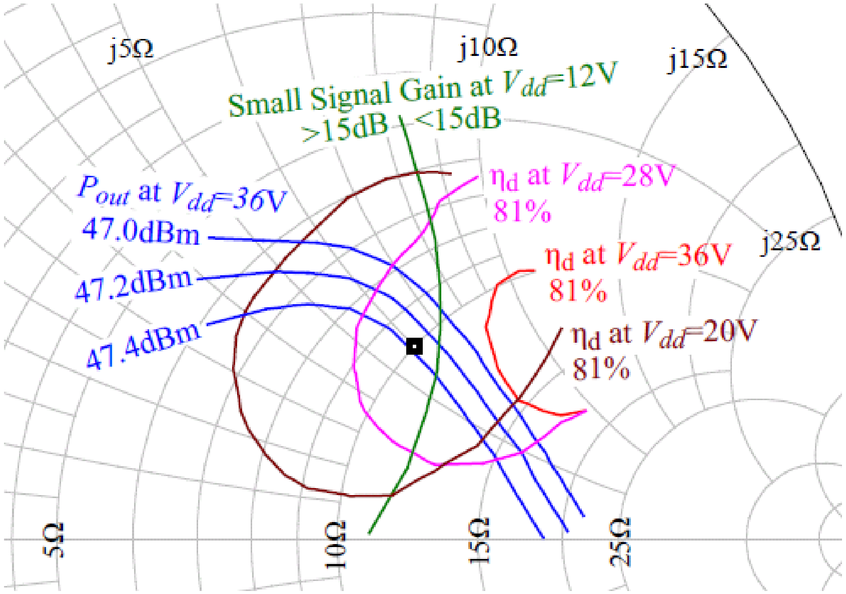


Components of SM-PA design

- **High-efficiency PA (e.g. harmonically-tuned)**
  - Improve maximum PA efficiency at a chosen power level with sufficient bandwidth for broadband signals
- **Efficient Supply Modulator**
  - Maintain PA efficiency at average power by varying the drain supply voltage
  - Enable high slew rates for tracking broadband signals
  - Introduce minimal reduction in overall efficiency
- **Linearization**
  - Restore linearity by identifying sources of distortion to simplify DPD
- **Integration and packaging**
  - Integrate supply modulator with PA with minimal loading
  - Thermal management
  - Integration of various drivers

High-Efficiency PA Design for SM

- PA design has to take into account:
  - small signal gain
  - efficiency and
  - output power over a range of supply voltages corresponding to an input envelope range
- Use **TriQuint 0.15um GaN:**
  - 20V CW
  - 100um SiC substrate
  - 60um diameter vias
  - 240, 300 and 1200 pF/mm^2
  - 50Ω/sq TaN resistors

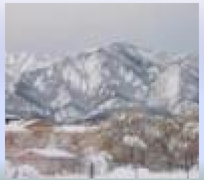


Parameter	Condition	Typical
IMAX	Vds = 20 V	1.15 A/mm
Peak Gm	Vds = 20 V	380 mS/mm
Vp	Ids = 1 mA/mm	-3.5 V
BVGD	Ig < 1mA/mm	50 V
Ft	20V-200mA/mm	38 GHz
FMAX	20V-200mA/mm	140 GHz

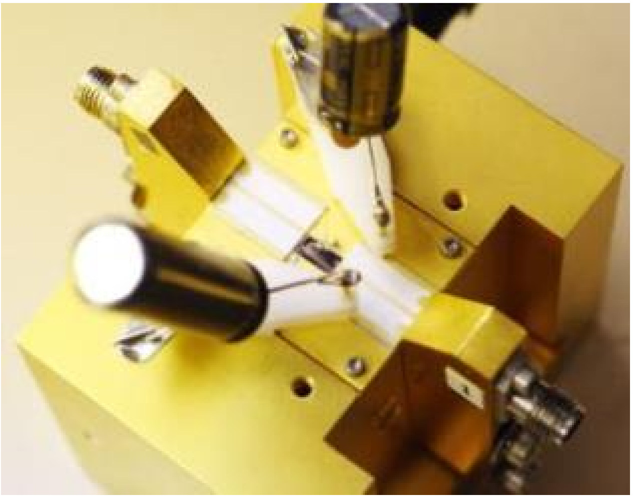
- Modeling:
  - Fit class Ab/B over a range of Vds
  - Pulsed IV at 25 and 85 deg C
  - S-parameters at 5, 10, 15, 20 V for Idq=10 and 100mA/mm

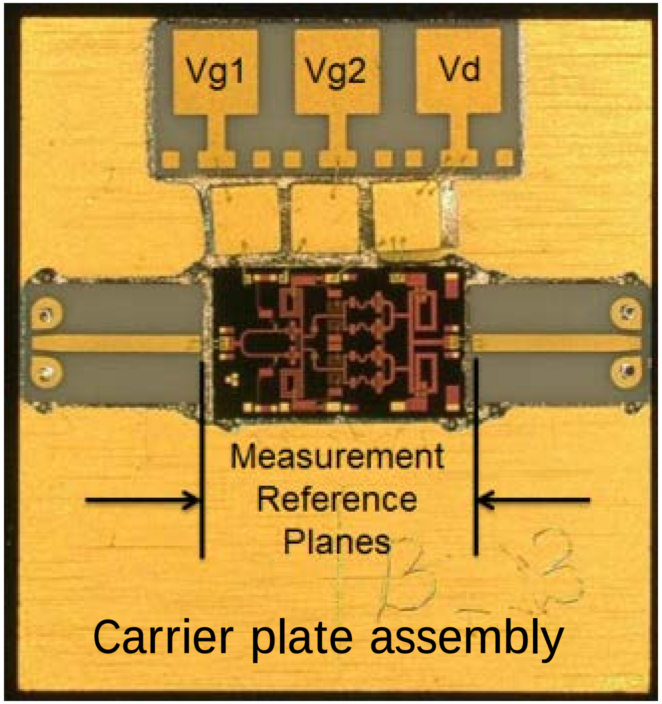
Load pull PAE and power tuned at Vd=20V

High-Efficiency X-band MMIC PAs



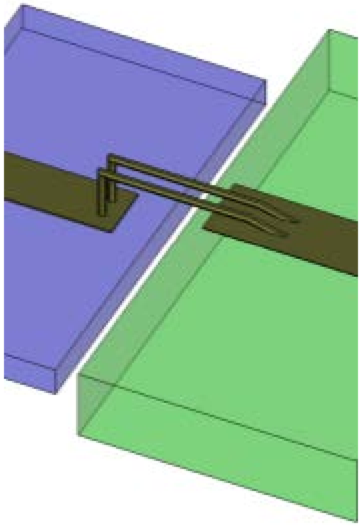
Fixture

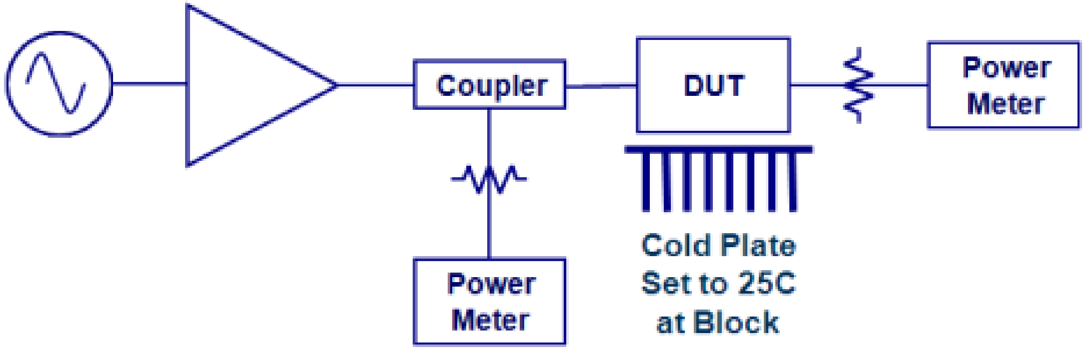


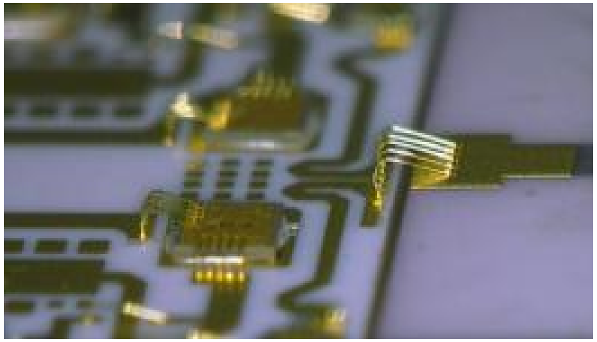


Carrier plate assembly

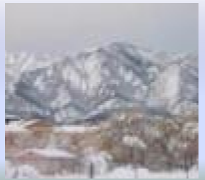
EM models for bondwires included in MMIC design

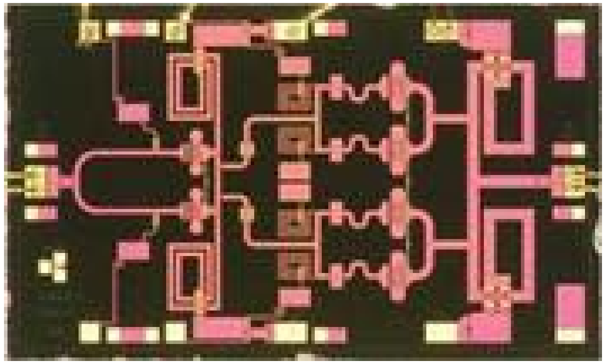






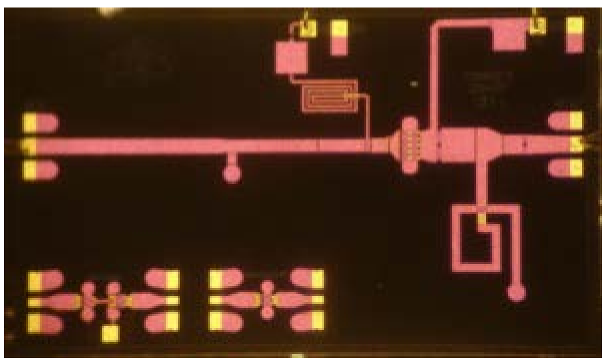
Example X-band MMICs





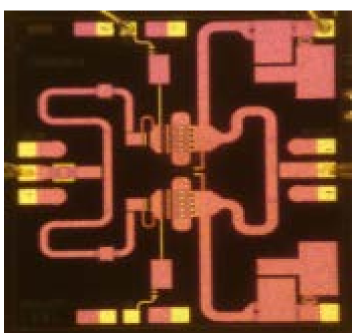
Circuit B:

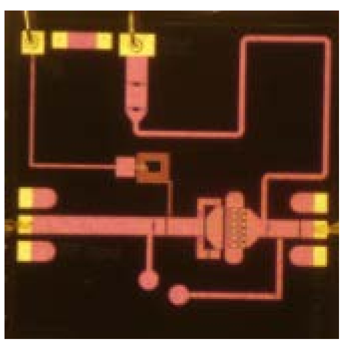
2-Stage MMIC, combi
four 10x90um.
3.8mmx2.3mm



Circuit F

Single stage, two
10x100um
2.0mmx2.3mm



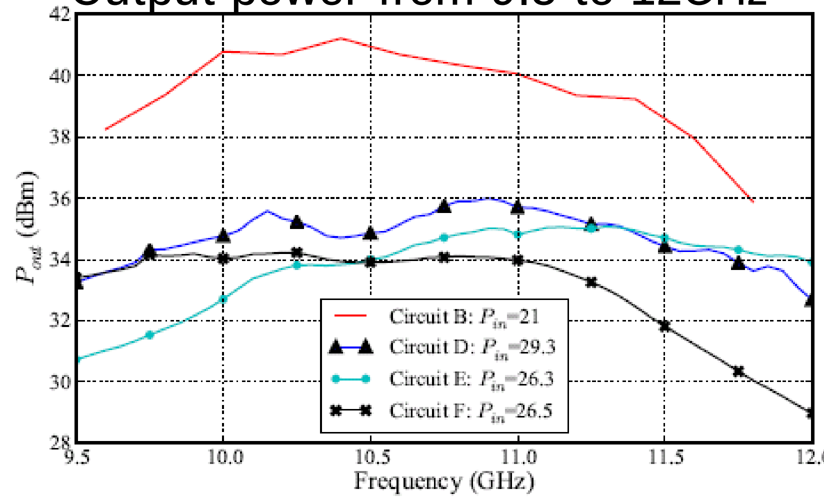


Circuits D/ E

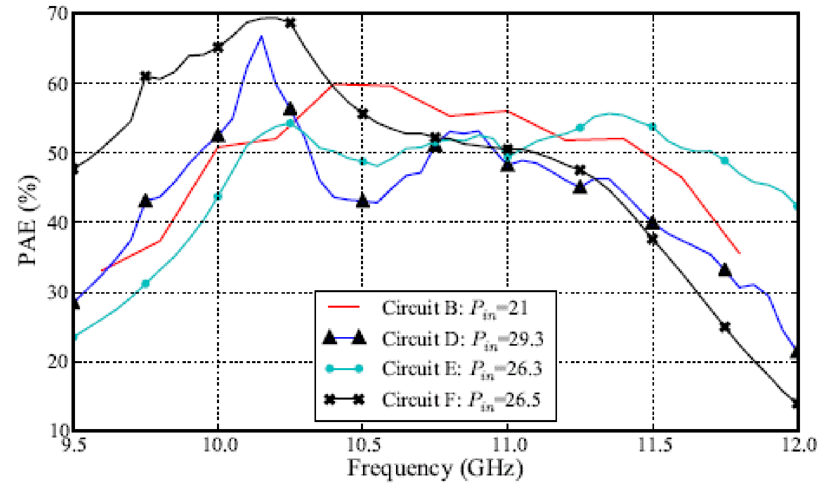
Single stage,
10x100um
3.8mmx2.3mm

and
12x100um
2.0mmx2.3mm

Output power from 9.5 to 12GHz

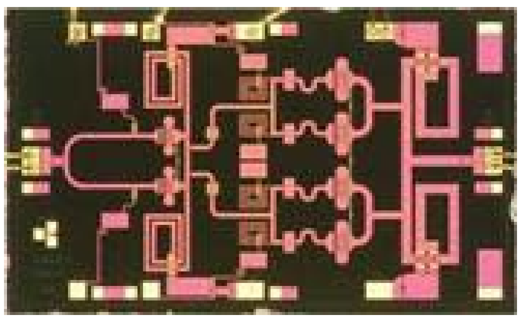


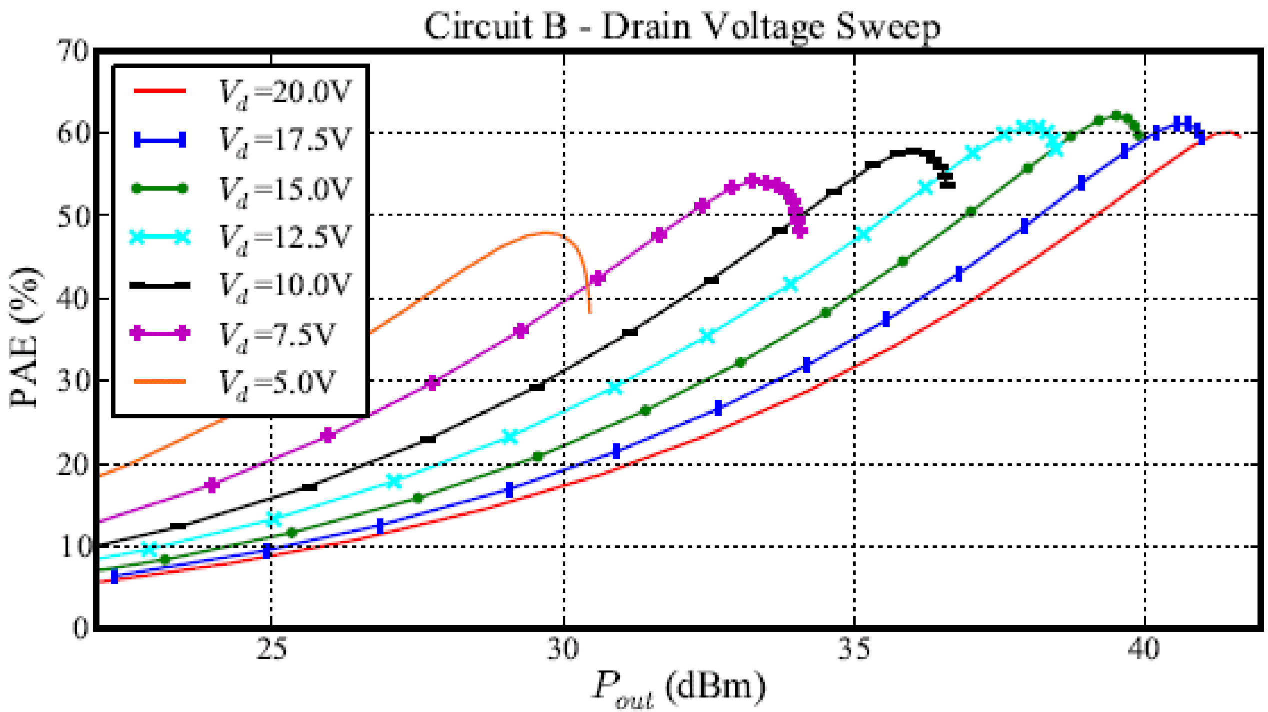
PAE from 9.5 to 12GHz



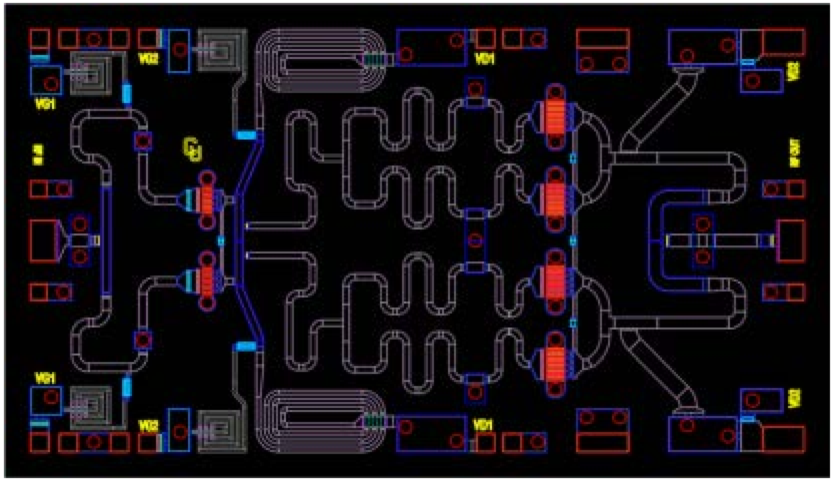
X-band MMICs for SM

Circuit	B	D	E	F
Max PAE (%)	59.9	66.8	55.7	69.4
Max P_{out} (W)	13.2	3.98	3.22	2.64
Gate size (mm)	3.6	2.0	1.2	1.0
W/mm	3.68	1.99	2.69	2.64
BW at PAE=45% (GHz)	1.6	0.77	1.88	1.95
ΔP_{out} (dB) / ΔV_{ds} (V)	11/12.5	3.3/7	4.8/9	5.3/8

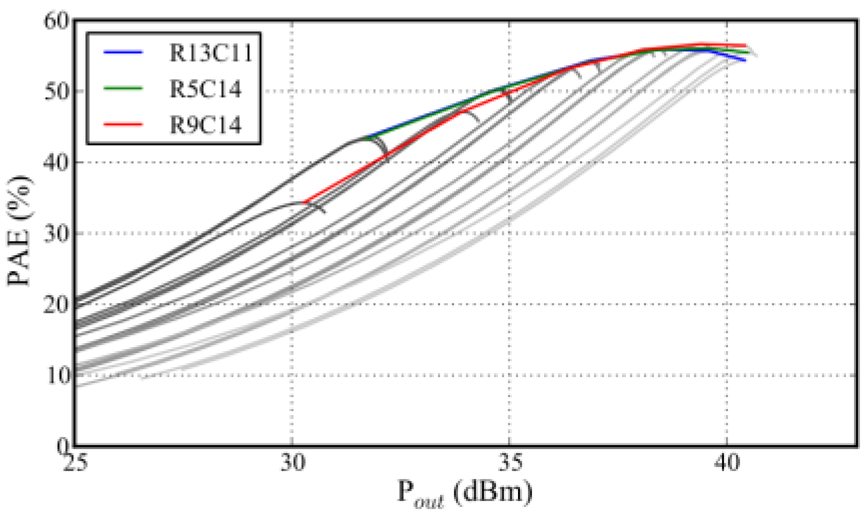


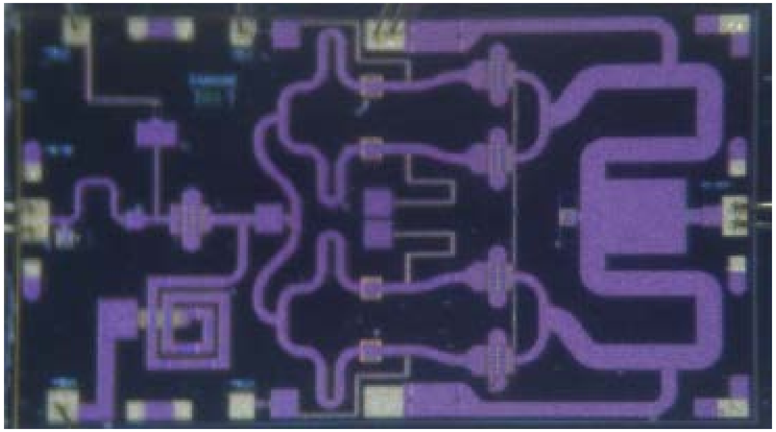


Some other MMIC PAs for SM

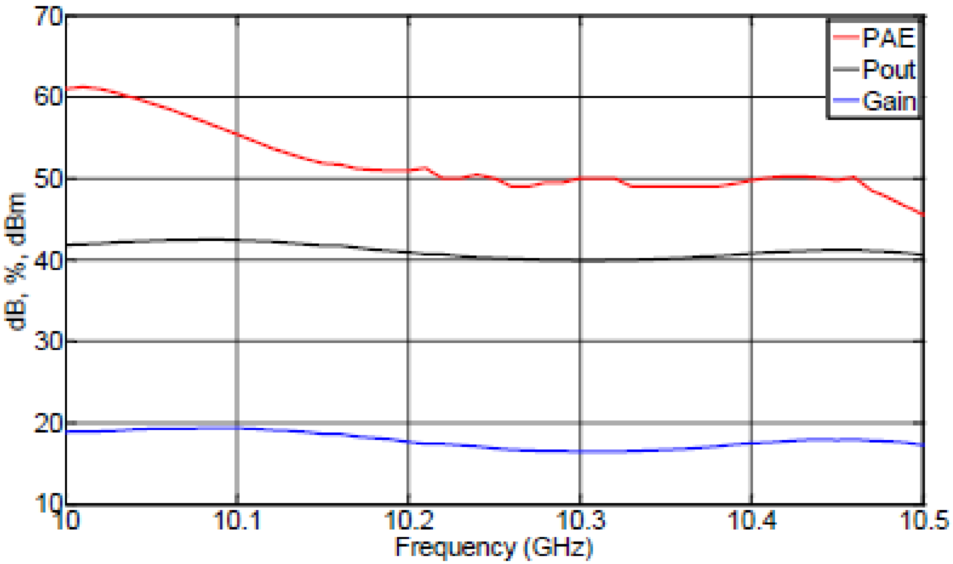


Run 2, >10W, more linear





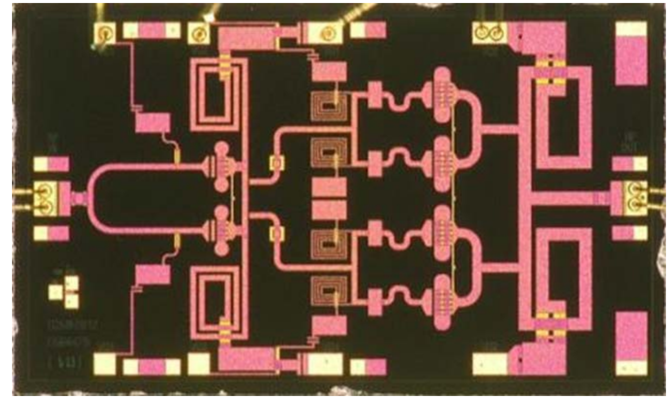
>13W, >60%, G=20dB

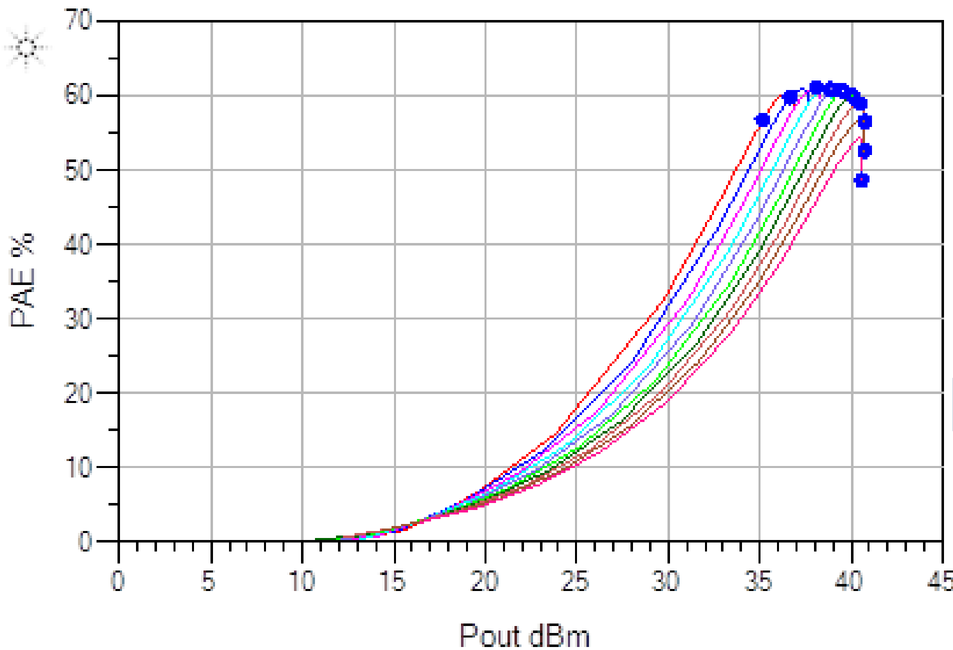


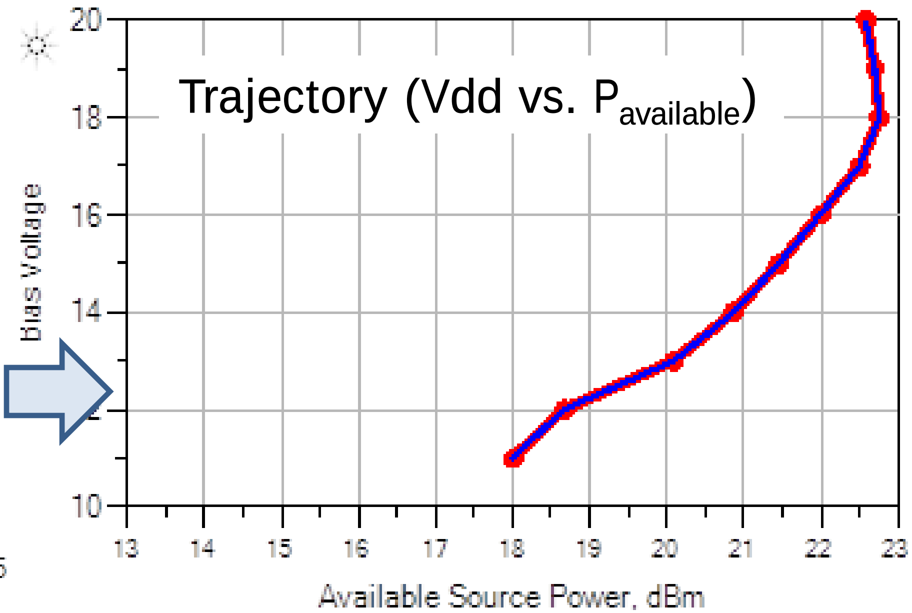
Real signal, integrated transmitter

- G = 18dB (constant)
- Both stages supply-modulated
- For reasonable AM/AM, 11V of voltage dynamic of the drain supply
- At low Vdd, gain drops
- Increasing gate bias voltage may improve the achievable dynamic range

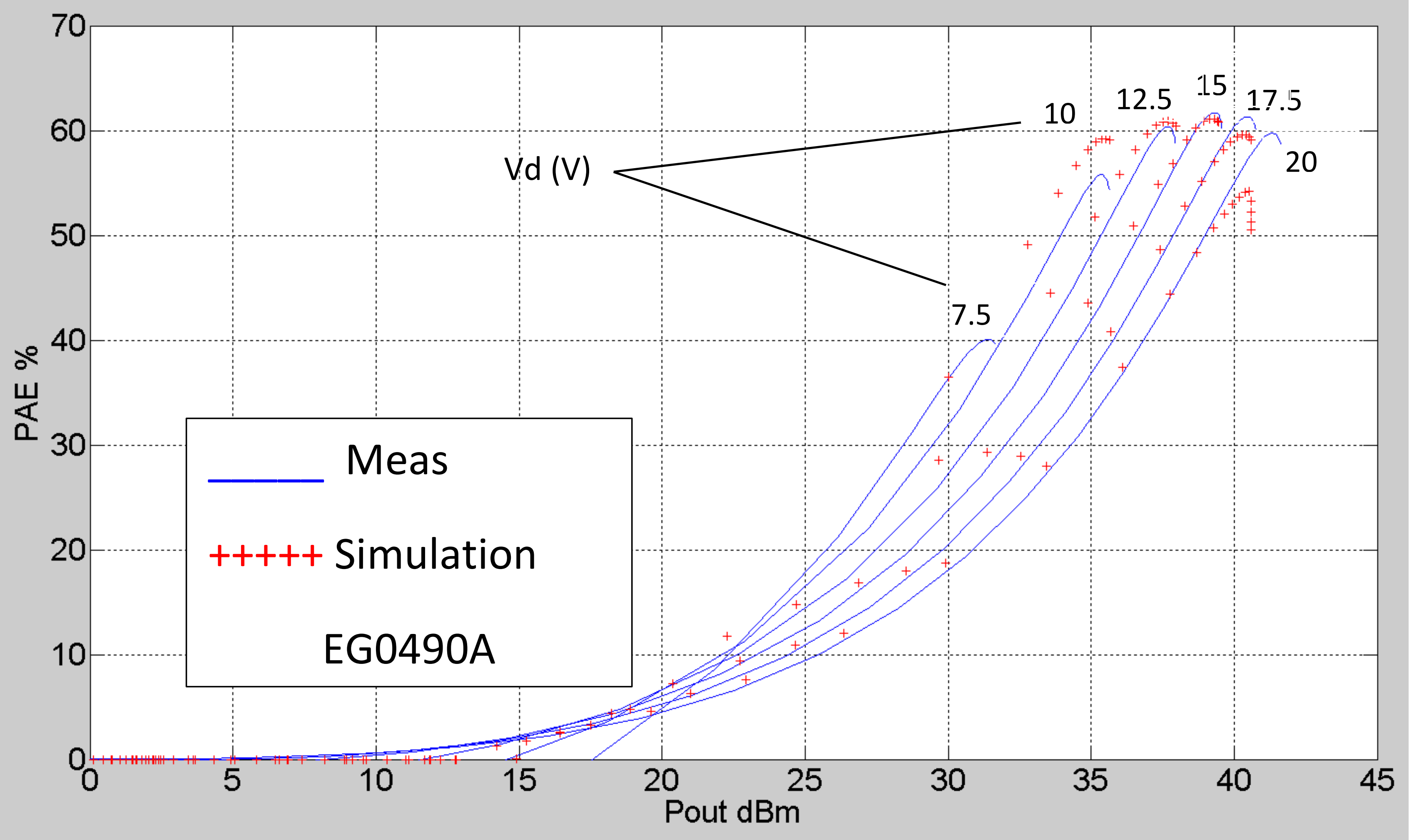
PA MMIC EG0490A, two stages, 10W





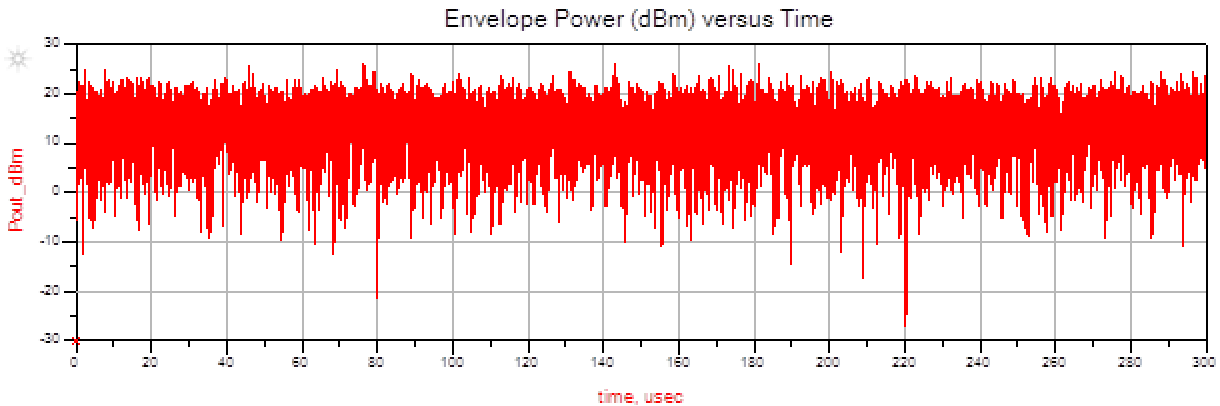


Measured vs. simulated static PA



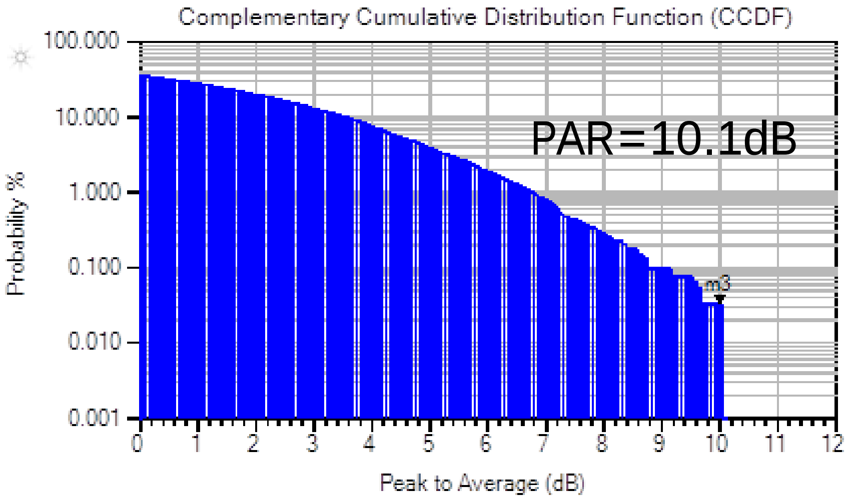
Signal characteristics

Example: LTE 18MHz 3GPP standard signal, envelope transient simulation

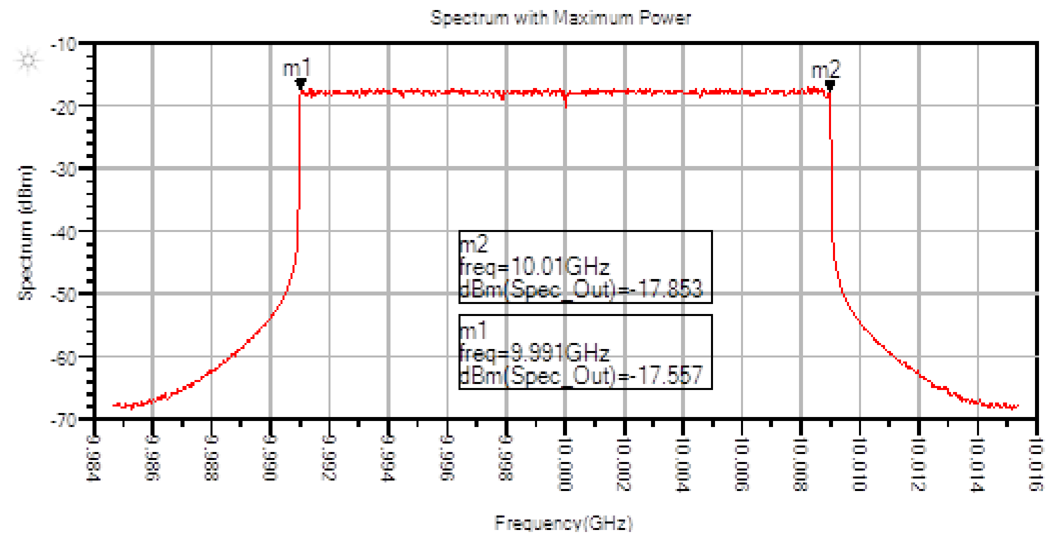


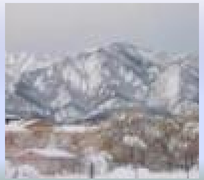
Envelope in time domain
Average power 16dBm

CCDF

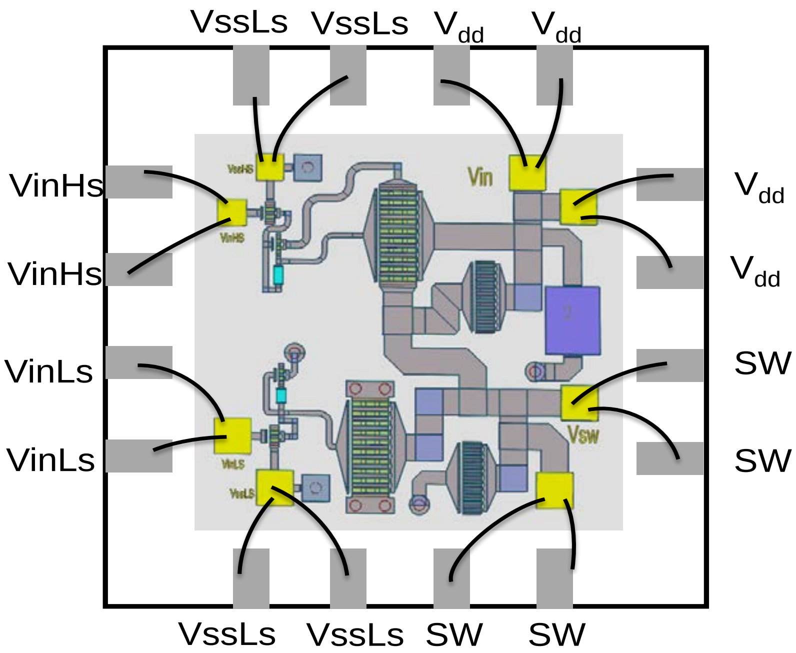


Spectrum





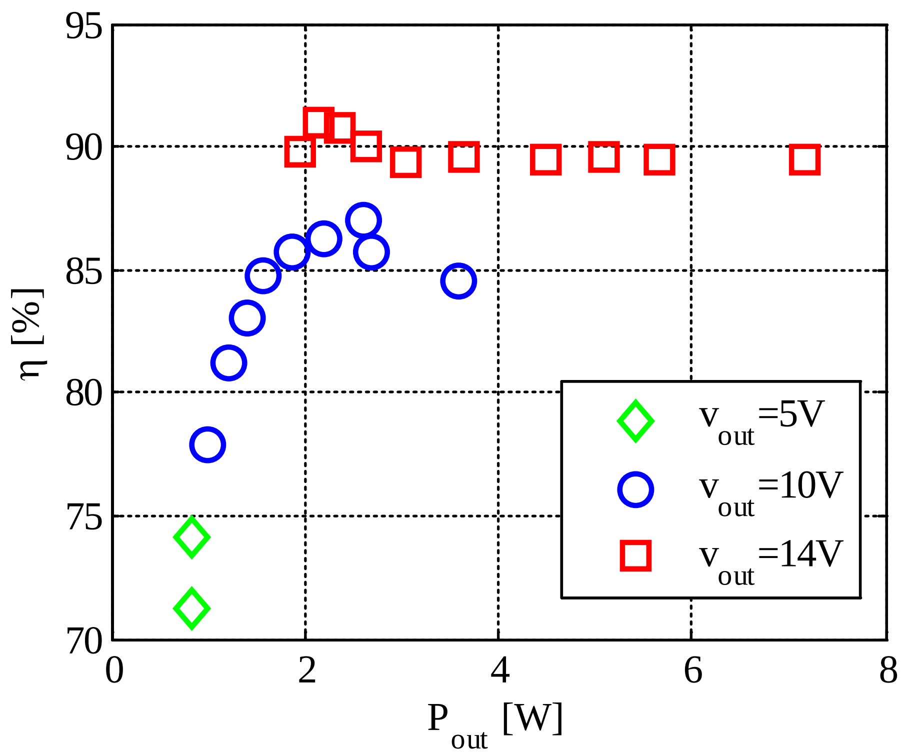
GaN supply modulator



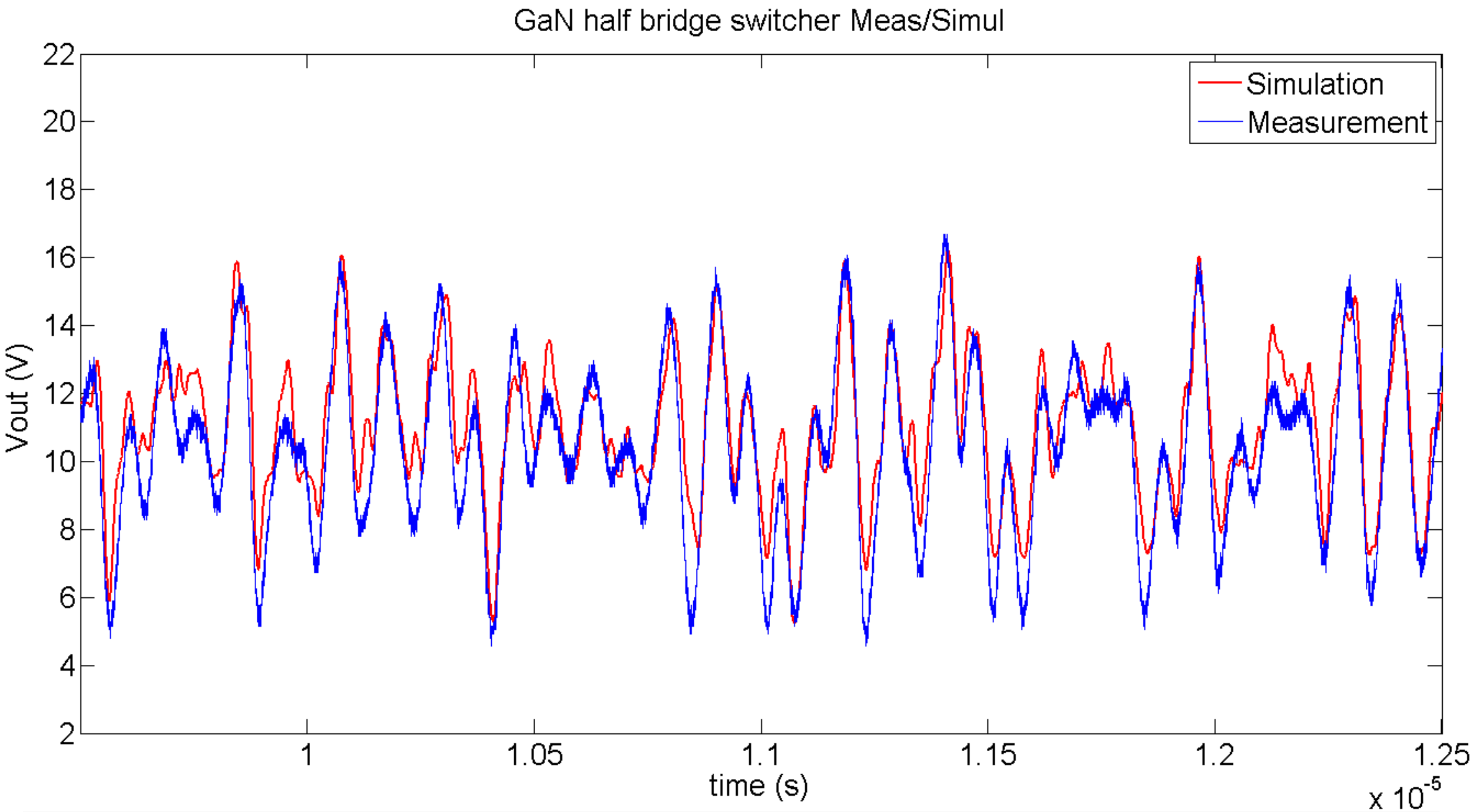
150-nm GaCN on SiC MMIC
Standard QFN package
10W at 20V, 100MHz switching

The switching converter operates as expected, showing an output voltage waveform ranging from 0V to 19V

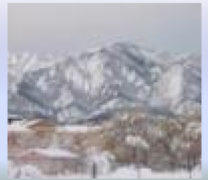
The high state of the PWM signal does not reach 20V because of the on resistance of the transistor.



Measured vs. simulated DSM

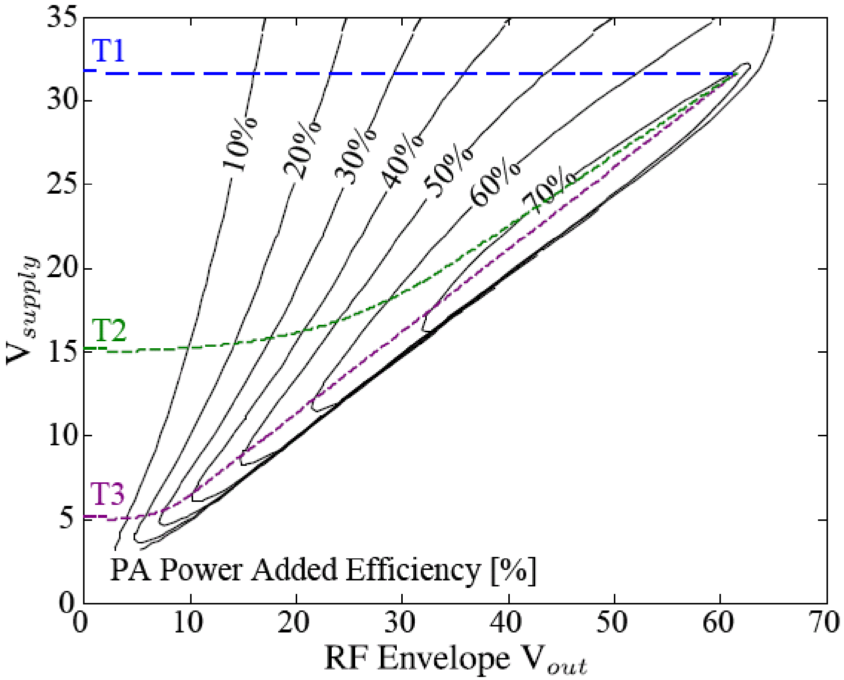


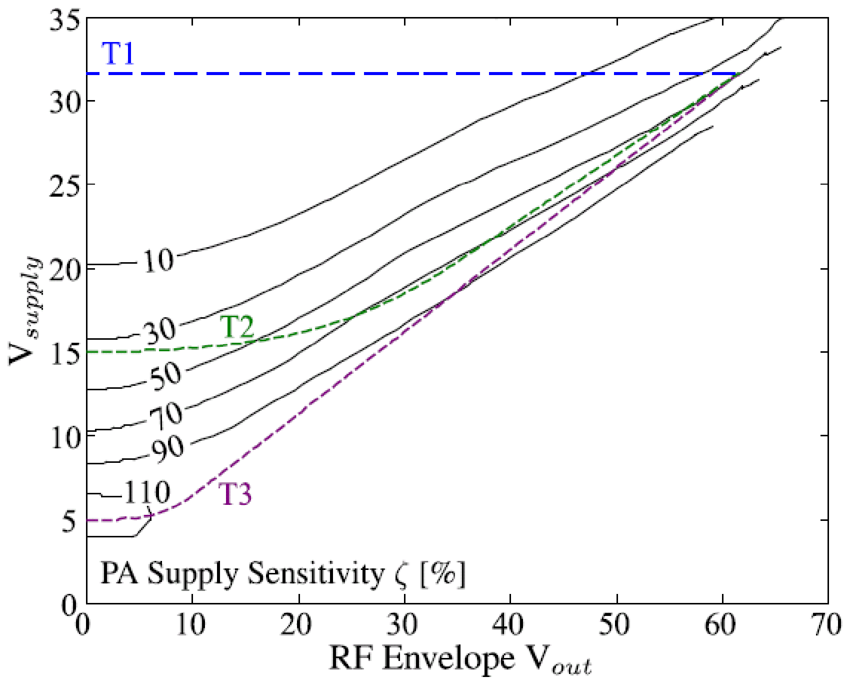
$$RMS\ error = 100 \times \sqrt{\frac{\sum_{t=1}^{n}\left(V_{out,t} - V_{in,t}\right)^2}{n}} \times \frac{1}{\left(V_{out\_max} - V_{out\_min}\right)} = \mathbf{4.5\%}$$



Issues for SM-PA design

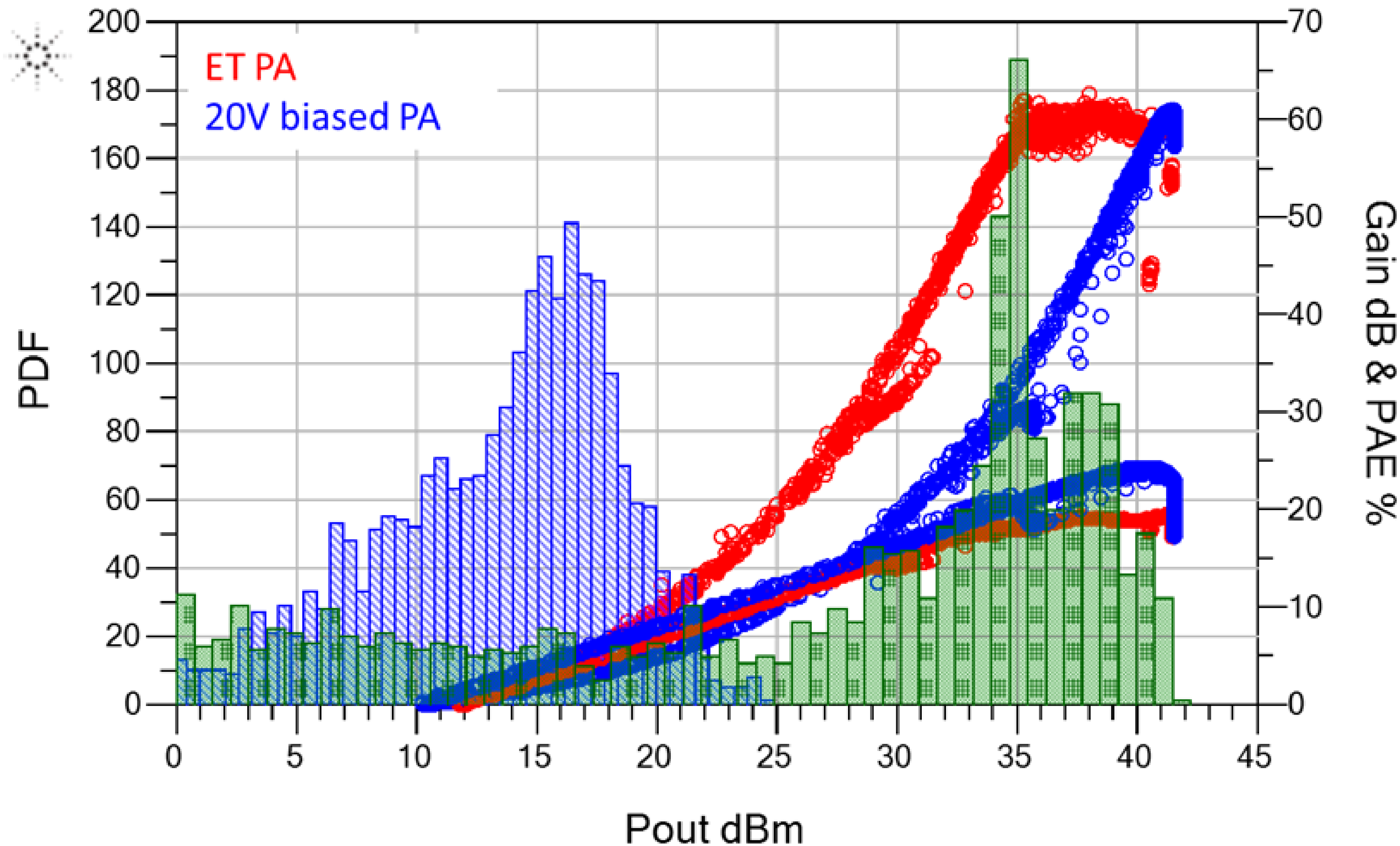
- PA Supply Sensitivity: $$\zeta = \frac{\frac{\Delta V_{out}}{V_{out}}}{\frac{\Delta V_{supply}}{V_{supply}}} \times 100\%$$



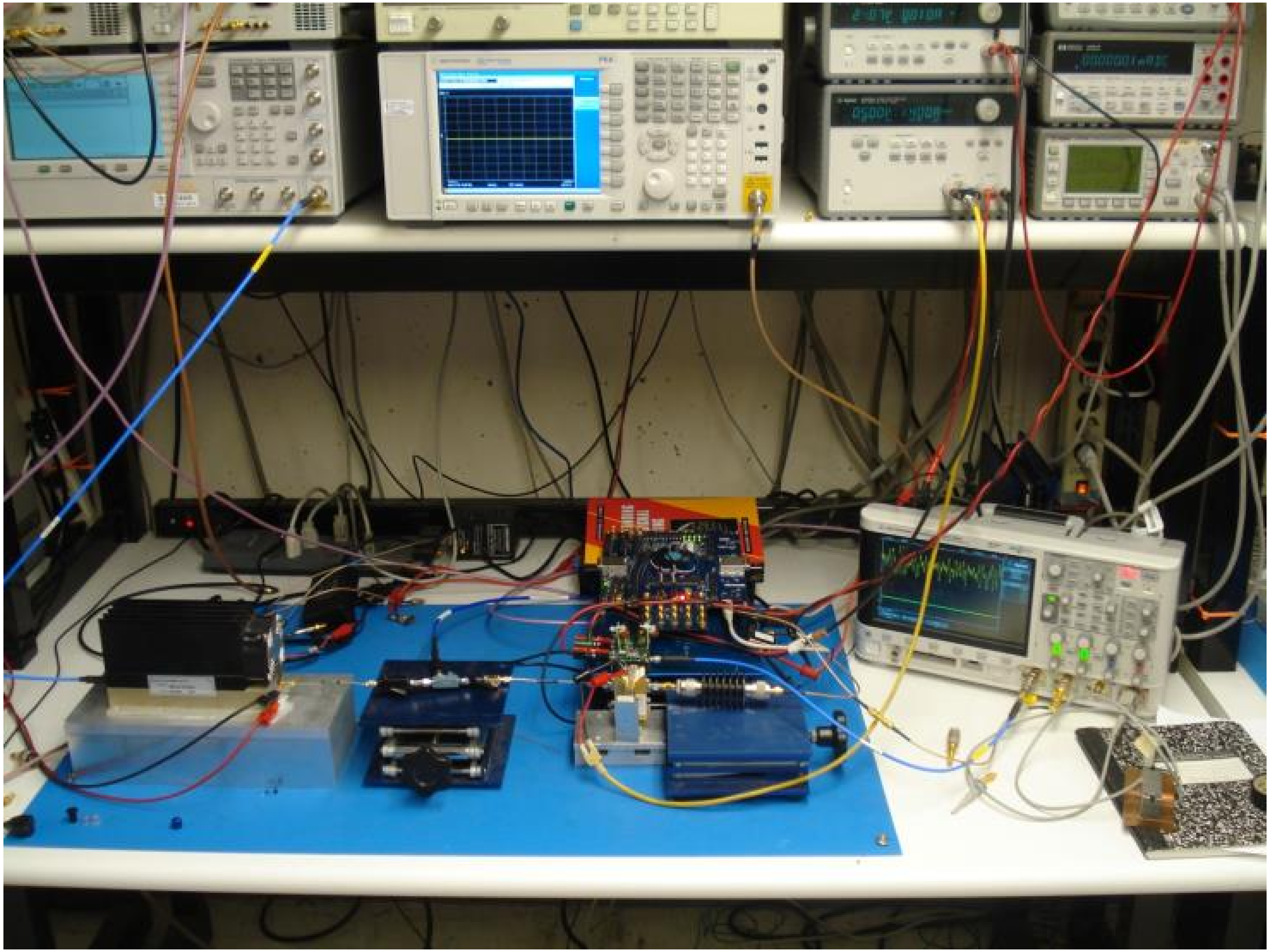


- High slew rate (envelope signal bandwidth)
- Dynamic drain complex impedance loads supply modulator

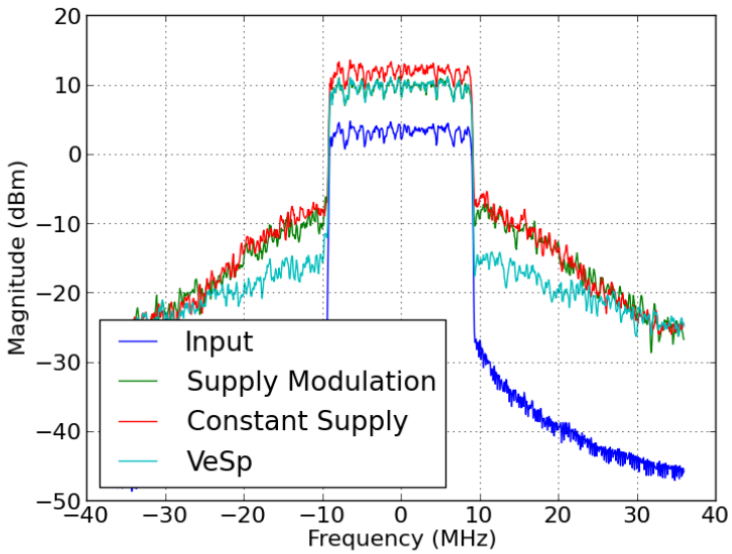
PA performance with LTE signal

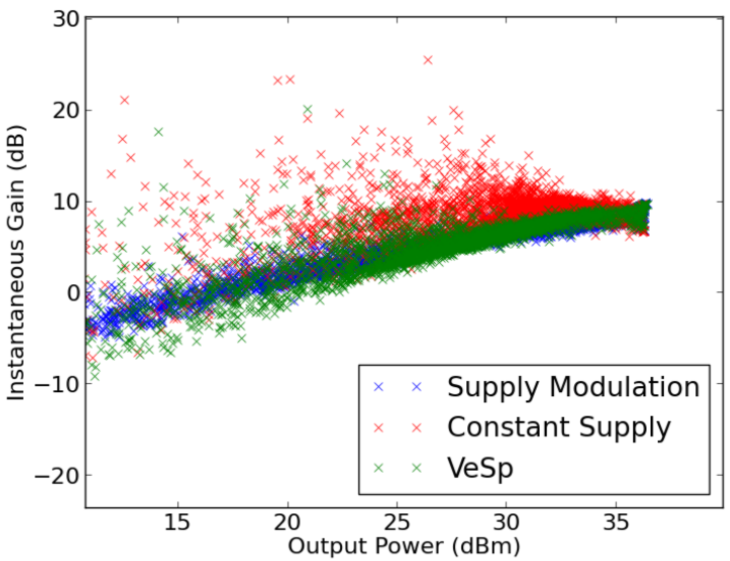


Test bench



Example measured results

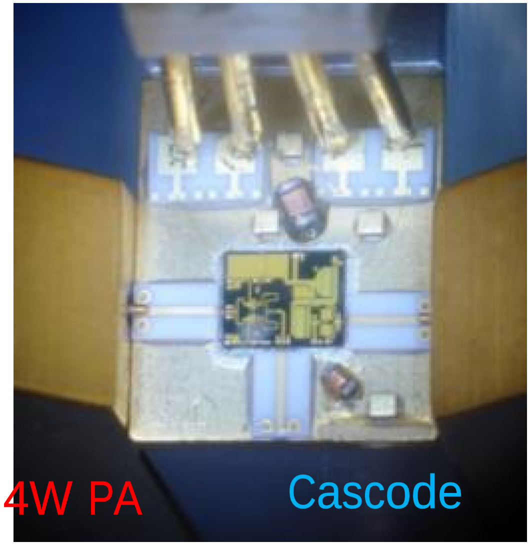


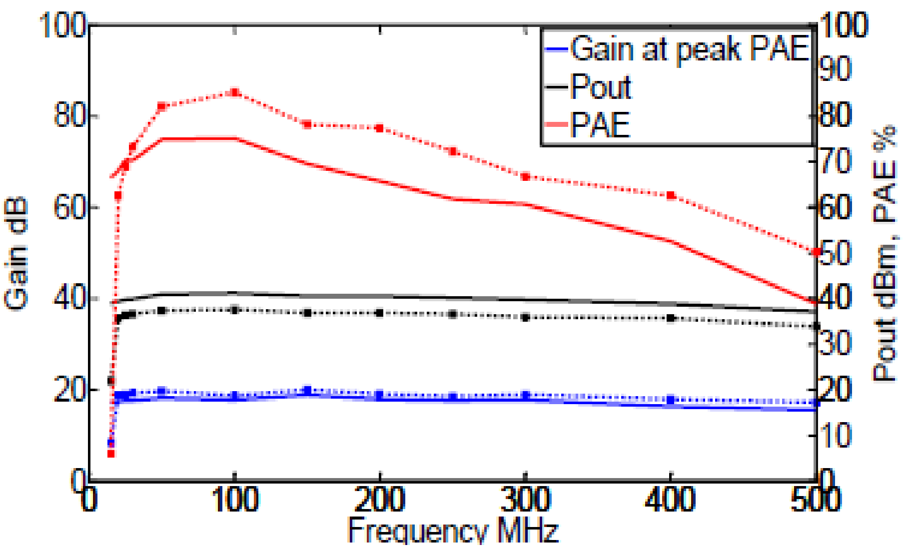


18MHz LTE
PAR=7.1dB

	Constant Supply	Modulated Supply	VeSP
Channel Power	30.6 dBm	28.6 dBm	28.5 dBm
Peak Power	36.3 dBm	36.5 dBm	36.5 dBm
CPAE	43.9%	65.4% (34.8%)	62.6% (33.1%)
Current	108.0 mA	75.6 mA	80.2 mA
ACPR	-27.1 dB	-23.3 dB	-28.0 dB
EVM	-31.2 dB	-29.3 dB	-29.3 dB

High-bandwidth SM-PAs

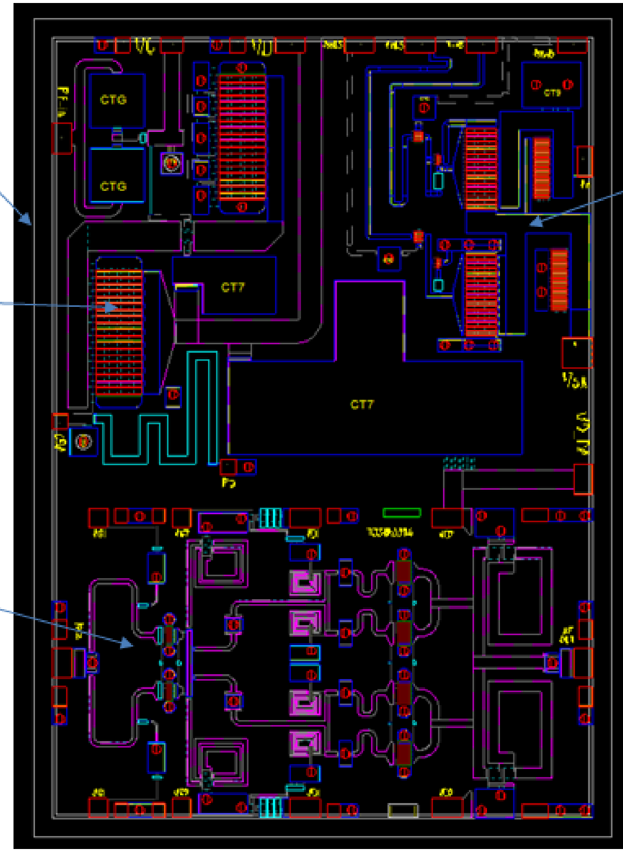




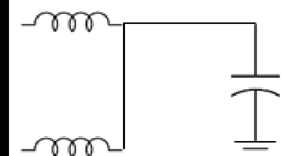
DC + RF pads

RF envelope input

Cascode VHF PA



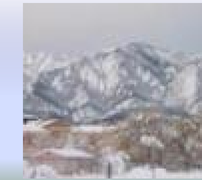
Single-phase half bridge converter



Off chip filtering

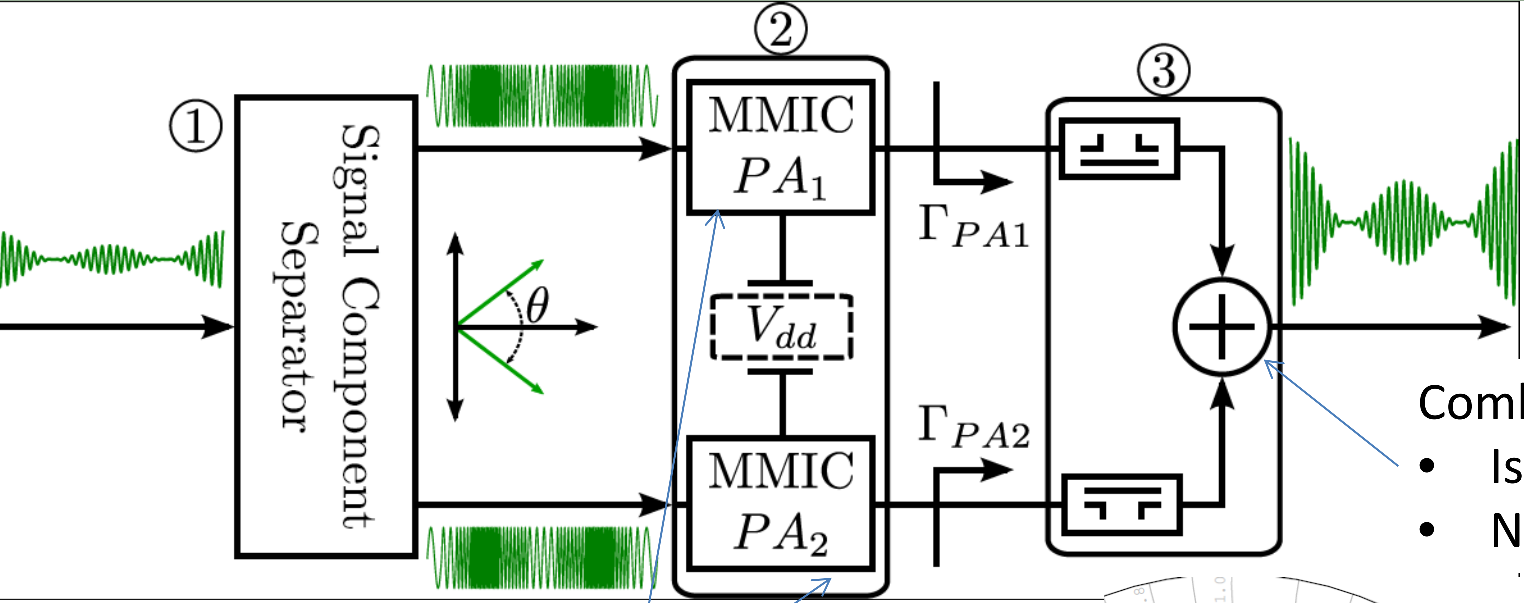
- **Higher band: 15-500MHz 80%-50%**
- **Lower band: 90% efficiency, >5W, 100 MHz switching**

Outline



- Overview of approaches for improving efficiency at power back-off
- Supply modulation
  - GaN PA design (10GHz carrier)
  - Supply modulator (100MHz switching)
  - Integration and modeling
- **Outphasing**
  - Quasi-MMIC isolated and non-isolated
  - Measurements of load modulation internal to the PA
  - Outphasing with supply modulation
- Discussion and some other challenges

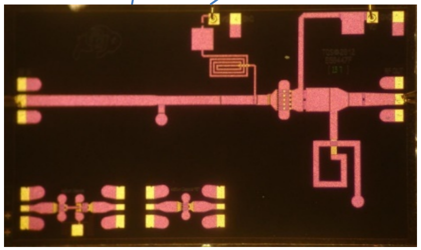
Quasi-MMIC outphasing PA

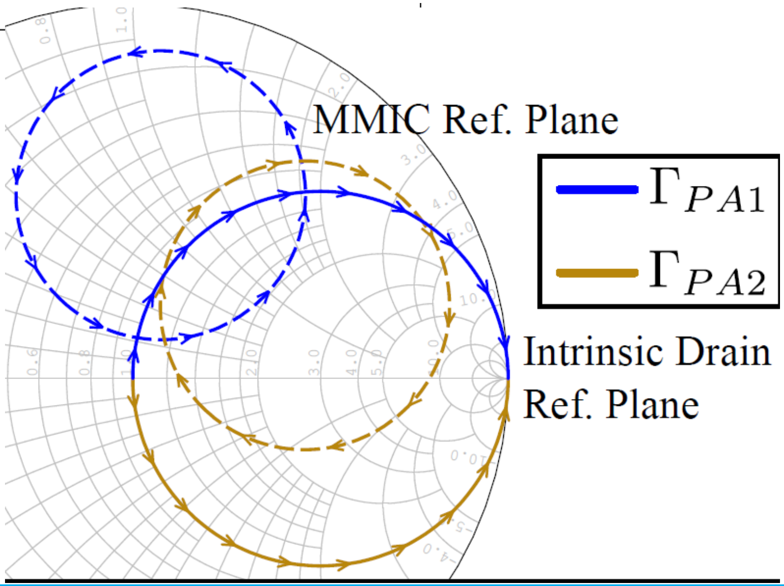


Combiner:

- Isolated
- Non-isolated

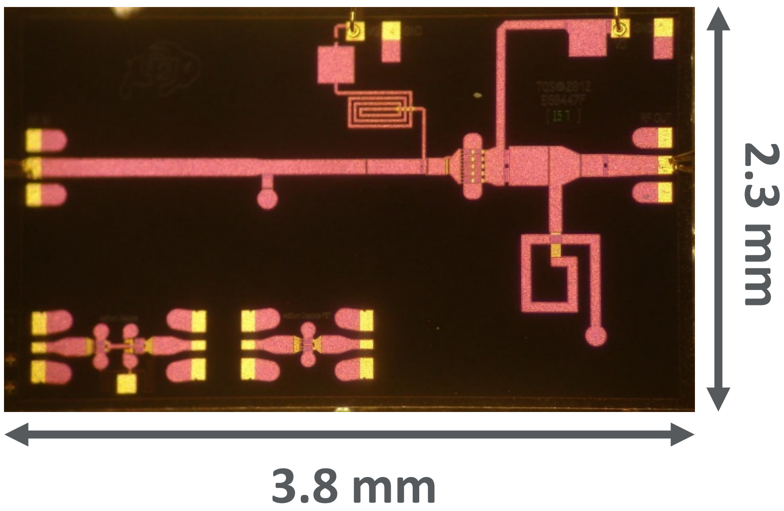
Digital

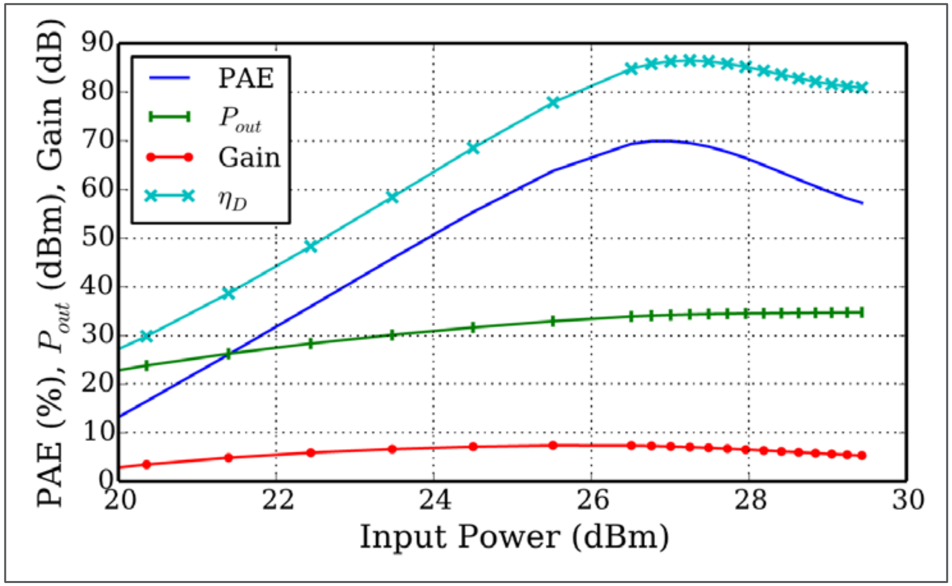




Load pull contours for non-isolated combiner

PA element for outphasing PAs

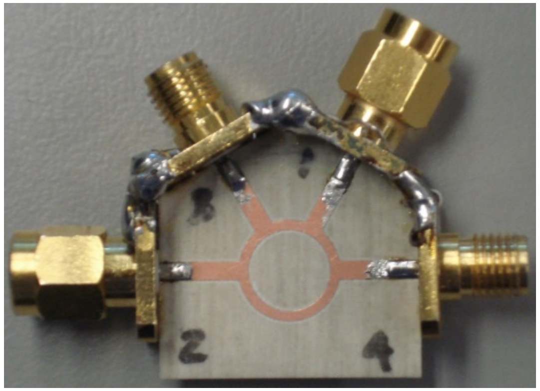




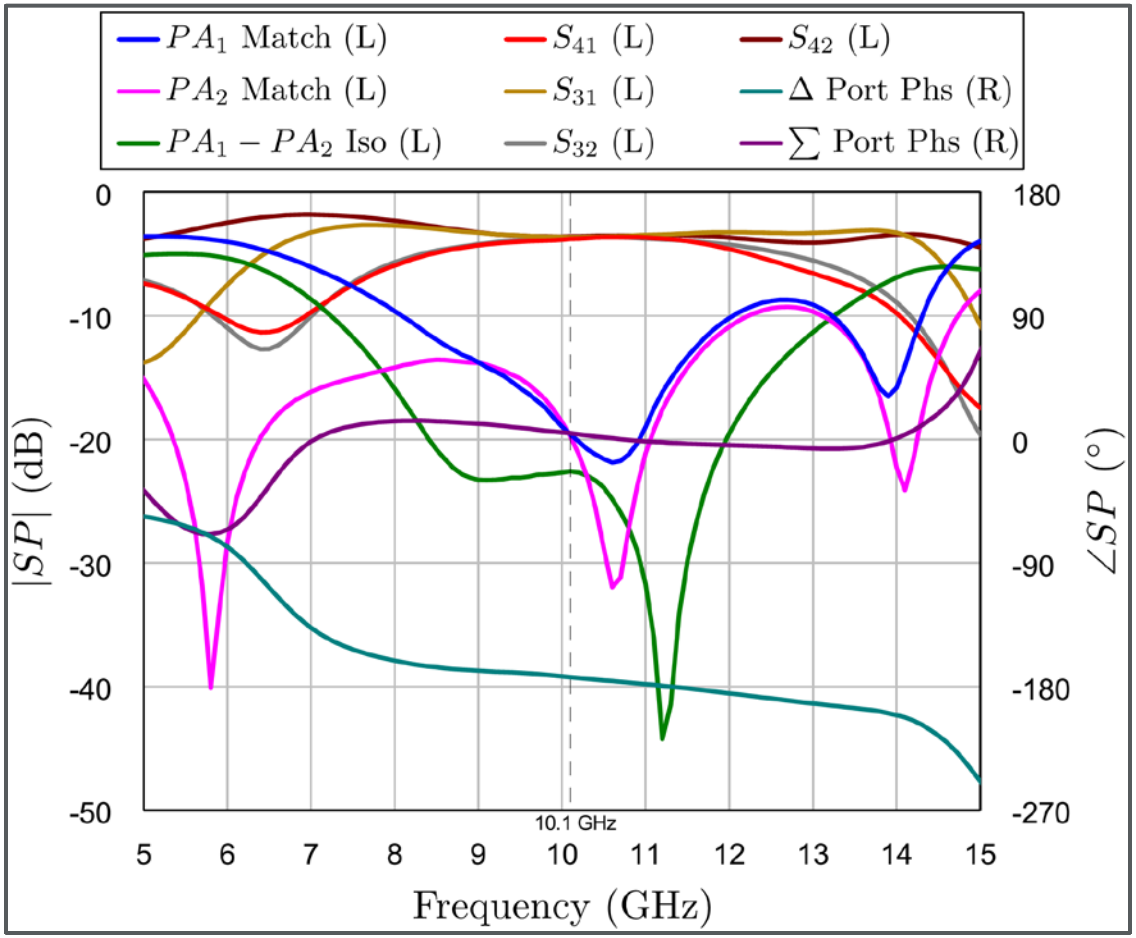
- Single-stage
- Biased in class-B
- GaN MMIC PA (TriQuint 0.15 µm)
- 10 x 100 µm FET

- V_{DD} = 20 V, V_G = -4.0 V
- f_0 = 10.1 GHz
- Peak PAE = 70%
- P_{out} = 2.7 W
- Gain = 7.2 dB

Isolated combiner

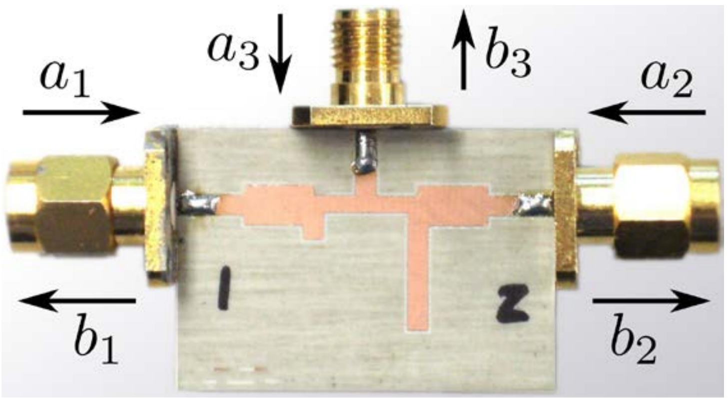


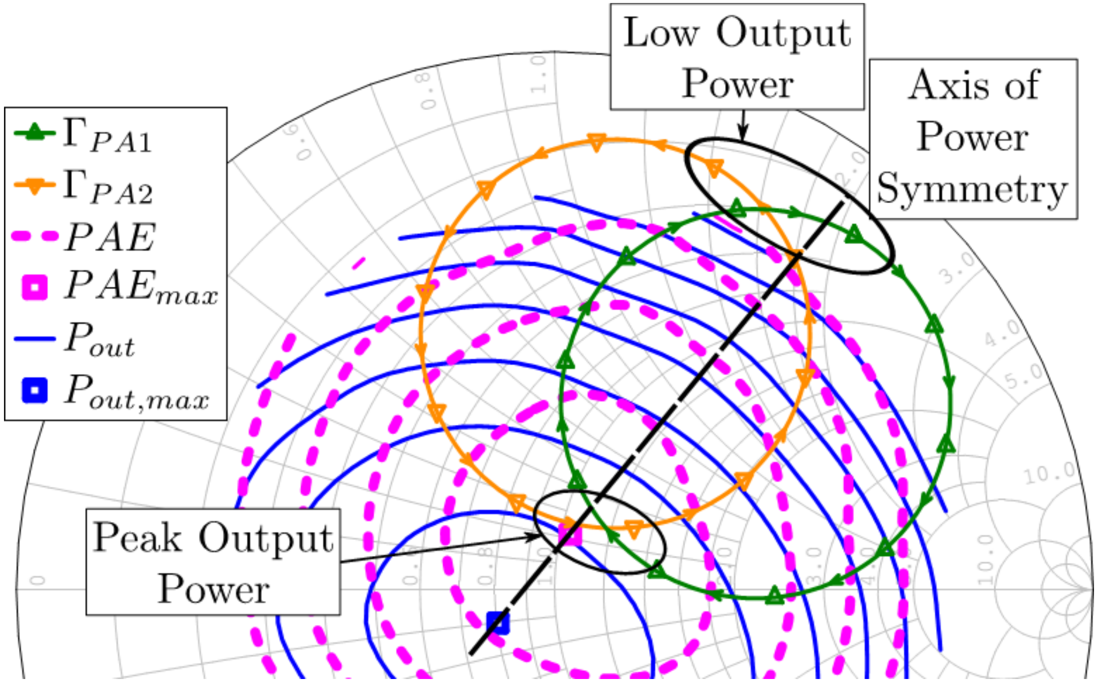
- 180° rat-race
- 30 mil Ro4350B
- < 1.4 dB loss
- 22.5 dB isolation
- > 19.5 dB return loss



- 4.5° sum port phase
- 173° diff port phase

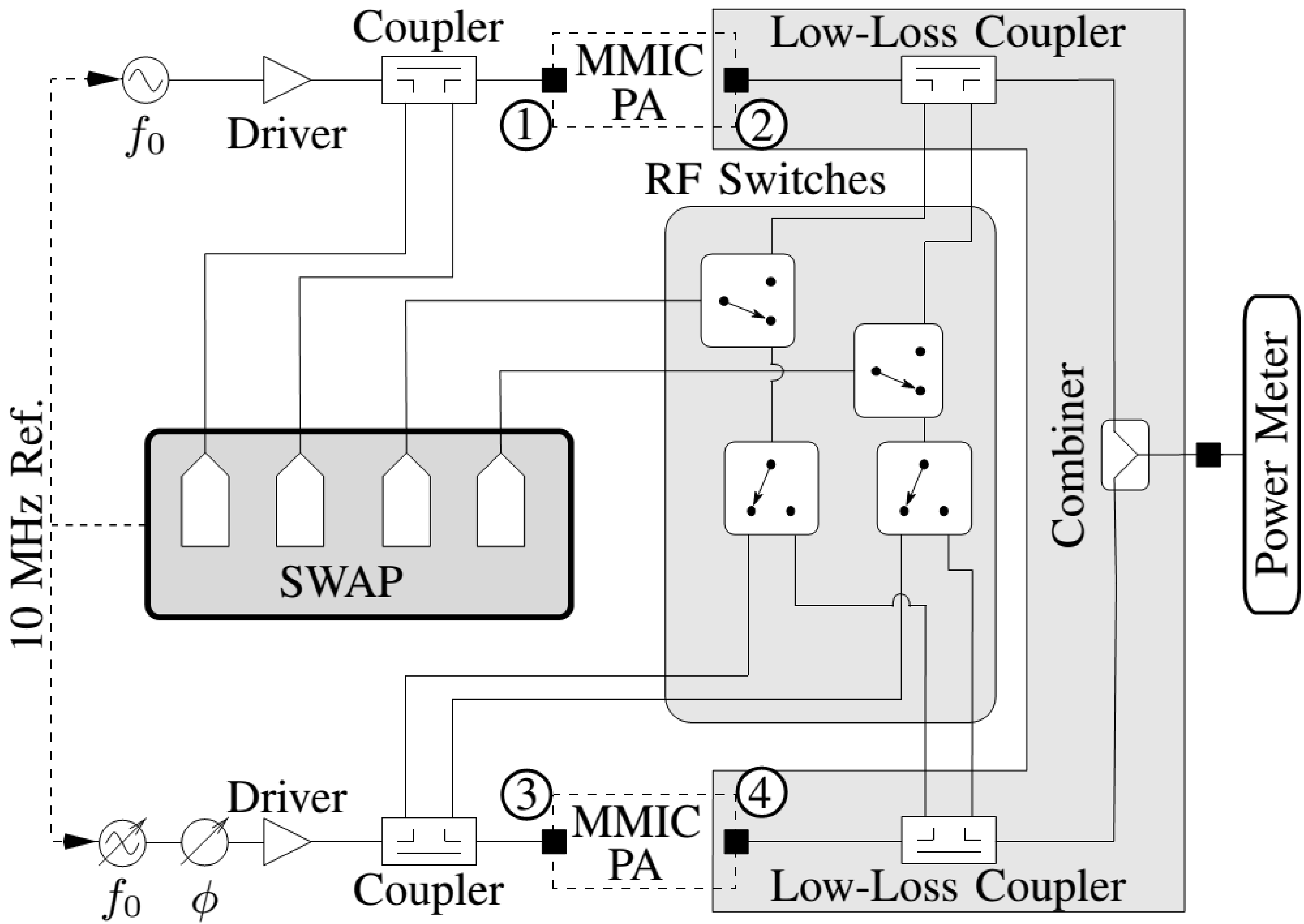
Non-isolated Combiner



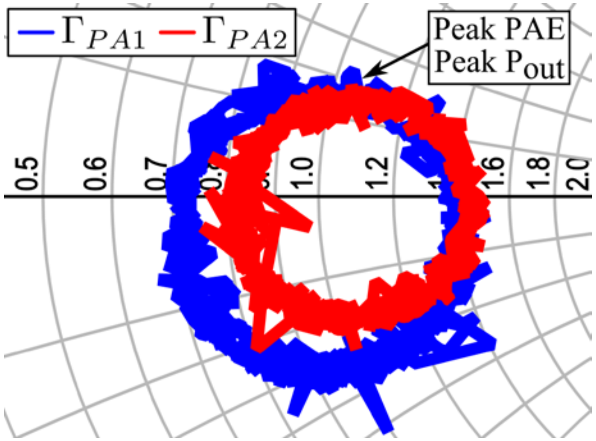


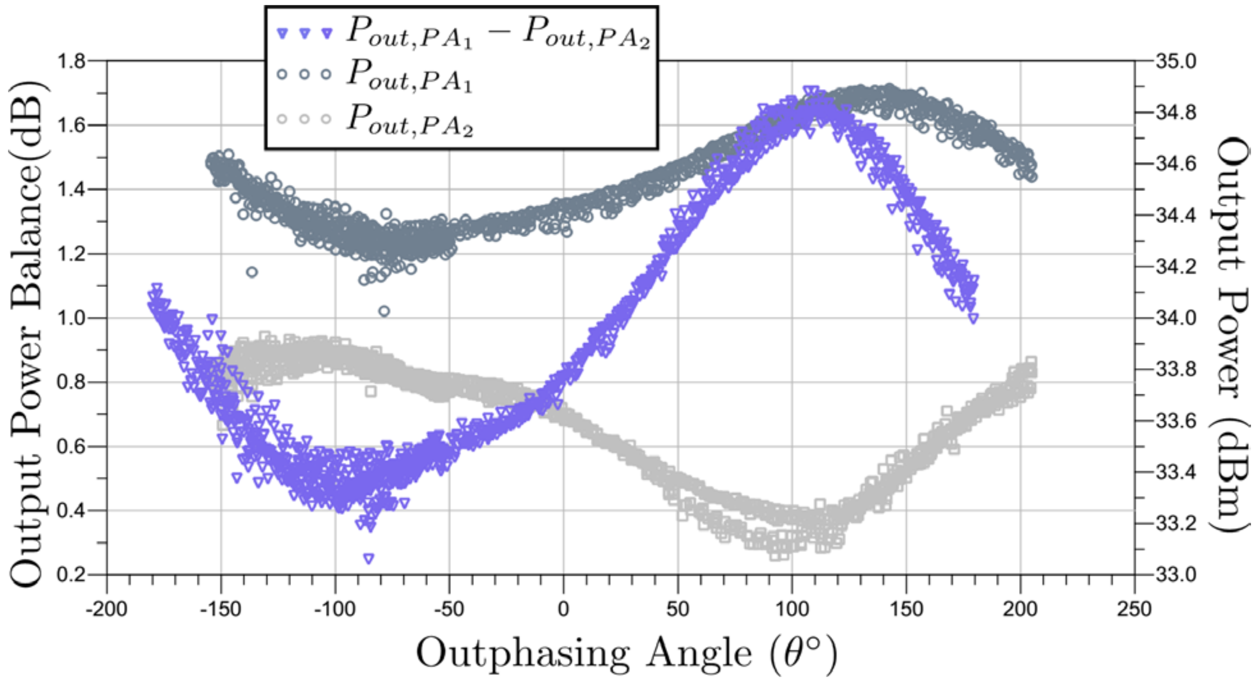
- Shunt susceptances and tuned 90° TLs
- Load modulation intersects at peak PAE load
- Internal PA power balance reasonably maintained

Internal PA Load Modulation



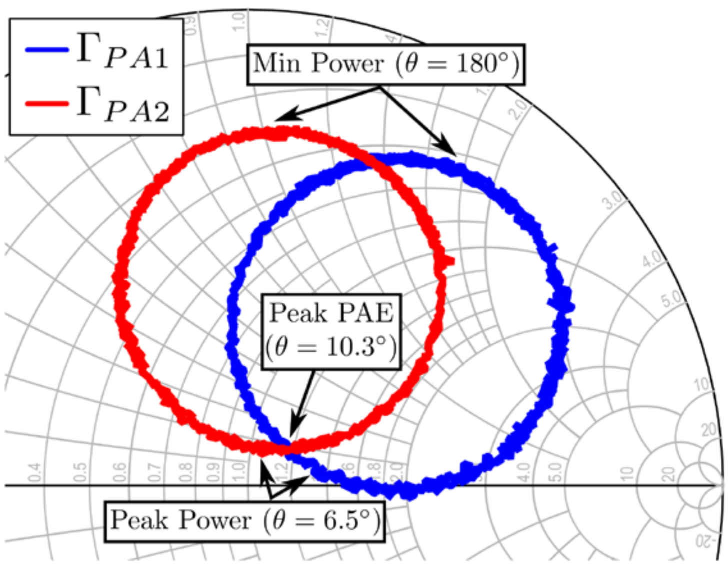
Isolated Outphasing PA

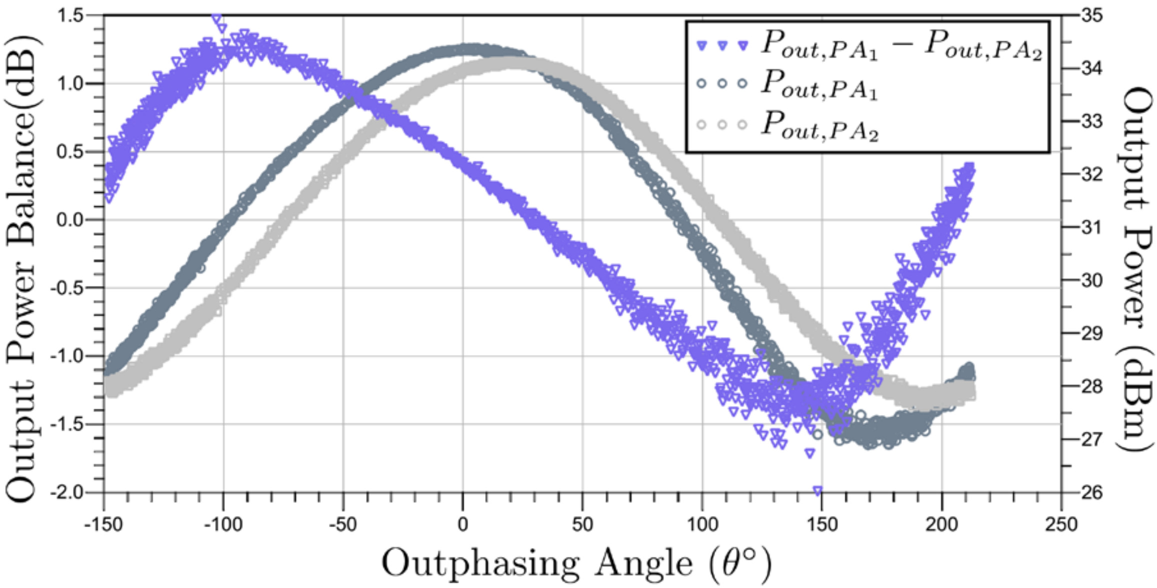




- Finite isolation yields minimal load modulation
- PAs rotate in opposite direction around contours
- 0.4 – 1.7 dB internal PA Pout imbalance caused by varying load

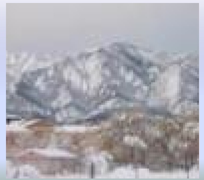
Non-Isolated Outphasing PA



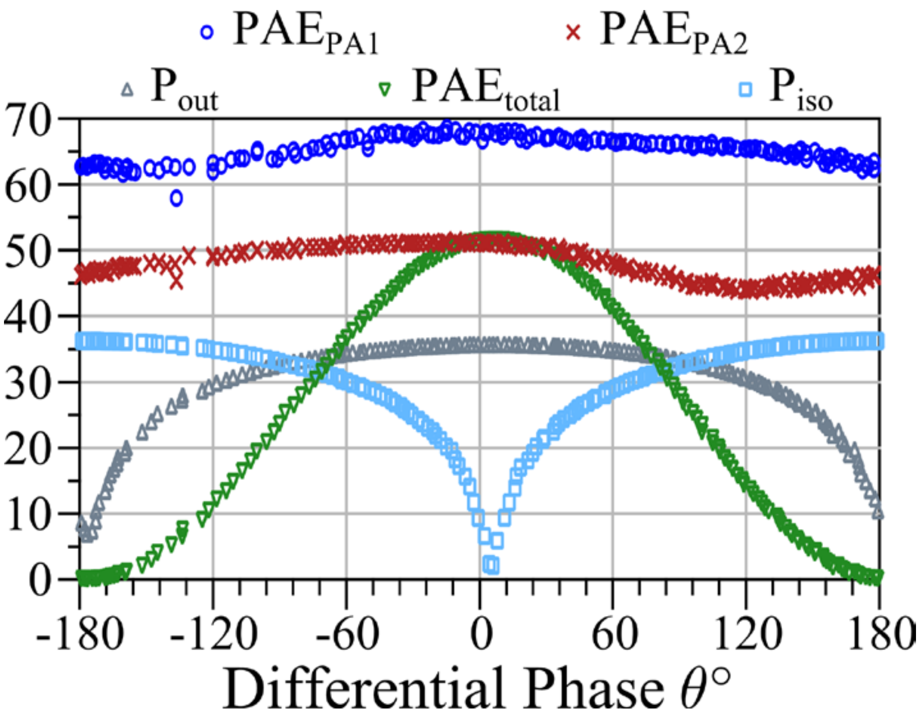


- Load modulation shows slight CW rotation due to ±1.5 dB internal PA Pout imbalance
- Peak power occurs near peak PAE
- Minimum Pout of 3.6 dBm near edge of smith chart

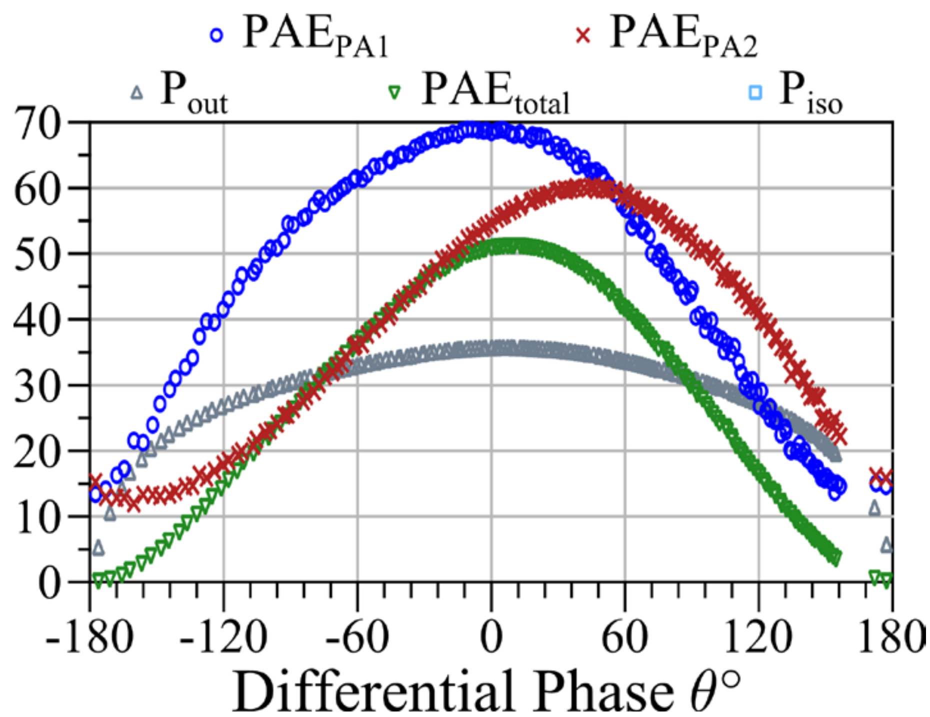
Comparison



Isolated



Non-isolated



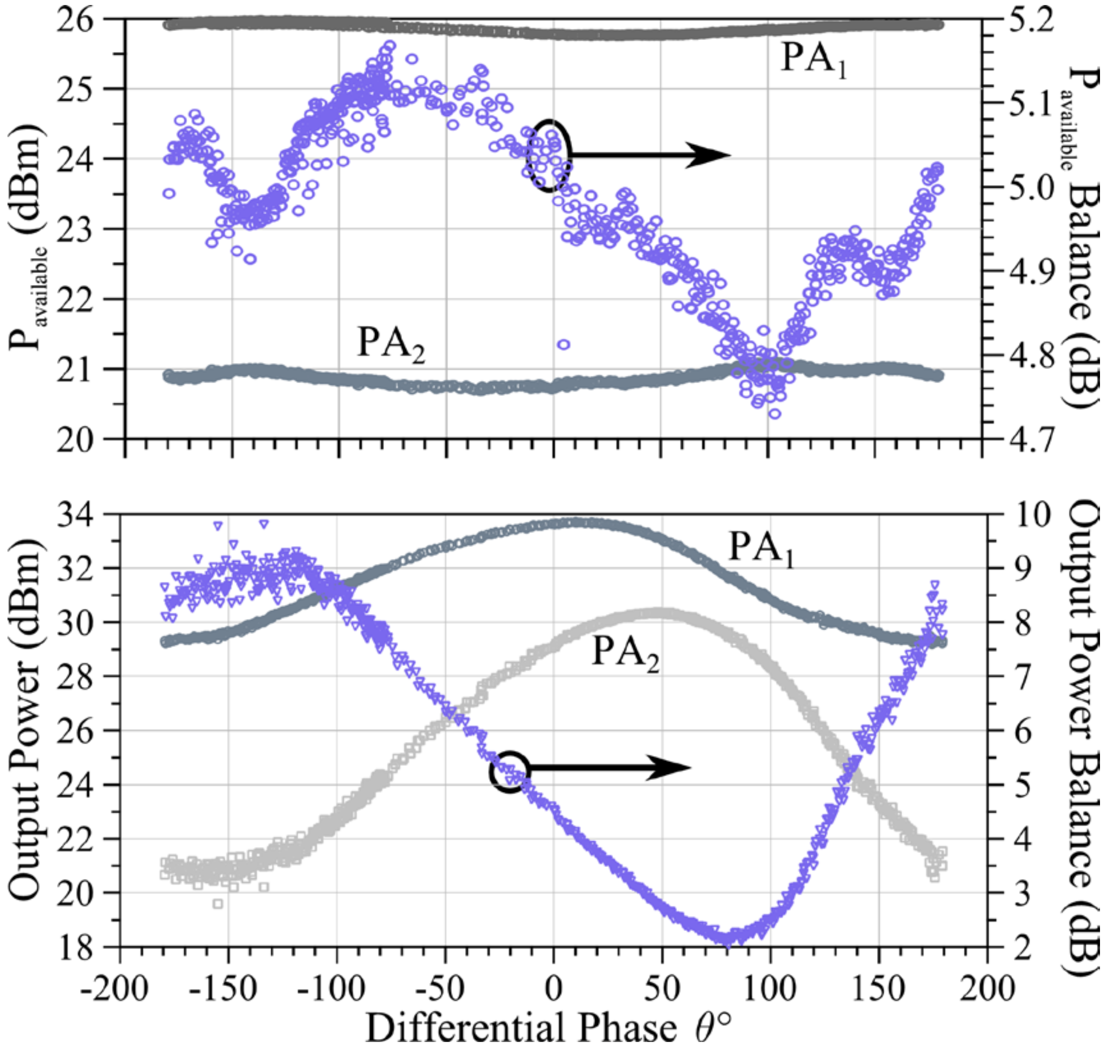
- Peak Pout = 35.8 dBm / 36.8dBm
- Peak PAE = 41.6 % / 59%
- Integrated design: 1 dB less loss

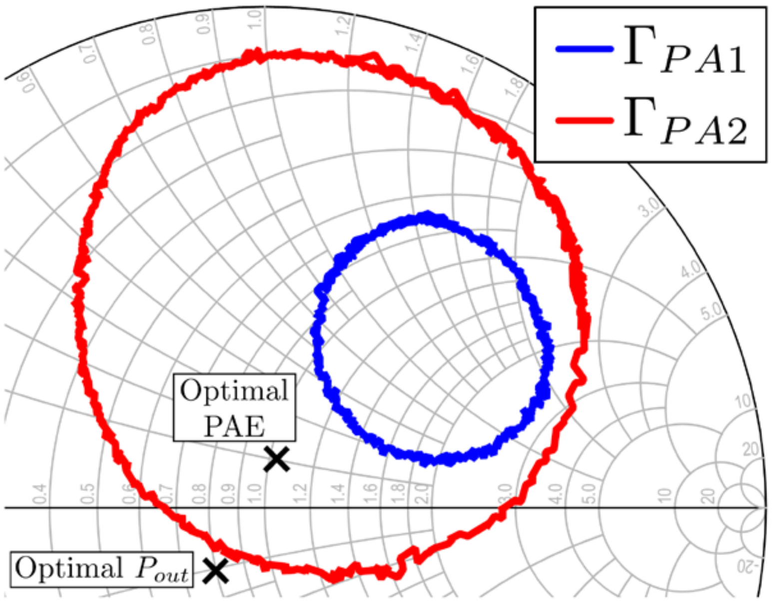
Peak Pout = 35.7 dBm / 37dBm

Peak PAE = 41.5 % / 60% (L=1.3dB)

8 % improvement in PAE at 4 dB OPBO

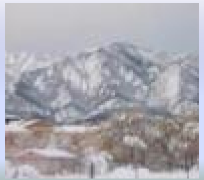
Effect of Power Unbalance





- 5±0.25 dB forced available power imbalance
- 2-9 dB internal PA Pout imbalance

Outline



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Doherty

- Simple, not expensive to implement, already accepted
- Broad bandwidth recently demonstrated
- Requires linearization
- Once designed, hardware cannot be modified to fit different signal statistics

Out-phasing

- Efficiency drops quickly with power back-off unless SM is used simultaneously
- Broadband signals require fast digital phase control

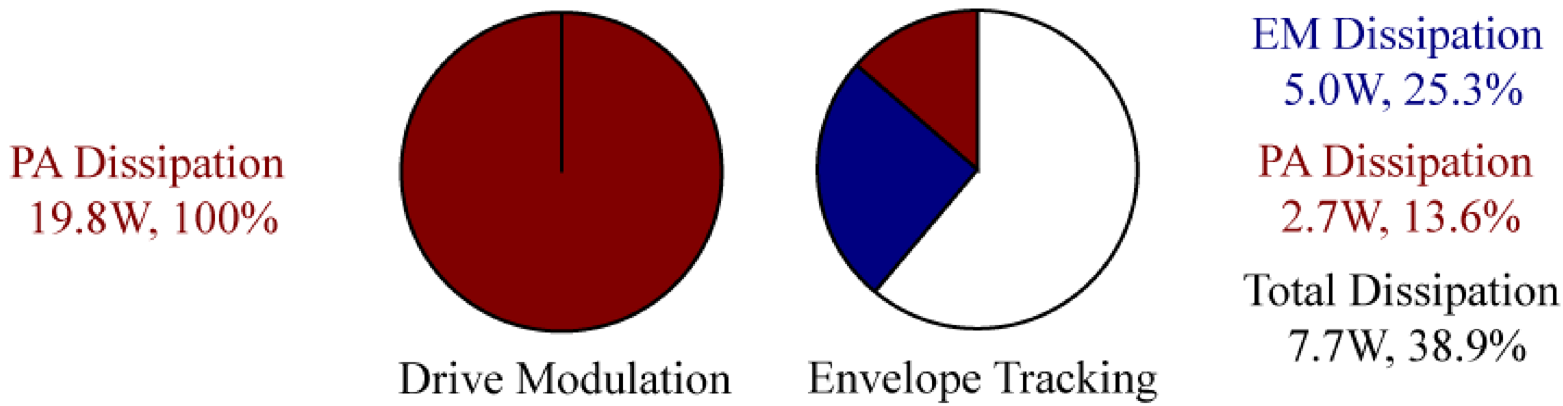
Supply modulation

- Requires efficient and fast supply modulator, stability compromised, needs linearization
- Can be digitally modified for different signals

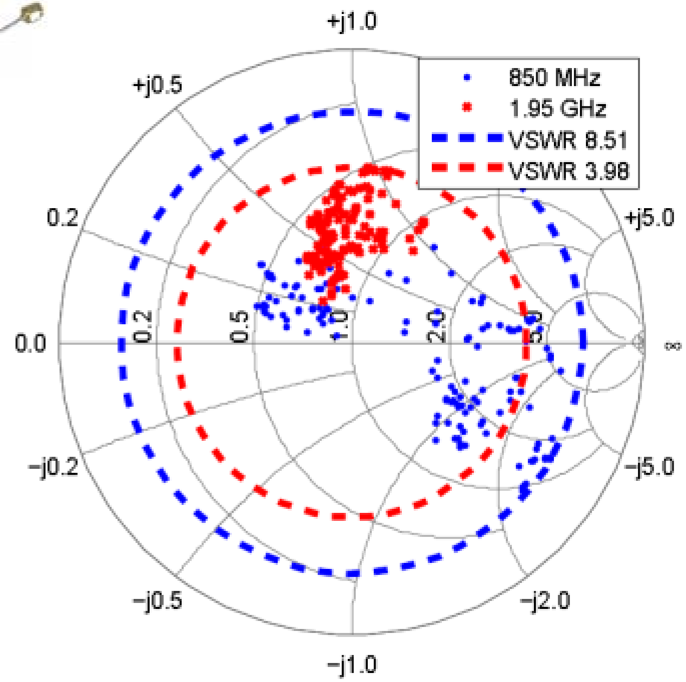
The heat advantage: example S-band PA

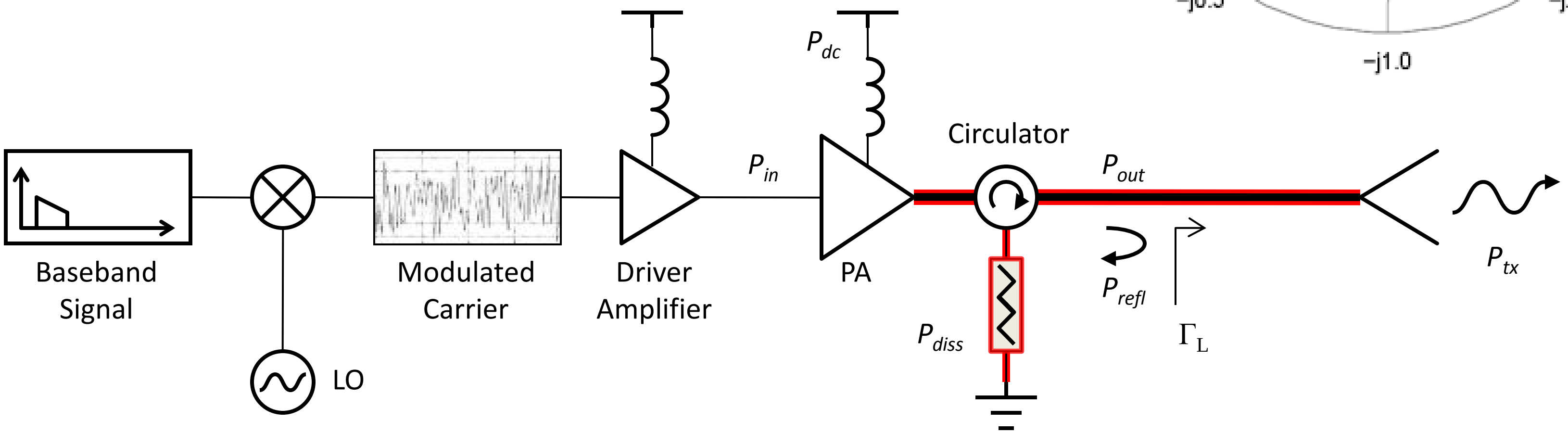
- Drive modulated conditions
  - Same W-CDMA signal
  - Same PA
  - Constant 32V V_{dd}
  - Achieves similar linearity
- Power consumption
  - **43% less power**
  - **75% longer from battery**
- Power dissipation
  - **61% less heat**
  - RF transistor operates **86% cooler**

	Drive (A)	Optimized Vdd
Peak/Average Power	40W / 8.5W	40W / 8.5W
RFPA drain eff.	30%	76%
SM efficiency	N/A	69%
ACP at 5 / 10MHz	-57/-58.3 dBc	-55.7/-57.8dBc
Transmitter efficiency	30%	52.5%
Supply power	28.3W	16.4W

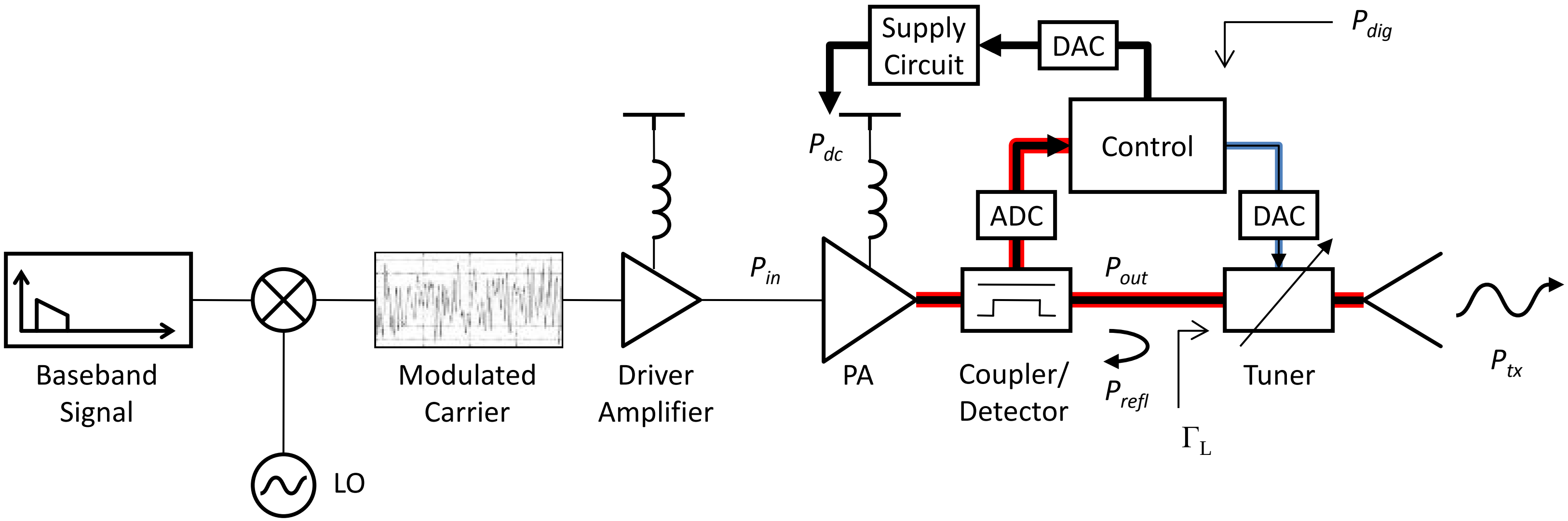


What if the antenna is not matched?





Matching the antenna



Efficiency improvement