Pad-Open-Short De-embedding Method Extended for 3-Port Devices and Non-Ideal Standards

W. Khelifi*, T. Reveyrand*, J. Lintignat*, B. Jarry*, R. Quéré*, L. Lapierre†, V. Armengaud† and D. Langrez‡
*XLIM, 123 av. Albert Thomas, 87060 Limoges Cedex, France
†CNES, 18 av. E. Belin, 31400 Toulouse, France
‡Thales Alenia Space, 26 av. F. Champollion, 31100 Toulouse, France

***Abstract*—This paper presents an extension of a three step de-embedding (Pad-Open-Short) method to a 3-port device for accurate on wafer MMIC S-parameters measurements. In the proposed method, an equivalent circuit-model using lumped elements is established according to the test-fixture. Furthermore, classical Pad-Open-Short method introduces systematic errors, observed beyond 20 GHz, due to perfect 'Open' and 'Short' standards assumption. This work also proposes a generalized Pad-Open-Short method with non-ideal standards.**

To validate the performance of this new method, reliable data were obtained from simulations and measurements of a GaAs transistor from UMS foundry operating up to 40 GHz.

***Index Terms*—De-embedding, 3-port, parasitics, On-Wafer Microwave Measurements, Open-Short, Calibration.**

I. Introduction

During the past few decades, there has been a tremendous increase in the use of multiport compact RF devices. Thus, a particular attention has been given to the accuracy of on wafer S-parameter measurements. Defining reference planes as close as possible to the device of interest was the motivation for de-embedding technique. Some are based on circuit lumped elements topology such as "Open", "Open-Short" or "Pad-Open-Short" techniques.

In the well-known "Open" de-embedding technique, the pad capacitance is measured on the open dummy structure and used to correct the measurement of the device-under-test (DUT).

Besides, the "Open-Short" de-embedding method uses two dummy structures in order to include interconnection resistance and admittance matrices [1], [2]. Specifically, this method is justified when the designer has difficulty to fabricate an accurate 50Ω matching standard, for the Short-Open-Load de-embedding technique, in an integrated circuit process, or when the area does not allow the use of a $\lambda/4$ (TRL) line. Moreover, at high operating frequencies or when the length of interconnects becomes longer, extending "Open-Short" to employ more dummy structures [3], [4], is required to increase the accuracy.

The "Pad-Open-Short" technique adds a third measurement to identify the Y_e matrix measured when the 'Pad' is terminated by an open circuit ($Y_{ext} = Y_e$) [5].

Such procedures have been published for 2-port devices framework assuming that "Open" and "Short" standards are ideals. In fact, a plenty of de-embedding methods for 2-port network are well established. However, few de-embedding methods for multi-port have been proposed. Moreover, it has been shown, in [6], that "Short" and "Open" patterns are not ideal since the presence of parasitics cannot be neglected at high frequencies.

The novelty of this work lies in the fact that the proposed de-embedding method for 3-port devices takes into account the imperfections of the standards. Furthermore, a 3-port transistor and its corresponding dummy structures, manufactured by UMS foundry on a GaAs technology, are characterized up to 40 GHz in order to validate the proposed method.

II. The Three Step De-embedding Procedure

A. Extension to 3-ports

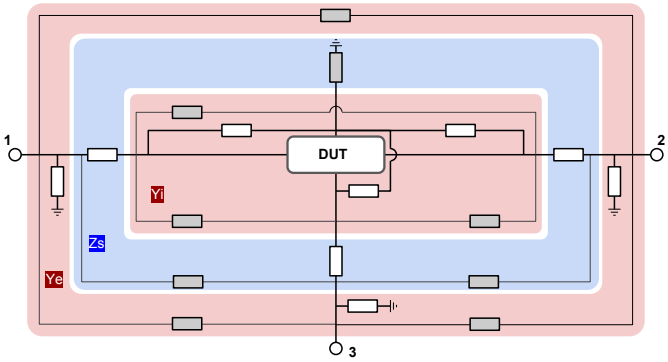

Fig. 1. Illustration of the parasitics assumed in the Pad-Open-Short de-embedding method for 3-port DUT. The coupling parameters are shown in gray.

In this section, the de-embedding method is depicted for three-port device case. The equivalent circuit topology for the test-fixture is shown in figure 1. This circuit has 18 unknown impedances that represents the parasitics. These parameters are distributed similarly between Y_e, Z_s and Y_i.

Indeed, the 'Pad' is modeled by a Y_e admittance matrix and the access line by cascading an impedance matrix Z_s and an admittance matrix Y_i. Usually, if the equivalent circuit model is sufficiently accurate, it is possible to de-embed the measured device (extrinsic reference plane) admittance matrix Y_{ext} in order to obtain the device under test admittance matrix Y_{int} at the intrinsic reference plane [5] such as:

$$\begin{aligned} Y_{ext} &= ((Y_{int} + Y_i)^{-1} + Z_s)^{-1} + Y_e \\ Y_{int} &= ((Y_{ext} - Y_e)^{-1} - Z_s)^{-1} - Y_i \end{aligned} \quad (1)$$

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B. Dummy non-idealities

Conventional "Open-Short" de-embedding method does not take into account the dummy imperfections: the S-parameters of the DUT are not accurate due to the intrinsic open fringe capacitance or the equivalent self-inductance of the short dummy which are not part of the DUT. Therefore, the non-ideality of the dummy structures and their impact on the final result need to be considered in order to obtain accurate S-parameters. Furthermore, since the "Pad" dummy structure contains only the probe pads, its non-idealities are not problematic as Y_e is directly measured by:

$$Y^{Pad} = Y_e \tag{2}$$

Hence, the analysis of the de-embedding method including non-ideal "Open" and "Short" is achieved by introducing admittance matrices of the standards (Y_{int}^{Short} and Y_{int}^{Open}) and solving the following linear system of equations:

$$\begin{cases} Z_{ext}^{Open} - Z_s &= \left(Y_{int}^{Open} + Y_i\right)^{-1} \\ Z_{ext}^{Short} - Z_s &= \left(Y_{int}^{Short} + Y_i\right)^{-1} \end{cases} \tag{3}$$

with $Z_{ext}^{Open} = (Y_{ext}^{Open} - Y_e)^{-1}$ and $Z_{ext}^{Short} = (Y_{ext}^{Short} - Y_e)^{-1}$.

By developing these equations we obtain a non-symmetric algebric Riccati equation, expressed by:

$$A + X.B + C.X + X.D.X = 0 \tag{4}$$

In our case, the unknown X is Y_i. Replacing $Y_{ext}^{dif} = (Y_{ext}^{Short} - Y_{ext}^{Open})$, leads to the following constant matrices:

$$\begin{aligned} A &= (I - Y_{int}^{Open}[I + (Y_{ext}^{dif})^{-1}.Y_{ext}^{Open}]^{-1}.Y_{ext}^{Open}) \\ &\quad .Y_{int}^{Short} \\ B &= I - [I + (Y_{ext}^{dif})^{-1}.Y_{ext}^{Open}]^{-1} \\ &\quad .[(Y_{ext}^{dif})^{-1}Y_{ext}^{Short} + (Y_{ext}^{Open})^{-1}Y_{int}^{Short}] \\ C &= -Y_{int}^{open}[I + (Y_{ext}^{dif})^{-1}Y_{ext}^{Open}]^{-1}(Y_{ext}^{Open})^{-1} \\ D &= -[I + (Y_{ext}^{dif})^{-1}Y_{ext}^{Open}]^{-1}(Y_{ext}^{Open})^{-1} \end{aligned} \tag{5}$$

A Schur decomposition method [7] is used to solve numerically the equation (4) that can not be solved analytically.

III. Experimental results and validation

A. Finding Y_{int}^{Short}

The S-matrix of the test-fixture, illustrated in figure 2.d can be partitioned into four sub-matrices associated to the extrinsic and intrinsic planes, as shown in equation (6).

$$S = \begin{pmatrix} S_{ee} & S_{ei} \\ S_{ie} & S_{ii} \end{pmatrix} \tag{6}$$

Therefore, the general embedding equation is expressed as follows [8]:

$$\begin{aligned} S_{ext} =& S_{ee} \\ &+ S_{ei}.(I - S_{int}.S_{ii})^{-1}.S_{int}.S_{ie} \end{aligned} \tag{7}$$

where I is the identity matrix, S_{ext} is the scattering matrix at the extrinsic reference plane and S_{int} at the intrinsic reference plane of a multiport standard. Equation (7) can be inverted as far as the global system is balanced:

$$\begin{aligned} S_{int} =& {S_{ei}}^{-1}.(S_{ext} - S_{ee}) \\ &.\left(S_{ie} + S_{ii}.{S_{ei}}^{-1}.(S_{ext} - S_{ee})\right)^{-1} \end{aligned} \tag{8}$$

In our case, in order to identify the parasitics of the "Short" standards, the "Pad + Line + Short" 3-port circuit, represented in figure 2.c, and the "Pad + Line" 6-port test-fixture circuit, represented in figure 2.d, have been simulated with Keysight Momentum. The non-ideal 3-port "Short" standard is then calculated according to equation (8). This S-matrix is converted to Y-parameters: Y_{int}^{Short}. This procedure, carried out on the "Open", allows us to verify that the latter can be considered as ideal dummy.

B. EM simulations results

Assuming ideal "Open" dummy ($Y_{int}^{Open} = 0$) and non-ideal "Short" dummy (a via-hole in micro-strip structure makes Y_{Short} exists), simplifies parameters expression (5) as:

$$\begin{aligned} A &= Y_{int}^{Short} \\ B &= I - [I + (Y_{ext}^{dif})^{-1}.Y_{ext}^{Open}]^{-1} \\ &\quad .[(Y_{ext}^{dif})^{-1}Y_{ext}^{Short} + (Y_{ext}^{Open})^{-1}Y_{int}^{Short}] \\ C &= 0 \\ D &= -[I + (Y_{ext}^{dif})^{-1}Y_{ext}^{Open}]^{-1}(Y_{ext}^{Open})^{-1} \end{aligned} \tag{9}$$

The Y_i solution (admittance matrix) is obtained numerically using the Schur algorithm [7]. Note that the Zs (impedance matrix) can be deduced afterward using equation (3).

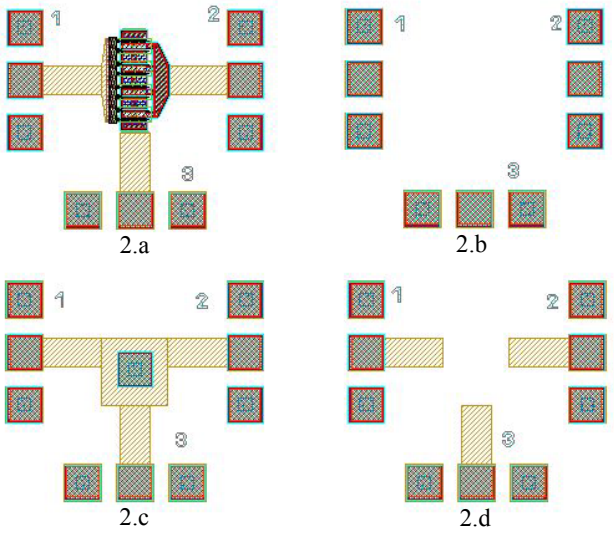

Fig. 2. Layout plan figures of the test structures 2.a DUT with interconnections 2.b Pad 2.c Short 2.d Open.

Figure 2.a illustrates the layout of the DUT and dummy patterns. Specifically, the DUT used in this procedure is high-electron-mobility-transistor (HEMT) from UMS foundry. The latter test fixture has a characteristic impedance of 50Ω and a 140μm interconnection line length. The dimensions of the

probe pads are 88 μm $\times$ 88μm, and the structures have been laid out for 125μm-pitch probes. Besides, the dummy set is composed of pad figure 2.b, short figure 2.c and open patterns figure 2.d.

The proposed de-embedding method, which takes into account the imperfections of the dummy patterns, as well as the conventional method (assuming the use of ideal dummy [5]) are applied to the aforementioned UMS transistor. Figure 3 illustrates a comparison of the simulated S-parameters for the conventional and proposed methods applied to the dummy structures depicted in figure 2. The simulations of the DUT are also plotted to verify the accuracy.

It can be observed that the proposed method, taking into account the via-hole parasitics, illustrated by the red curve, highly increases the accuracy of the de-embedding procedure in contrast to the conventional method.

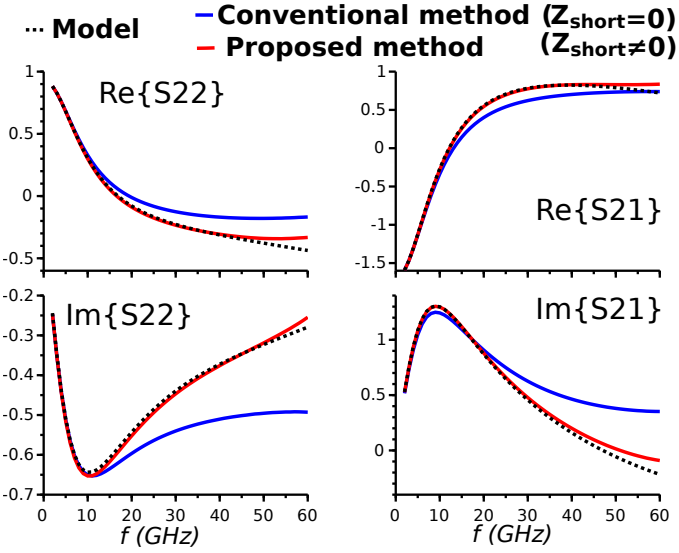

Fig. 3. Comparison of the "Pad-Open-Short" de-embedding with the proposed and the conventional methods.

C. Measurements results

In order to validate the performance of the proposed method, the dummy structures and the transistor were measured with a Keysight PNA-X vector network analyzer (VNA) on a probe station from 2 GHz to 40 GHz.

Before measuring the dummy structure, VNA and probe station were calibrated with a Short-Open-Load-Thru (SOLT) kit placed on an Impedance Standard Substrate (ISS). This reference plane is our extrinsic one.

3-ports "Open" (figure 2.d) and "Short" (figure 2.c) dummy structures have been simulated and measured. S_{11} and S_{33} port matching examples are plotted in figures 4 and 5. It can be observed that the simulated and measured curves are close to each-other, which validates the simulation results and justify the assumptions about the standard. Furthermore, the measured scattering parameters of the dummy structures were then used to extract the DUT parameters using the two possible methods for "Pad-Open-Short".

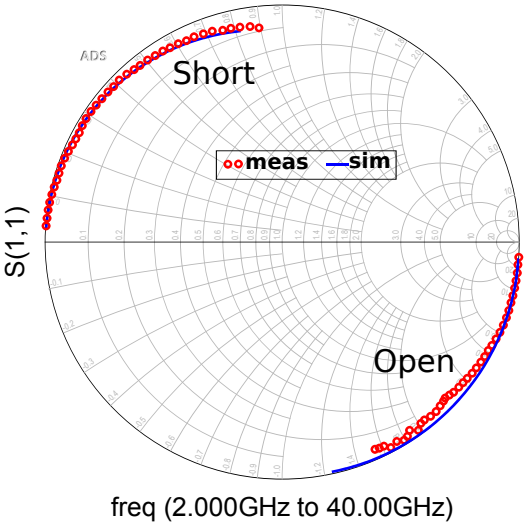

Fig. 4. Simulation vs measurement of S_{11} of the "Open" and "Short" dummy structures.

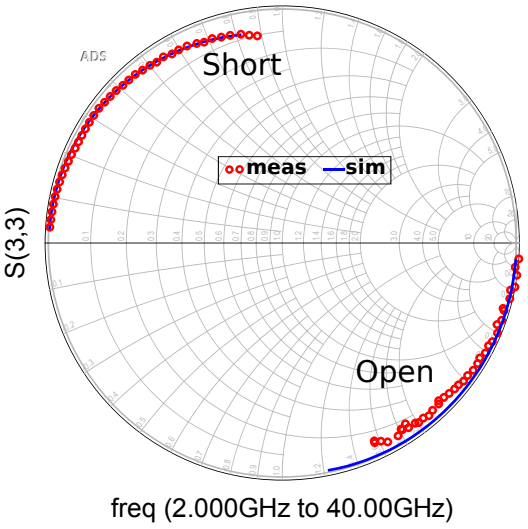

Fig. 5. Simulation vs measurement of S_{33} of the "Open" and "Short" dummy structures.

In figure 6, a comparison with the transistor model is presented on the de-embedded S_{21}. The two methods (the conventional and the proposed new method) for "Pad-Open-Short" de-embedding are compared. The new method shows accuracy improvement above 15 GHz. The classical method, for which the parasitics of the "short dummy" are not taken into account, indicates that these effects cannot be neglected for frequencies above 20 GHz. The enhancement provided by the proposed method is very well highlighted here. The measurements validate the proposed method up to 40 GHz.

Figure 7 shows the 3-port model scattering parameters (simulated) and the corresponding measurement extracted by implementing the proposed de-embedding method. It can be observed that the simulated and measured S-parameters of the transistor using the proposed "Pad-Open-Short" method are in

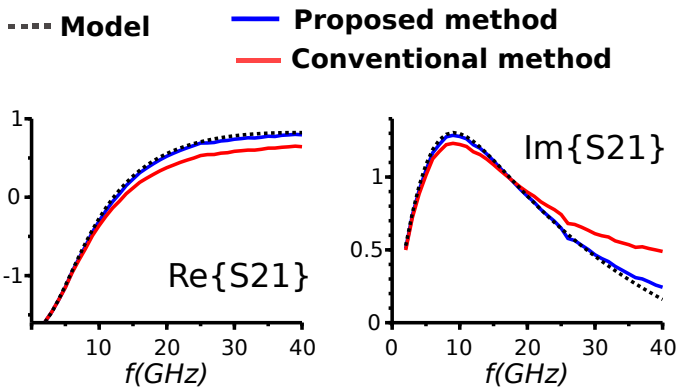

Fig. 6. S_{21} measured with 2 version of "Pad-Open-Short".

quite good accordance for a frequency band of 2 GHz up to 40 GHz which validates the proposed methodology and the design concept.

IV. Conclusion

In this study, we have proposed an extension for the three step de-embedding procedure to a 3-port device taking into account the imperfections in the standard. Furthermore, a 3-access circuit topology is proposed in addition to a simple method for obtaining multi-port S-parameters of standards.

The proposed de-embedding method can further de-embed the interconnect parasitics. Indeed, the effects of the external parasitics on device characteristics can be removed up to 40 GHz. Compared to the conventional method, this result has been confirmed by measurements on a high frequency GaAs transistor. Simulation and measurement results have shown that the proposed method has a better self-consistency and a higher accuracy than the conventional method.

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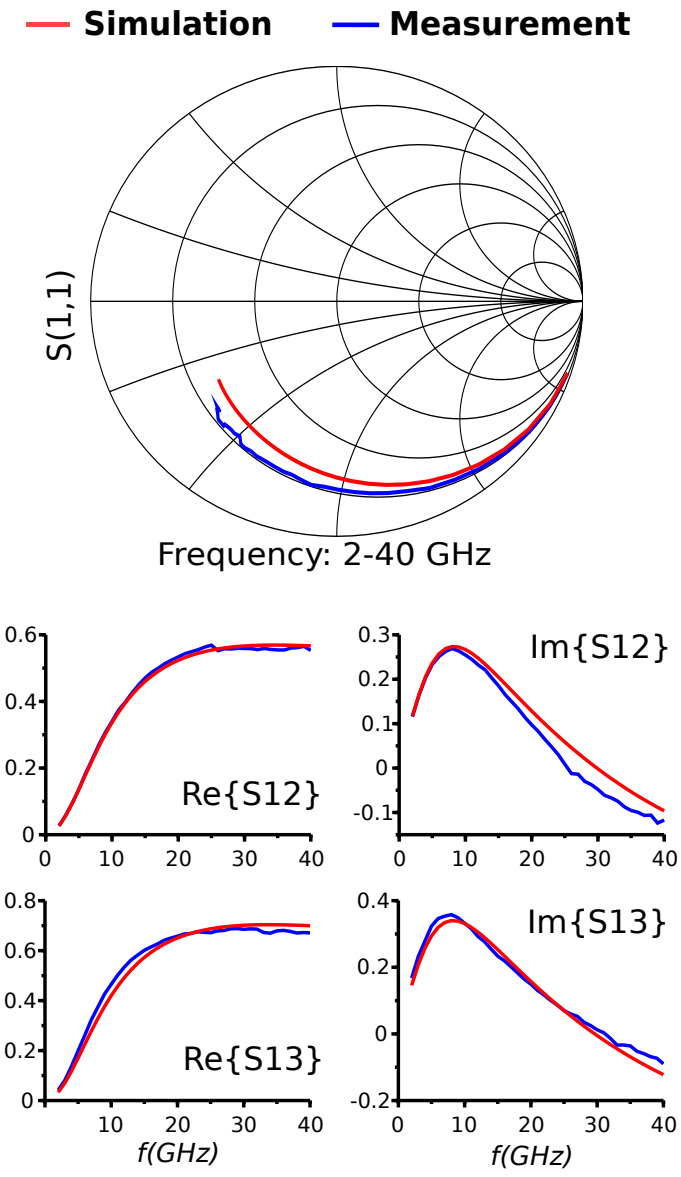

Fig. 7. De-embedded measurements using the new "Pad-Open-Short" method compared with the simulated transistor model on other S-parameters.