Non-linear Characterization and Modeling of 3-port Transistor

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***Abstract*—This paper presents a 3-port modeling and electrical characterization methodology for a GaAs HEMT transistor. From the I-V measurements and the S-parameters, a nonlinear model has been developed. The interest of this methodology is to determine accurate 3-port nonlinear model in high frequencies compared to the standard 2-port modeling approach provided by foundries. The modeling methodology presented in this paper has been validated up to 40 GHz for several bias points on a transistor expected for a Ku-band LNA design. Accuracy of this approach is highlighted by simulation and measurements comparisons.**

***Index Terms*—GaAs HEMT, Ku-band, LNA, S-parameter, characterization, Modeling.**

I. Introduction

The design of high performance MMIC circuit depends on the quality of transistor non-linear models provided within the Process Design Kit (PDK). In fact, a Process Design Kit (PDK), proposed by the founders of MMIC, provides microwave models of these elementary components such as different line configurations, resistors, inductors, capacitors, transistors for different gate development, $\cdots$

Indeed, transistors are usually modeled in 2-port configuration with the source connected to the ground. Moreover, using a 3-port transistor model identified from 2-port configuration is not optimal for several circuits such as LNA with resistive feedback [1]. Hence, a 3-port transistor model is well-advised in order to enhance the accuracy of high frequencies simulations. Therefore, a 3-port transistor model extracted from 3-port measurements is more suited for better simulation accuracy.

This paper presents the complete 3-port modeling process, from I-V curves, S-parameters and model parameter extractions. Finally, comparison between this new approach and a standard 2-port extracted non-linear model from a foundries PDK will be presented.

II. I-V measurements

In this section, the transistor measurement design patterns will be introduced. Figure 1 illustrates the layout of the test fixture used to characterize the transistor. Specifically, the considered transistor in this procedure is high-electron-mobility-transistor (HEMT) on a GaAs technology.

The aforementioned test fixture is characterized by an impedance of 50 Ω and an interconnection line length of 140 μm. The dimensions of the probe pads are 88 μm $\times$ 88 μm, and the structures have been laid out for 125 μm-pitch probes.

Figure 1 shows two reference plans. The first reference plan illustrates the reference plan of the RF and DC measurements, while the second reference plan depicts the intrinsic accesses of the transistor (gate drain source). It is worth-noting that for the RF measurements, a de-embedding has been applied in addition to the calibration in order to remove the effects introduced by these access lines [2].

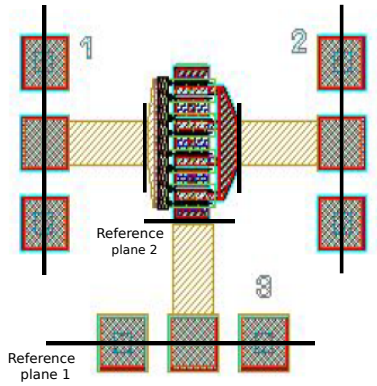

Fig. 1. Layout plane figure of the transistor measurement pattern.

A. Measurement setup

The I-V setup is based on a commercially available 2-port pulsed I-V measurement system (AMCADs BILT), bias tee and acquisition system (see figure 2). The 3-port transistor characterizations are performed with a short applied to DC path and a match on the RF path of the source access. Because this short is non-ideal, its DC resistance value, seen in the source reference plane, is properly identified. Its value will be obtained during the DC model extraction of the transistor. Furthermore, 50 Ω resistances have been connected on the RF accesses of the bias tee in order to ensure the stability of the transistor.

B. Current Source Model

The nonlinear drain current source of the model is based on the modified Tajima equations [3]. Moreover, The parasitic resistive value applied to the short access is taken into account

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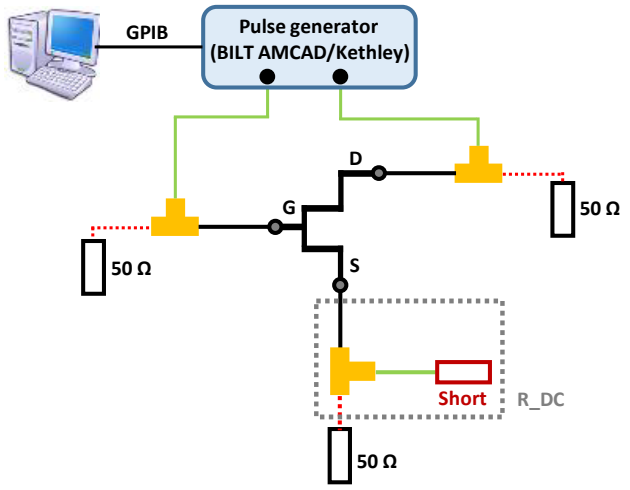

Fig. 2. 3-port I-V measurement bench.

during the DC parameters extraction values of the transistor. Figure 3 illustrates the comparison between the measurement and simulation results for the GaAs HEMT .

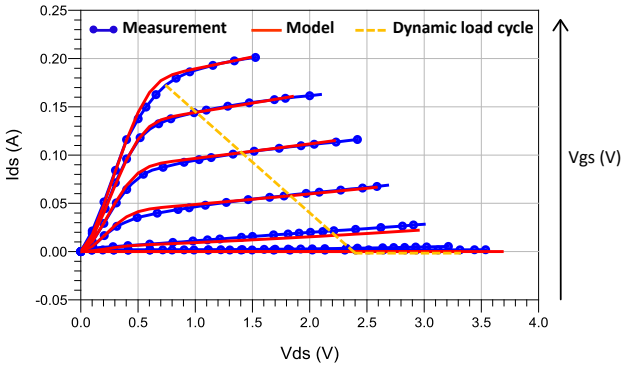

Fig. 3. Comparison between the I-V measured and simulated curves of a 8*60 μm GaAs HEMT (Vgs is stepped from -1 V to +0.2 V with step=0.2 V).

III. S-PARAMETERS MEASUREMENTS FOR RF MODEL PARAMETERS EXTRACTION

The S-parameters were measured for each point of the I-V network with a Keysight PNA-X vector network analyzer (VNA) on a probe station from 5 GHz to 40 GHz (see figure 4).

A. Linear Model

Figure 5 illustrates the electrical model of the 3-port transistor. In fact, the equivalent small signal model is composed of two parts: an intrinsic part and an extrinsic part corresponding to the parasitic elements due to the metalization accesses.

The principle of the linear modeling consist of the de-embedding of the extrinsic parameters in order to determine the intrinsic S-parameters (S^{int}) when the source access is connected to the ground. These latter are converted to Y-parameters (Y^{int}), then all the intrinsic parameters of the

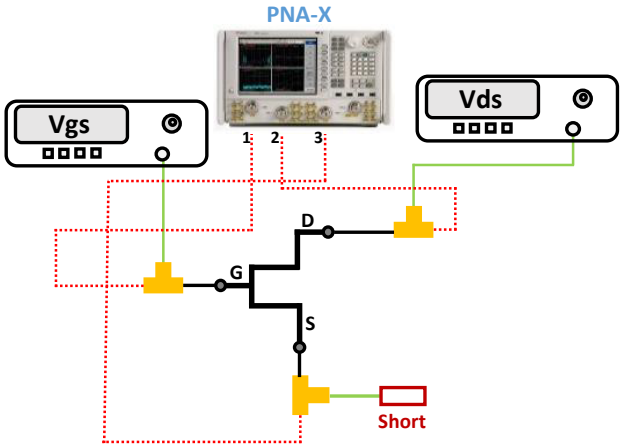

Fig. 4. 3-port S-parameters measurement bench.

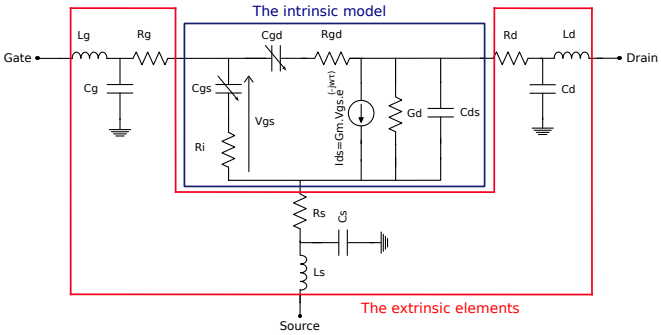

Fig. 5. Small signal model of the 3-port transistor.

model are extracted by analytical calculation since the equation system is linear. The set of extrinsic values is considered correct when the intrinsic parameters obtained after the de-embedding are independent of the frequency.

B. Non-linear Model

The linear model, introduced in the previous section, is validated for different polarization points. Indeed, only the intrinsic non-linear elements of the polar point will change, i.e. Id, Gm et Gd, Cgs et Cgd. In fact, Id, Gm and Gd are determined from the I-V network. Note that the multi-polarization extraction prove that these capacities depend on the voltage Vgs and Vgd. Nevertheless, [4] investigated the impact of the capacitance 1D and 2D on the transistor modeling and have proved that the error rate introduced by the 1D capacitance is low and do not impact the model. Hence, the modeling of the non-linear capacitances can be simplified by limiting their dependence to only one variable, which is the tension between the ports. On the other hand, the extraction of the non-linear capacities Cgs and Cgd is accomplished according to the dynamic load cycle much more extended than the LNA load cycle. The dynamic load line of the proposed transistor model is presented in figure 3.

In order to simplify the modeling procedure, the same mathematical equations are used for the aforementioned ca-

pacitances. Hence, the corresponding mathematical functions are expressed as follows [5]:

$$C = C_0 + \frac{C_1 - C_0}{2}.[1 + tanh(A * (V + V_m))] - \frac{C_2}{2}.[1 + tanh(B * (V + V_p))] \quad (1)$$

Once the model of the non-linear current source as well as that of the nonlinear capacitors is developed, the optimization of the extrinsic parameters (Cg, Cd, Rg, Lg, Ld, Ls ,Cs, Rs) is accomplished in order to ensure a consistency between the measurements and simulations of S-parameters. It should be noted that the access resistance Rd is optimized during the modeling of the current source and kept constant for the other steps. Furthermore, the accuracy of the model in the high frequencies range was checked through S-parameters measurements in various regimes of the transistor.

Figures 6 and 7 illustrate a comparison between the S-parameters measurement and the simulation of the developed model. The simulations of the design kit model are also plotted to verify the accuracy. The results of the developed model are in good agreement with the measurements model and outperform the results obtained with the design kit model. Indeed, the difference between the proposed model and the design kit can be clearly observed on S_{33}. In fact, both have the same electrical model, however the S-parameters of the proposed model are measured in a 3-port configuration.

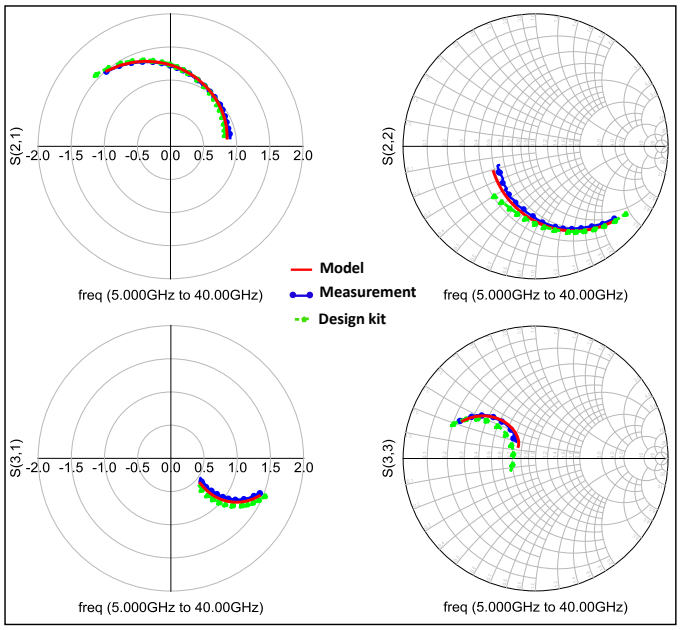

Fig. 6. Comparison between S-parameters measurement (blue symbols), proposed model simulation (red) and PDK standard model (green) for a 8*60 μm GaAs HEMT at (Vds=2 V, Ids=36 mA).

IV. Conclusion

In this study, a 3-port transistor modeling method has been described. The proposed model reproduces the I-V characteristics measurement for the 3-port configuration. The modeling methodology chosen for the 3-port GaAs HEMT structure have shown its efficiency at high frequency compared to the design kit model. Measurements and modeled S-parameters shows a good agreement and a higher accuracy up to 40 GHz for several bias points than the PDK model.

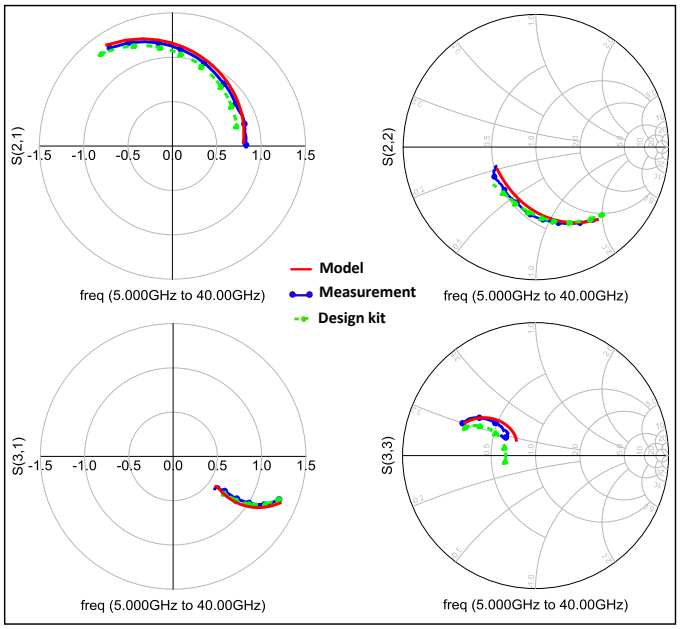

Fig. 7. Comparison between S-parameters measurement (blue), proposed model simulation (red) and PDK standard model (green) for a 8*60 μm GaAs HEMT at (Vds=1 V, Ids=144 mA).

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