A Drain-Lag Model for AlGaN/GaN Power HEMTs

O. Jardel*, F. De Groote*, C. Charbonniaud**, T. Reveyrand*, J. P. Teyssier*, R. Quéré*, D. Floriot***

*XLIM C²S² - UMR CNRS 6172, Université de Limoges, 7 rue Jules Vallès, 19100 Brive, France
**AMCAD Engineering, ESTER Technopole, BP 6915, 87069 Limoges, France
***ALCATEL-THALES III-V Lab/MITIC, route de Nozay, 91460 Marcoussis, France

***Abstract* — A circuit modeling drain-lag effects has been added in a non-linear electrothermal model for AlGaN/GaN HEMTs. Modeling these trapping effects allows a better description of the I-V characteristics of measured devices as well as their large-signal characteristics. This drain-lag model is well suited to preserve the convergence capabilities and the simulation times of the non linear models of theses devices. This paper presents our drain-lag modeling approach, the implementation of the model in CAD software, its operating mode, and also the parameters extraction from measurements. Then, significant comparison results will be reported on pulsed IV and large signal measurements with an AlGaN/GaN HEMT transistor.**

***Index Terms* — AlGaN/GaN HEMTs modeling, Drain-lag, Trapping effects.**

I. Introduction

Recently, some foundries began to commercialize AlGaN/GaN HEMTs, showing excellent performances for high power and high frequencies applications, thanks to their very high breakdown voltages and their high sheet carrier densities.

But these components, presenting on one hand free surfaces located a few nanometers above the channel and having on the other hand no additional doping, are very sensitive to the trapping effects. Some techniques, like surface passivation, have been found or borrowed to the GaAs HEMT and MESFET technologies to reduce the impact of these traps. But some trapping effects, originating in inherent material characteristics like lattice mismatches -at the origin of dislocations- are more difficult to reduce.

The gate-lag effects are attributed to the surface traps and the drain-lag effects to buffer or substrate traps [1][2]. Many measurements validated this point: techniques of surfaces passivations are now very efficient and we can notice that gate-lag effects are quasi-removed on the up to date devices. Nevertheless, drain-lag effects represent a big issue, as they imply current transients harmful to power and linearity characteristics.

However, there is a need for non-linear models of these devices, and hence some solutions have been proposed to deal with modeling dispersion effects on transconductance and on output characteristics in FETs [3][4][5] due to drain-lag effects during transient simulations. The circuit presented here takes into account these effects but also separates the capture and emission process, which leads to a better description of the pulsed IV and large signal characteristics obtained by harmonic balance simulations. Our method also enables an easy implementation in CAD software, and preserves the convergence capabilities and the simulations times of the devices non-linear models.

II. Description of the Drain Lag Effects

The term "drain-lag" is used to describe the slow transient response of the drain current when the drain-source voltage is pulsed.

When the voltage within the pulse is higher than the quiescent bias point one, the traps capture free charges. This phenomenon is very fast, compared to the typical lengths of the pulses.

When the voltage within the pulse is lower than the quiescent bias point, the traps release their charges. The process duration can be very large (about a few seconds in some cases).

As free carriers are captured or released, they do not take part to the output current instantaneously. This phenomenon is at the origin of current transients, as illustrated on the fig. 1, and induces a dispersion of the devices power characteristics.

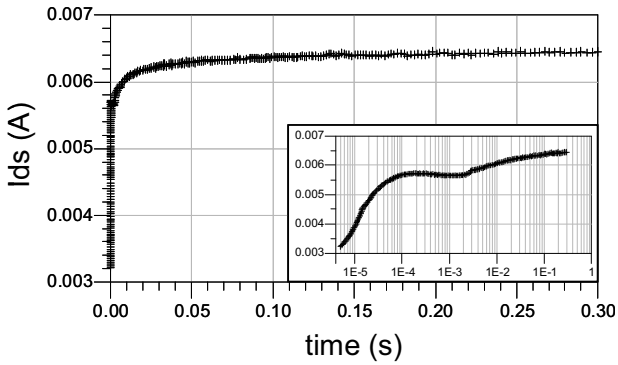

Fig. 1. Evidence of drain-lag phenomenon on a 0.6 mm AlGaN/GaN HEMT. Vgs is kept at a fixed value equal to -6V, whereas Vds is pulsed from 30 to 20V. Self-heating effects are negligible in this case.

Each trap level adds an exponential contribution to the current transient. Fitting this current transient would require at least 6

exponential terms, i.e. as many as trapping levels. Our model adds these exponential terms thanks to RC cells.

III. Circuit Description

Drain-lag effects can be considered as self-backgating effects, as they are caused by deep traps beneath the channel: the space charge area created by these traps acts as a virtual gate by constricting it, and so adds a contribution to pinch the transistor off [6][7]. Hence, the drain voltage transients are equivalent to a virtual gate voltage transient and a fortiori to a gate-source voltage transient. We will use this analogy in our model.

A one-trap drain-lag model schematic is given at fig 2.

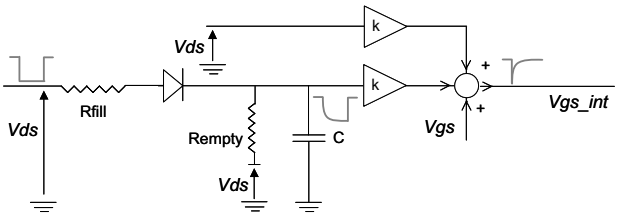

Fig. 2. Schematic of the drain lag model.

This circuit works as an envelope detector. There are two input voltages: Vgs and Vds; and one output voltage, named Vgs_int, which becomes the command voltage of the current source. The diodes have a threshold voltage of 0 Volt.

In the case where Vds increases, the diode is opened, and the capacitance C charges through the resistance R_{fill}. The time constant associated to the filling of the trap is given by:

$$\tau_{fill} \approx R_{fill}.C\,, \qquad (\text{as } R_{empty} >> R_{fill}) \qquad (1)$$

When Vds decreases, the diode blocks and the capacitance C discharges trough the resistance R_{empty}. The release time constant is given by:

$$\tau_{empty} = R_{empty}.C \qquad (2)$$

The density of each trap is directly linked to the amplitude of the transient it creates. The relative amplitude of the trap number n (i.e. if we normalize steady-state current value to 1) is noted k_{rel_n}. Each k_{rel_n} has to be multiplied by the total drain current there would be at steady state or if there were no traps to obtain the absolute amplitude of the trap transient k_n. This current is expressed as a linear function of Vgs for reasons of simplicity:

$$I_d = Gm_{DC}.\left(V_{gs} - V_{pinch-off}\right) \qquad (3)$$

Thus, we have:

$$k_n = k_{rel\_n}.Gm_{DC}.\left(V_{gs} - V_{pinch-off}\right) \qquad (4)$$

but the equation we exactly use is :

$$k_n = k_{rel\_n}.Gm_{DC}.\left(\left(above\left(V_{gs}, 0.1, -V_{pinch-off}\right) - V_{pinch-off}\right)\right) \qquad (5)$$

The function above works in the following way:

$$If\ Vgs<V_{pinch\text{-}off},\ then\ Vgs=V_{pinch\text{-}off},\ else\ Vgs \qquad (6)$$

The smooth transition between the two slopes is tuned by the second parameter (here equal to 0.1). An equation based on a tanh can also be used. The form of k_n is showed at fig 3.

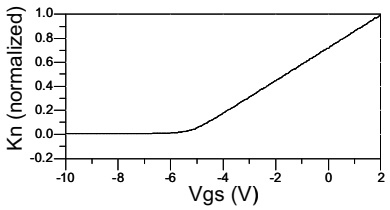

Fig. 3. Model parameter : k_n versus vgs.

IV. Parameters Extraction

In our example of fig.1, we can obtain a fairly adequate fit with only two time constants, as it is showed on fig 4, and thus we have implemented a drain lag circuit with two traps. As the dependence in temperature of time constants of the traps is not considered here, the measurements were performed at the estimated temperature of work of the device in its spotted application.

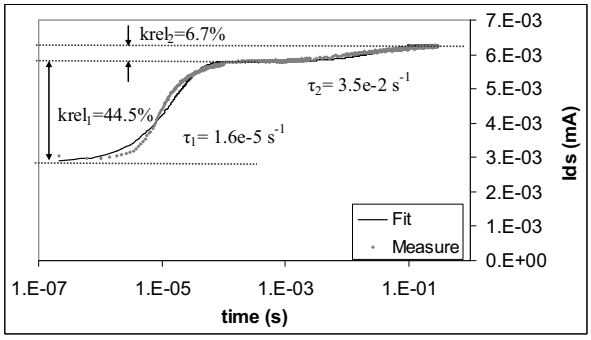

Fig. 4. Approximate fit of a current transient due to drain-lag effects on a 8x75µm device. We obtain the relative amplitudes and the time constants of the traps.

From this measured curve, we obtain the couples of parameters describing each one a trap: (τ1 , krel1) and (τ2 , krel2), where the terms τ_n represent the emission time constants.

The parameter Gm_{DC} in (3) is obtained from DC IV curves (at low Vds to limit thermal reduction of Gm_{DC}) or pulsed IV curves with a quiescent bias point of Vds0=0V, i.e. when trapping effects do not appear (see paragraph V).

The Rfill value is fixed at a small value, as we consider that the filling of the traps is very fast (<50 ns).

V. Pulsed I-V Characterization of the Transistor

A. Measurements description

In order to characterize the traps, pulsed IV measurements were performed at ambient temperature. The choice of the quiescent bias point allows to observe the trapping effects on the output current and even to discern gate-lag from drain-lag effects. The method has already been described in [8].
We can focus on three configurations:

1) If the quiescent bias point is Vgs0=0 V and Vds0=0 V, the classical IV curves measurement implies that Vgs is pulsed down and Vds is pulsed up. Hence, both gate- and drain-lag related traps are filling.
Considering that the filling of the traps is very fast compared to pulses duration, the traps state is that of the bias during pulse.

2) If the quiescent bias point is, for example, Vgs0=-6V (when the device is pinched-off) and Vds0=0V, the gate source and the drain source voltages are pulsed up during the measurement. Hence, the traps commanded by gate-source voltage are filling (fast), and the traps commanded by drain-source voltage are emptying (slowly). We can conclude that inside the pulse, the traps commanded by gate-source voltage remain in the same state they had at quiescent bias point, and the traps commanded by the drain-source voltage have changed state and are now in the state of the pulse bias.

3) If the quiescent bias point is, for example, Vgs0=-6 V (pinched-off) and Vds0=25 V, the drain source voltage is pulsed down for the measurement points where Vds< 25 V and pulsed up for Vds>25V.
Considering that the traps discharge is very slow compared to the duration of the pulses, the traps state inside a pulse is that of the quiescent bias point for Vds<25 V.
Note that we took care of maintaining the output current equal to 0 A. at quiescent bias points and that we chose the length of the pulses as short as possible to avoid thermal effects and their influence on output current.

These measurements allow us to discriminate traps and even gate- from drain-lag related traps: by comparing the measurement described in 1) with the measurement described in 2), we note that only gate bias changed and thus we observe the influence of gate-lag effects.
By comparing 2) with 3), only the drain bias changed and we observe the influence of drain-lag effects.
The IV networks showed fig.5 were measured on a 2x50µm AlGaN/GaN HEMT. On the first graph are superimposed two IV Networks corresponding to cases 1) and 2) and showing that gate-lag effects. On the second graph are compared cases 2) and 3) showing drain-lag effects.

This device has negligible gate-lag effects, which shows that the passivation layer is very efficient, but the drain-lag effects are important, inducing a large drain current dispersion and a knee voltage increasing.

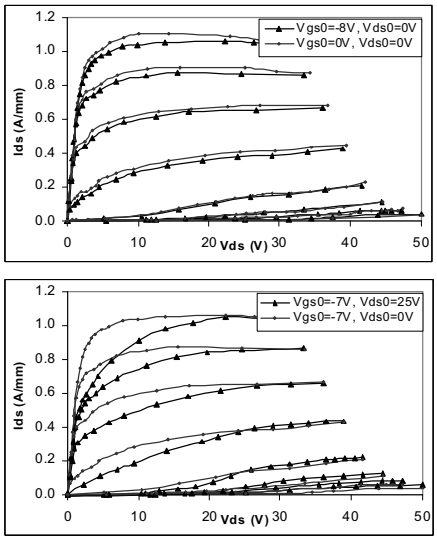

Fig. 5. Pulsed IV measurements at different quiescent bias points of a 2x50µm AlGaN/GaN HEMT (pulses length: 350 ns, period: 30µs, Vgs from -7 to 0V).

VI. Model Validation on Pulsed I-V and Large Signal Measurements

The AlGaN/GaN HEMT model used here has already been presented in [9]. However, the drain-lag subcircuit we present here could be implemented in any model, as it just impacts on the gate-source voltage at the input of the current source.

A. I-V simulations

Fig. 6 shows the influence of the trapping effects on pulsed IV characteristics. Measurements corresponding to case 3) are first compared to pulsed IV simulations at the same quiescent bias point, and then to simulations at a bias point corresponding to case 1). This latter case corresponds to the results we would obtain for all the quiescent bias points if the trapping model were inactivated.

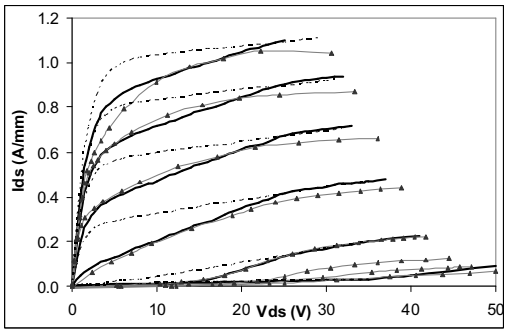

Fig. 6. Pulsed IV measurements for Vgs from -7 to 0 V at a quiescent bias point of Vgs0=-7V and Vds0=25V (lines with tics), pulsed simulations in the same conditions (continuous lines), and for a quiescent bias point of Vgs0= 0V, Vds0= 0V (dashed lines).

We can remark that the trapping model allows reproducing the current dispersion and the knee voltage increase due to drain-lag effects. The large decreases of the load cycles excursions during large signal operations induced by these phenomena have a significant influence on power characteristics. Thus, it is very important to reproduce them well, as we can see in the following chapter.

B. Large signal simulations

The modeled device is an 8x75µm AlGaN/GaN HEMT on SiC substrate from Thalès-Tiger. The model is electrothermal, and was extracted from pulsed I-V and [S]-parameters measurements. Load-Pull measurements are performed at 25 V in class AB at 10 GHz for an optimum load impedance of 20.3+j29.6 Ohms. The measured and simulated (with and without drain-lag modeling) large-signal characteristics are showed fig.7.

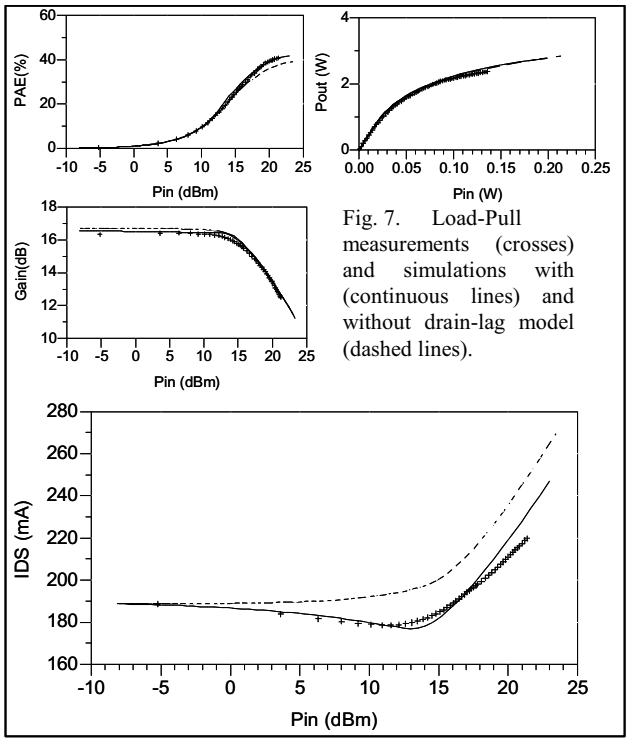

Fig. 7. Load-Pull measurements (crosses) and simulations with (continuous lines) and without drain-lag model (dashed lines).

What is to notice is that the measured DC output current decreases when the input power increases and increases after (when power saturation begins). This phenomenon is impossible to fit without the drain-lag model, which leads to an important error on this parameter. Drain-lag effects also induce a decrease of the output power and the gain. The PAE is increased and hence better fitted as it directly depends on the DC output current. Broadly, the power characteristics are better reproduced.

VII. CONCLUSION

A subcircuit modeling drain-lag by modifying the gate-source voltage at the input of the current source was presented. A very similar circuit can be used for gate-lag modeling by replacing the Vds dependence by a Vgs one, inverting the diodes terminals and choosing negative traps amplitudes. The latter circuit can be useful when devices present strong gate-lag effects, inducing a slower increase of the DC component of the drain current at the compression.
This circuit can be implemented on HEMTs and even MESFETs models. Its simplicity allows extracting quite fast the circuit parameters, with a few measurements.

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XLIM-C²S²/MITIC 7, rue Jules Vallès, 19100 Brive, France

Outline

Presentation of a sub-circuit modeling drain-lag (and also gate-lag) effects especially for AlGaN/GaN HEMTs non-linear models

- 1) Origins and impacts of trapping effect on transistors performances
- 2) Description of the sub-circuit modeling traps and the procedure of extraction of the parameters
- 3) Validation (Pulsed-IV, Load-Pull, LSNA) of a large-signal model including trapping effects

Motivation

- Lag effects are difficult to remove (especially drain-lag), and have harmful consequences on electrical performances of devices
- Large-signal models of transistors without trapping effects can’t reproduce well large-signal characteristics, especially for several load impedances.

Pros & Cons

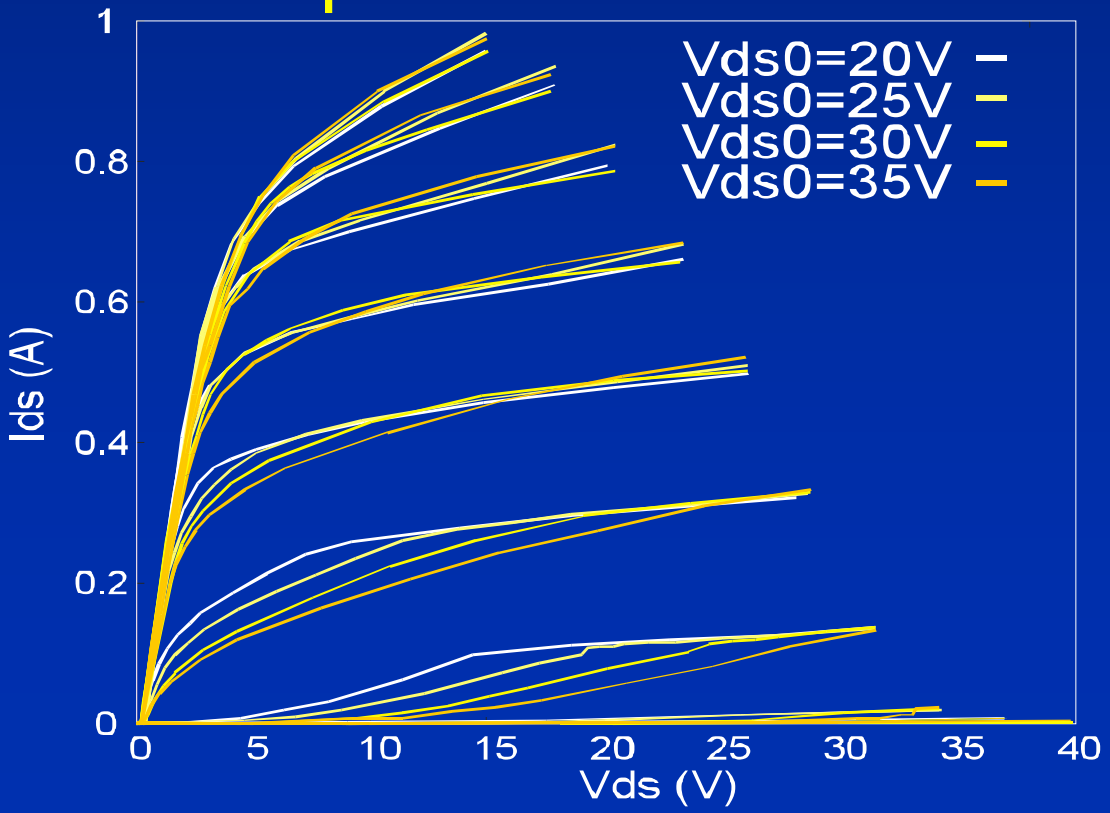
- ++ • Better description of the large-signal characteristics in function of the voltages excursions and the frequencies
- \- • Adds little complexity to the transistor model, and to the extraction procedure.
- \- • Simulation time slightly increased

➔ Designed to be easy to implement and to extract…

… simplifications to describe the trapping effects

The drain-lag phenomenon

- **Origins:** Attributed to buffer defects (lattice mismatches, dislocations, doping…)
- **Impact :** electrical anomalies – ex: dispersion of pulsed-IV characteristics versus quiescent Vds bias and pulses durations

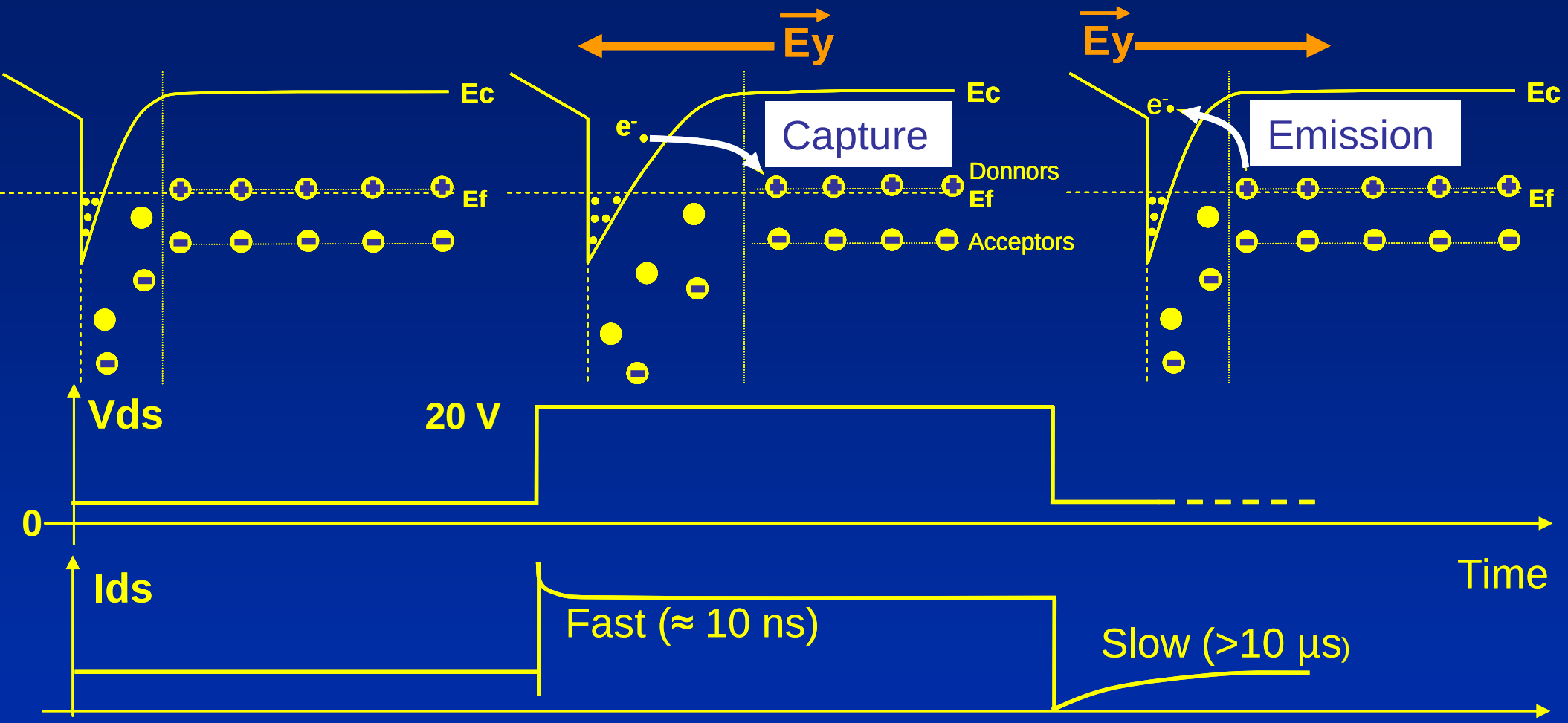


~~Id= f(Vgs,Vds)~~

Traps

Id=f(Vgs,Vds, Vbias, time)

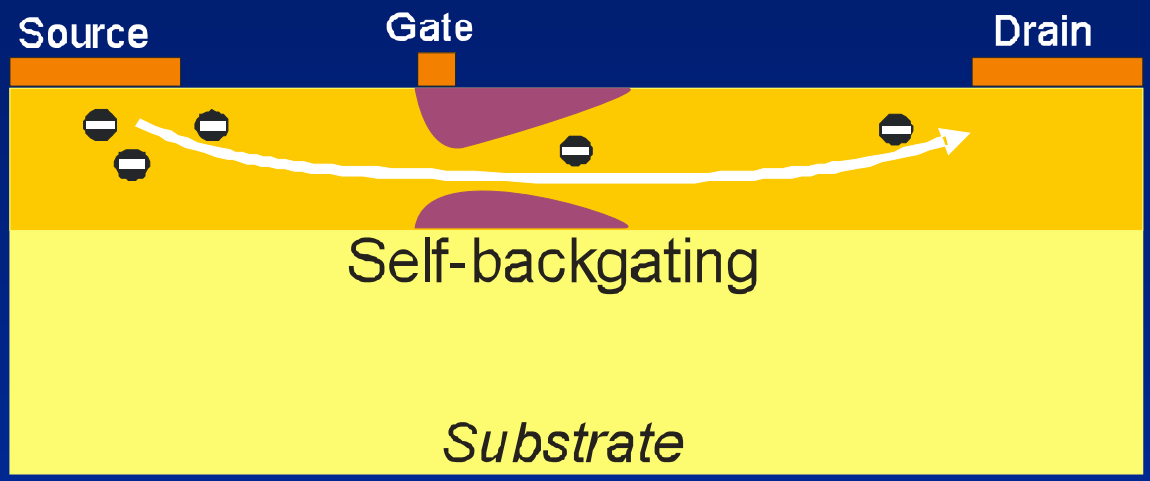
Bands point of view



- Some charges don’t participate to output current
- Asymmetric behavior of capture and emission times

➔ **Electrical performances decrease**

Modeling drain-lag: analogy with MESFET's self-backgating (1/2)



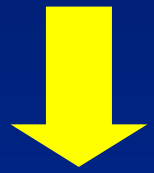
- MESFETs: charged traps at channel/substrate interface acts like a virtual gate

➔constricts the channel and decrease Ids (similar to a Vgs change)

- HEMTs: Traps capture free charges➔ decrase Ids …

Modeling drain-lag: analogy with MESFET's self-backgating (2/2)

$$Ids = f(Vgs, Vds, Vds\_bias, t)$$



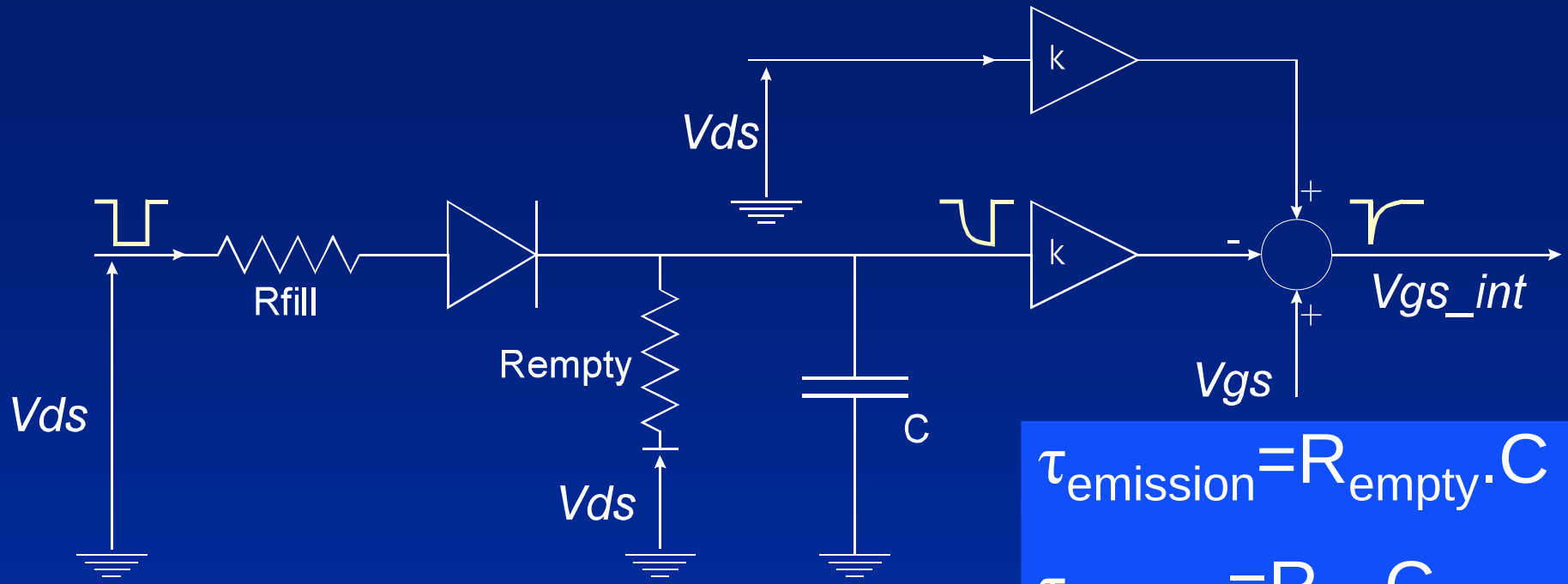
$$Ids = f(Vgs\_trap(Vds\_bias, t), Vds)$$

- Trapping effects are seen like a contribution on Vgs

➔ Do not change the current source topology, just change Vgs commanding the current source

➔ Easier to implement, can be used for different models/topologies of current sources

Drain-lag sub-circuit description



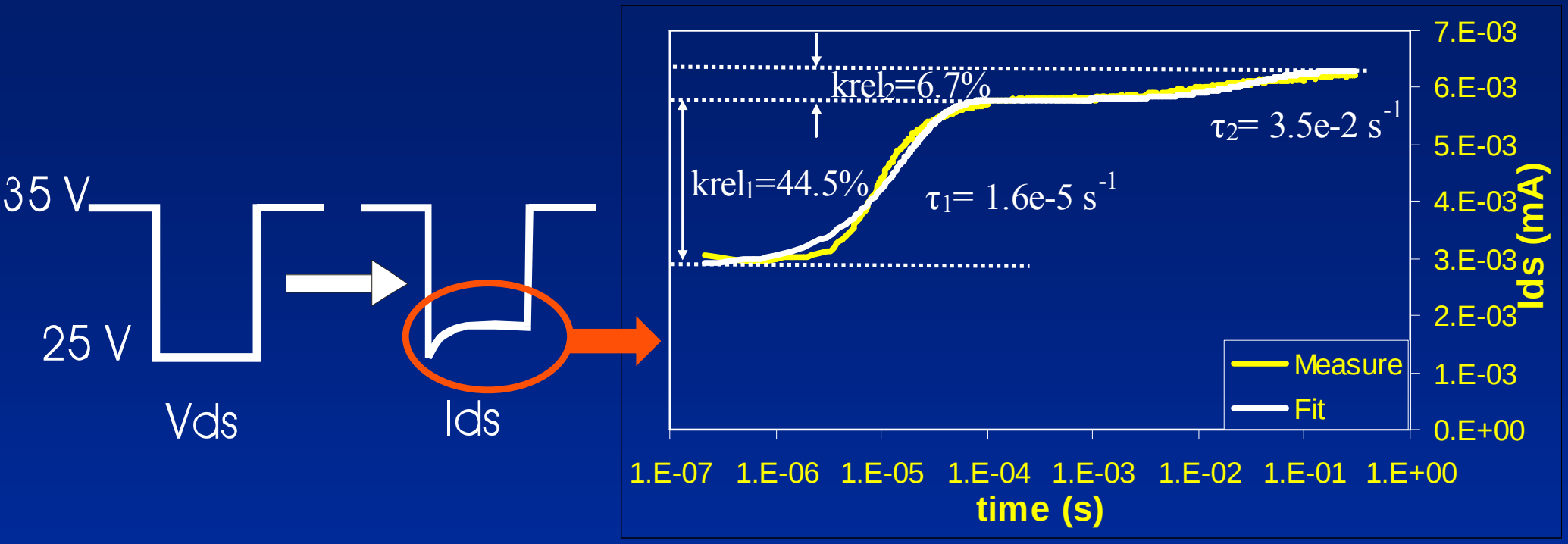
$\tau_{emission} = R_{empty} . C$

$\tau_{capture} = R_{fill} . C$

- Works like an envelope detector
- Number of circuits = number of traps modeled
- Only 3 parameters to extract for each trap:

  Rempty, Rfill, k

Extraction of parameters (1/2)



- Current transient measurement when Vds is pulsed (in order traps to release their charges)

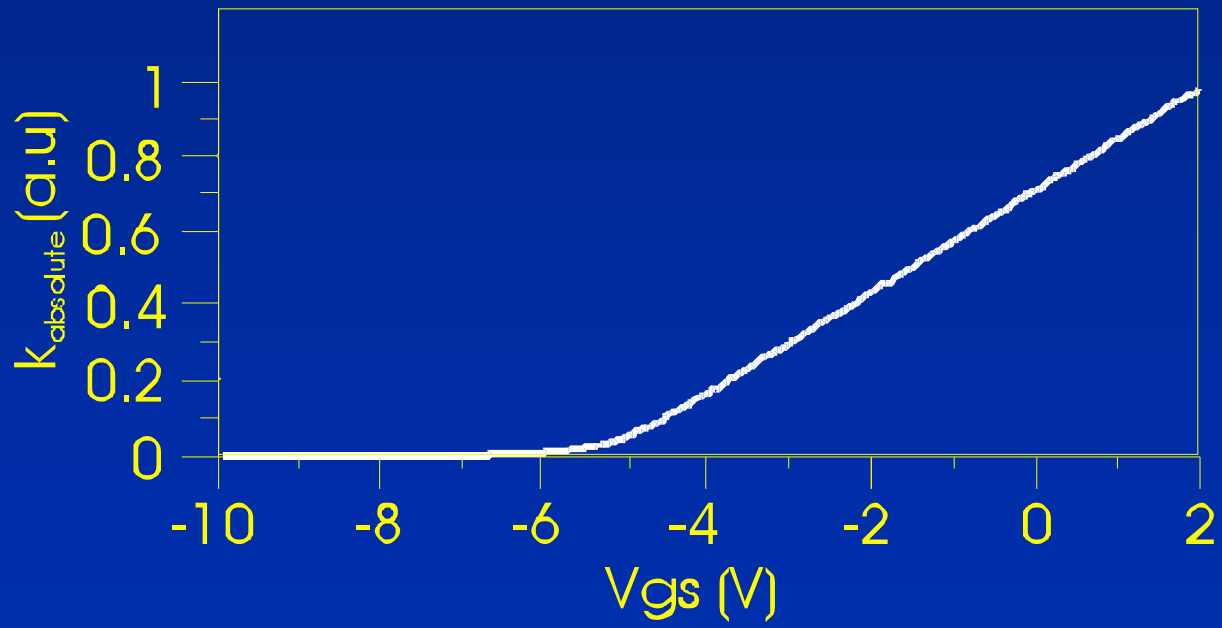
➔Obtaining: - Number of modeled traps
- Emission time constants
- Relative amplitude of each trap

Avoid thermal effects during meas.

Extraction of parameters (2/2)

Absolute amplitude of each trap (k) = relative amplitude (k_{REL}) *x* output current

Ids modeled simply as: *Ids = Gm_DC .(Vgs-Vpinch-off)*

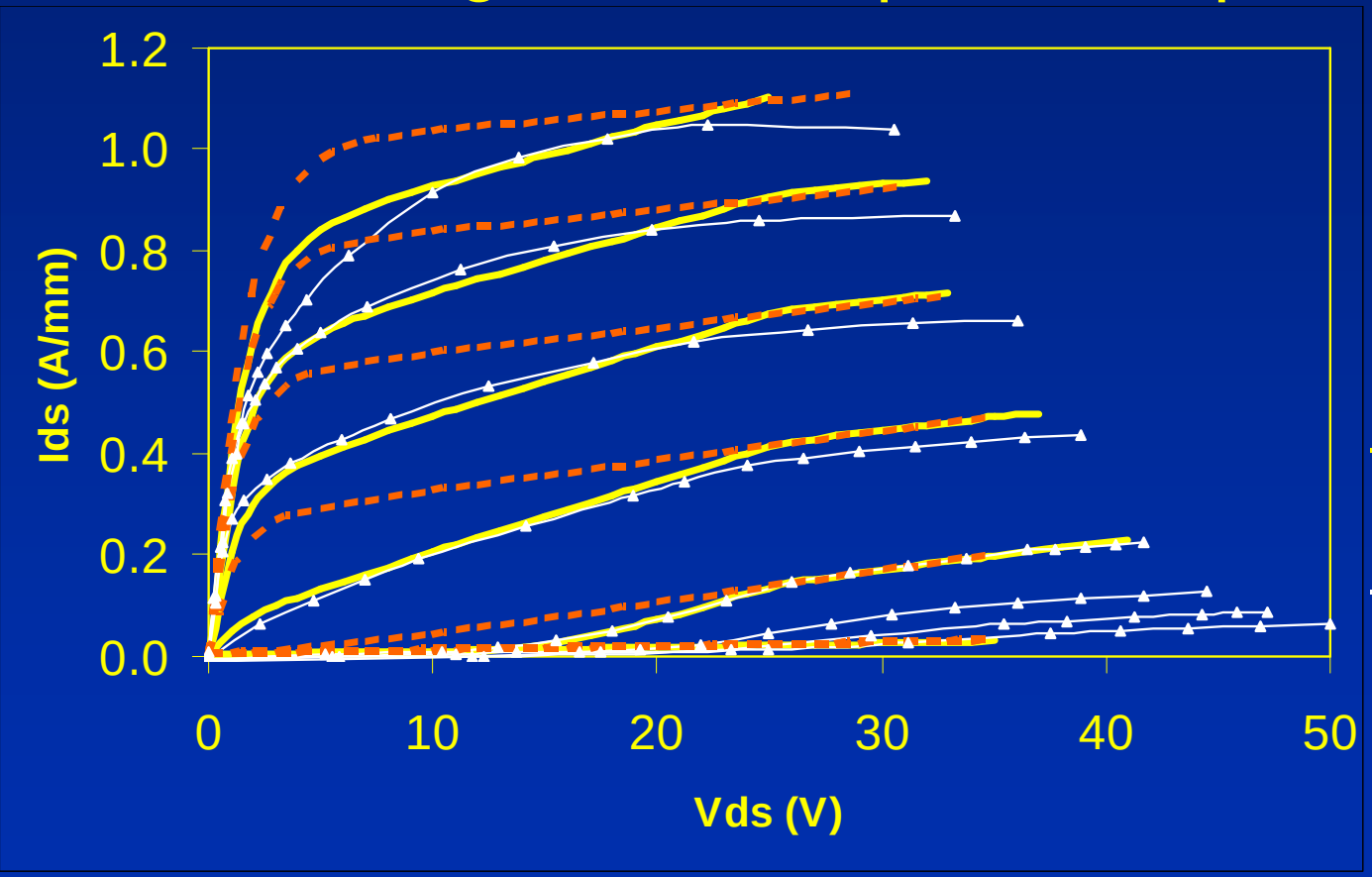


Capture time constants not measured (too fast)

➔fixed at a few nanoseconds

Model (drain-lag) validation on Pulsed-IV measurements

- Pulsed IV measurements @ Vds_bias=25V
- Pulses lenght: 400 ns, period: 10µs



capture<400 ns

400ns<émission

Traps model activated

inactivated

Measurement (Vds0=25V)

- Modeling of 1) Knee voltage increase

  2) Current decrease for Vds_pulse<Vds_bias

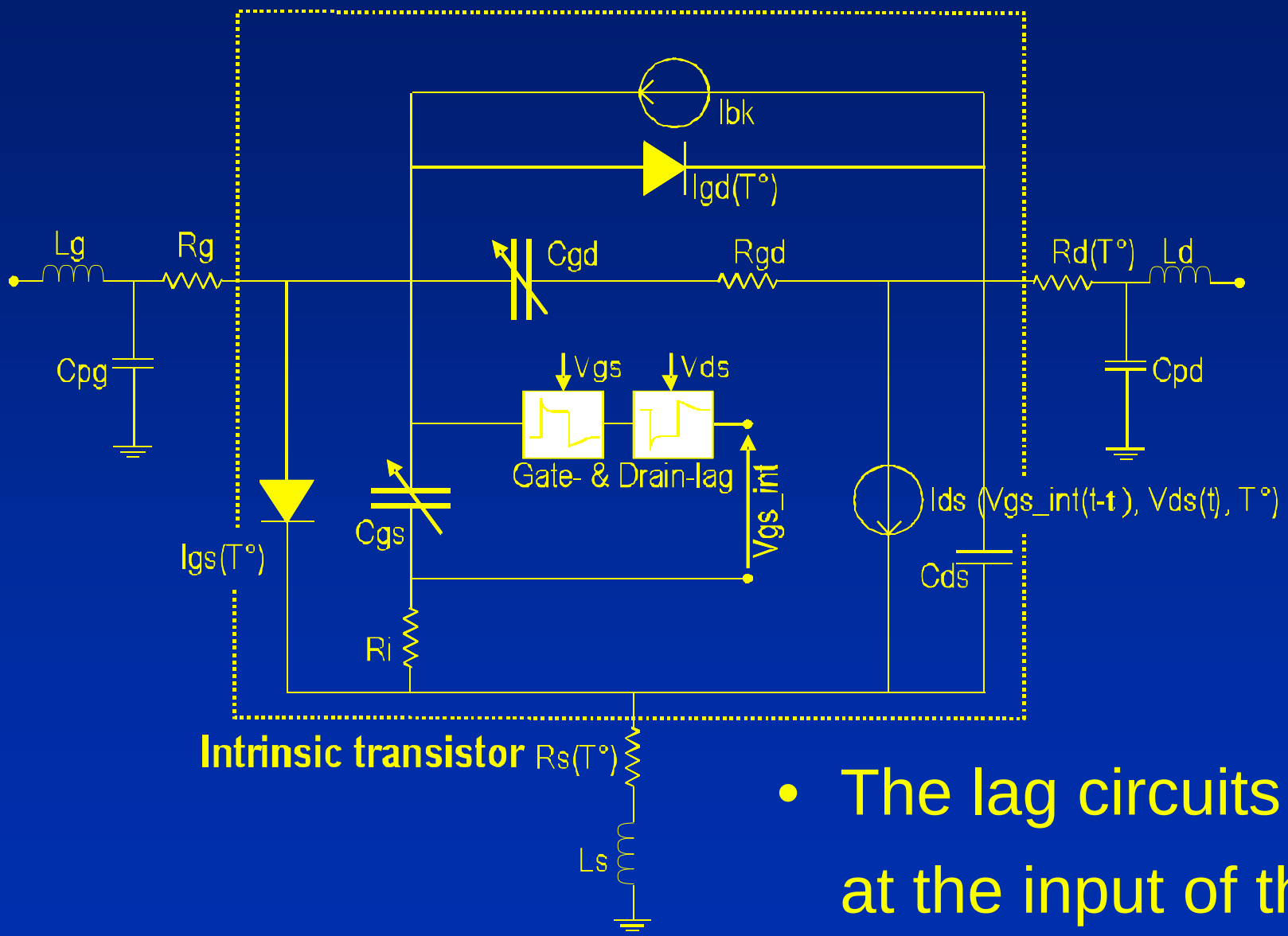
Model of Gate-lag

- The same sub-circuit topology can be used for modeling **gate-lag** effects

➔Invert diode terminals

➔ k negative

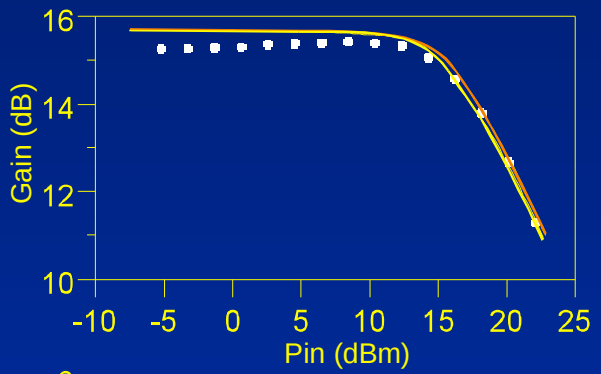
Topology of the non-linear model with gate- & drain-lag

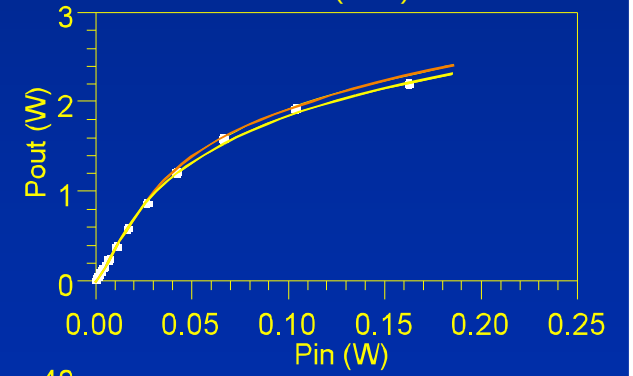


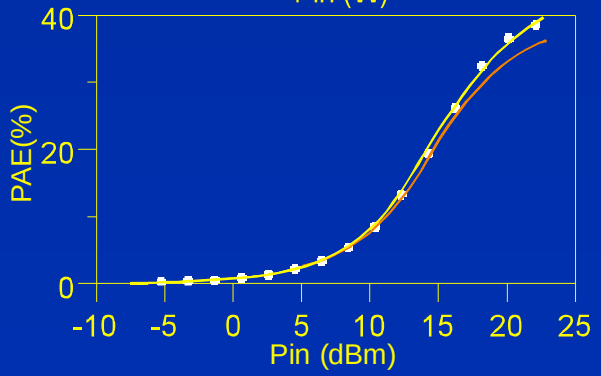
- The lag circuits are in series at the input of the main current source

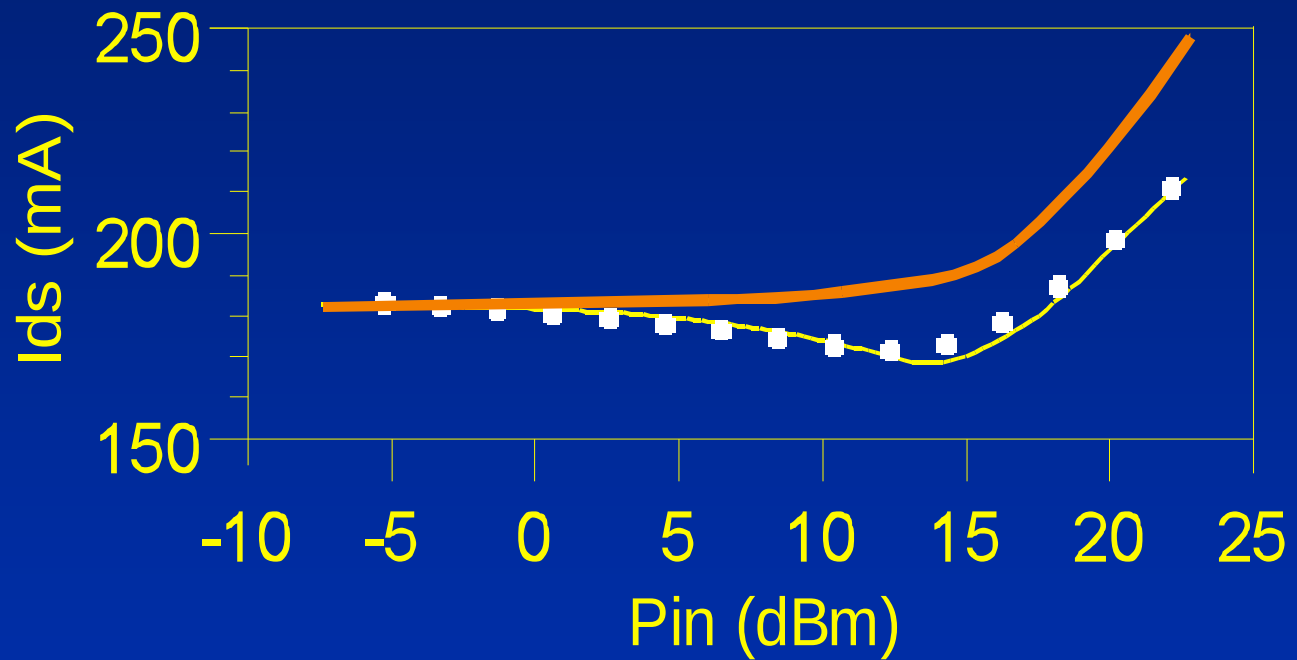
Load-pull validation @ 10 GHz

AlGaN/GaN HEMT 8x75µm : Load-pull measurement on Zopt=20.3+j29.6 (DC/CW) class AB (25V, 180mA)









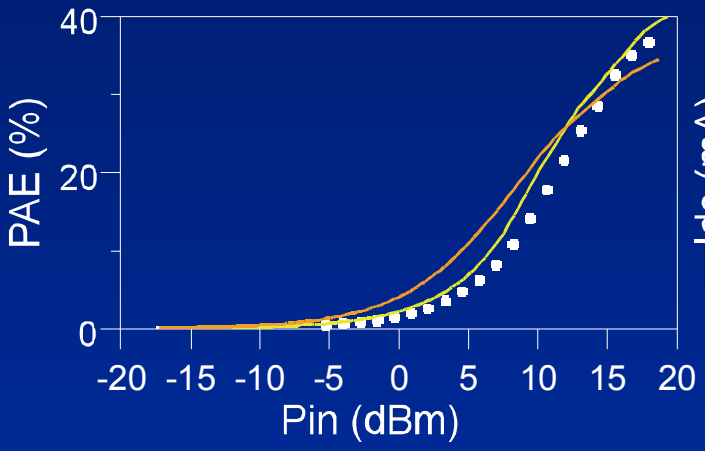
- Decreasing form of the mean output current only reproduced with traps modeled

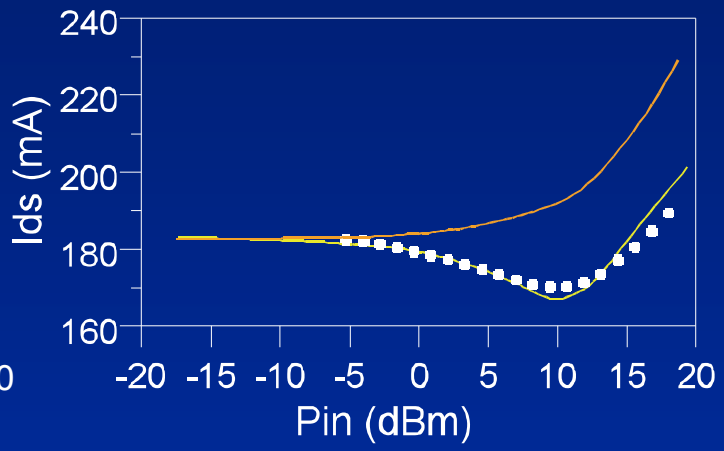
➔ PAE better reproduced

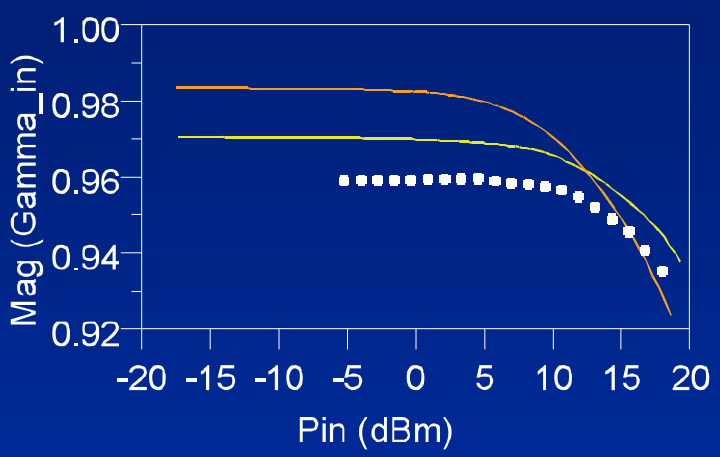
Load-pull validation @ 10 GHz

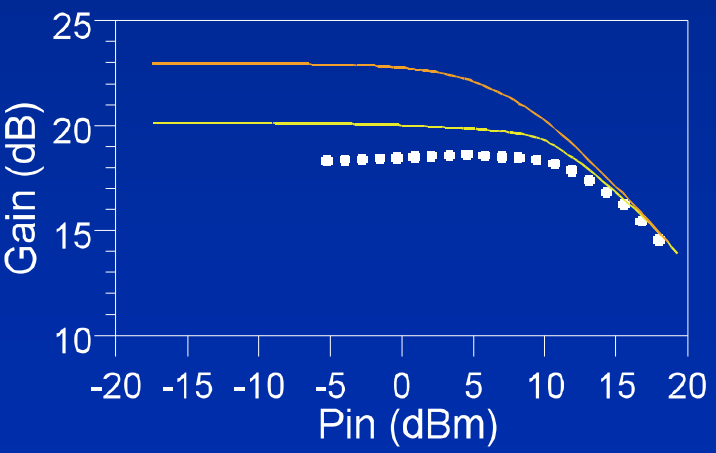
Impact of traps modeling on simulations on high VSWR

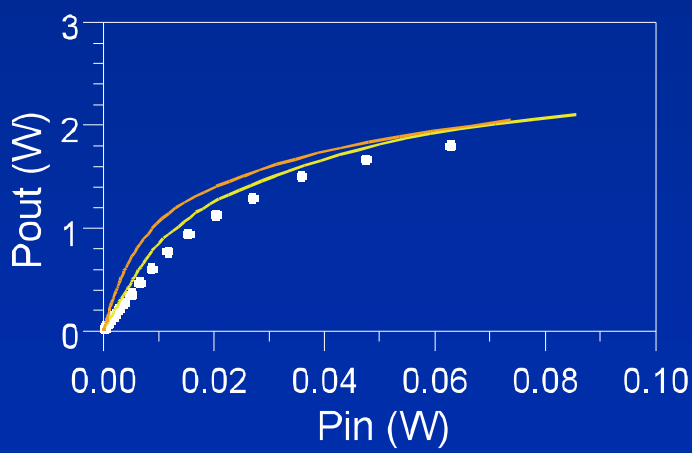
Example:Measurement on Z=13.4+j29 (VSWR=1.6)

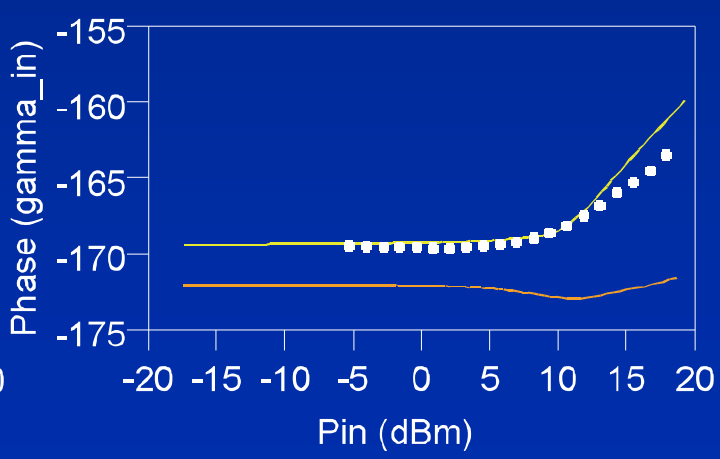








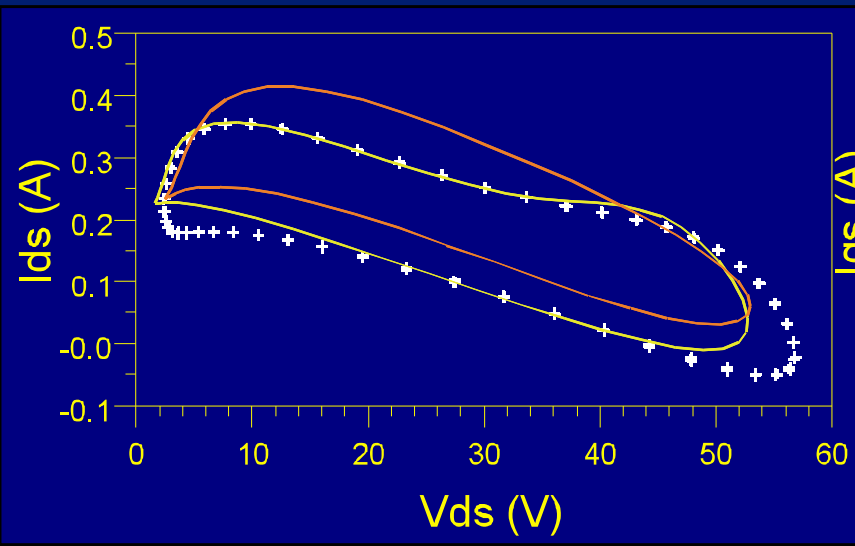


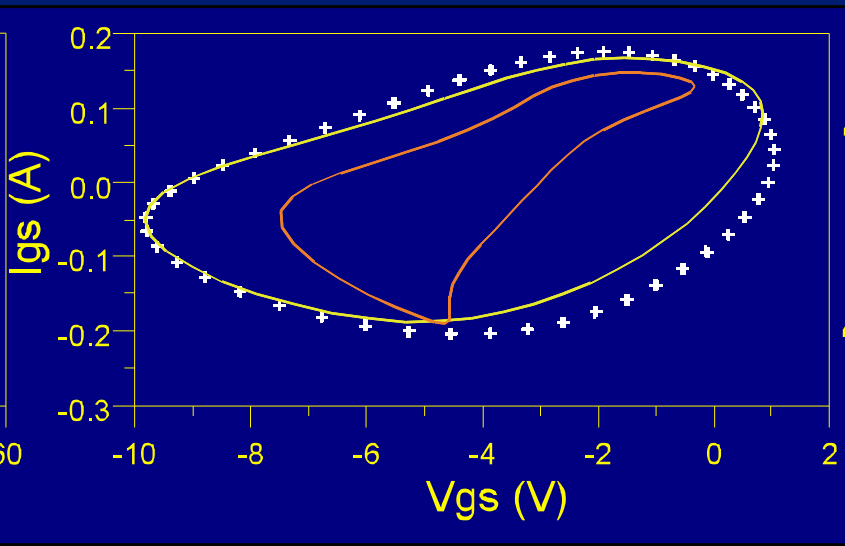


- Characteristics better reproduced (especially Gamma_in and Ids)

Validation on LSNA measurements @ 5 Ghz

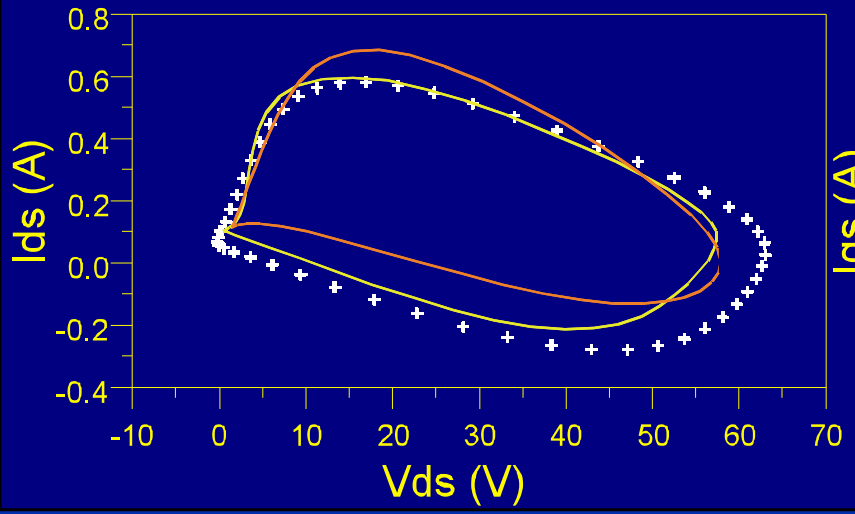
Time-domain measurements in class AB (25V, 200mA)

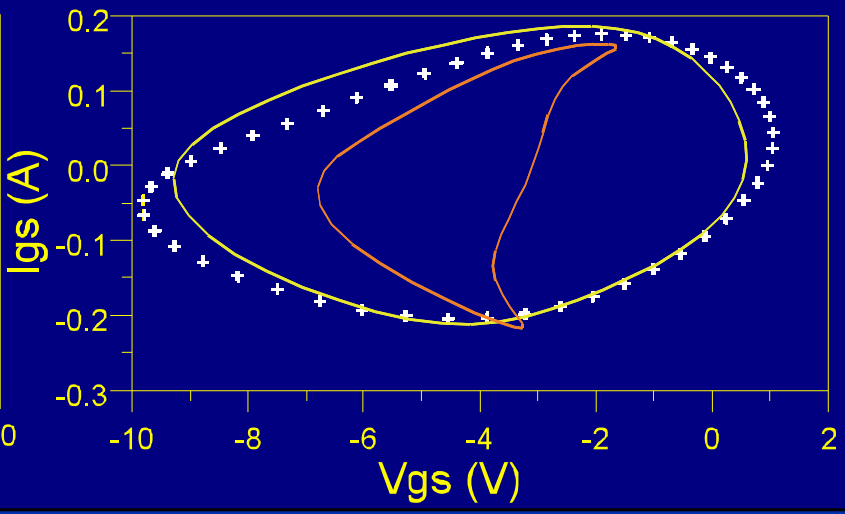




Z=130+j125 (VSWR=4)

4.6dB comp.





Z=27+j84 (VSWR=3.3)

7dB comp.

- Output current more realistic
- Strong impact on input cycles

Conclusions

- Modeling trapping effects allow reproducing better:

  -the pulsed IV curves versus the quiescent bias point.

  -the decreasing form of the output current form in large-signal

  -the large-signal measurements (larger range of Zload)

- Fast and easy extraction of the trapping model (1 measurement)
- Convergence of the models not affected, simulation times in H-Balance *x*1.5

Thank you for your attention

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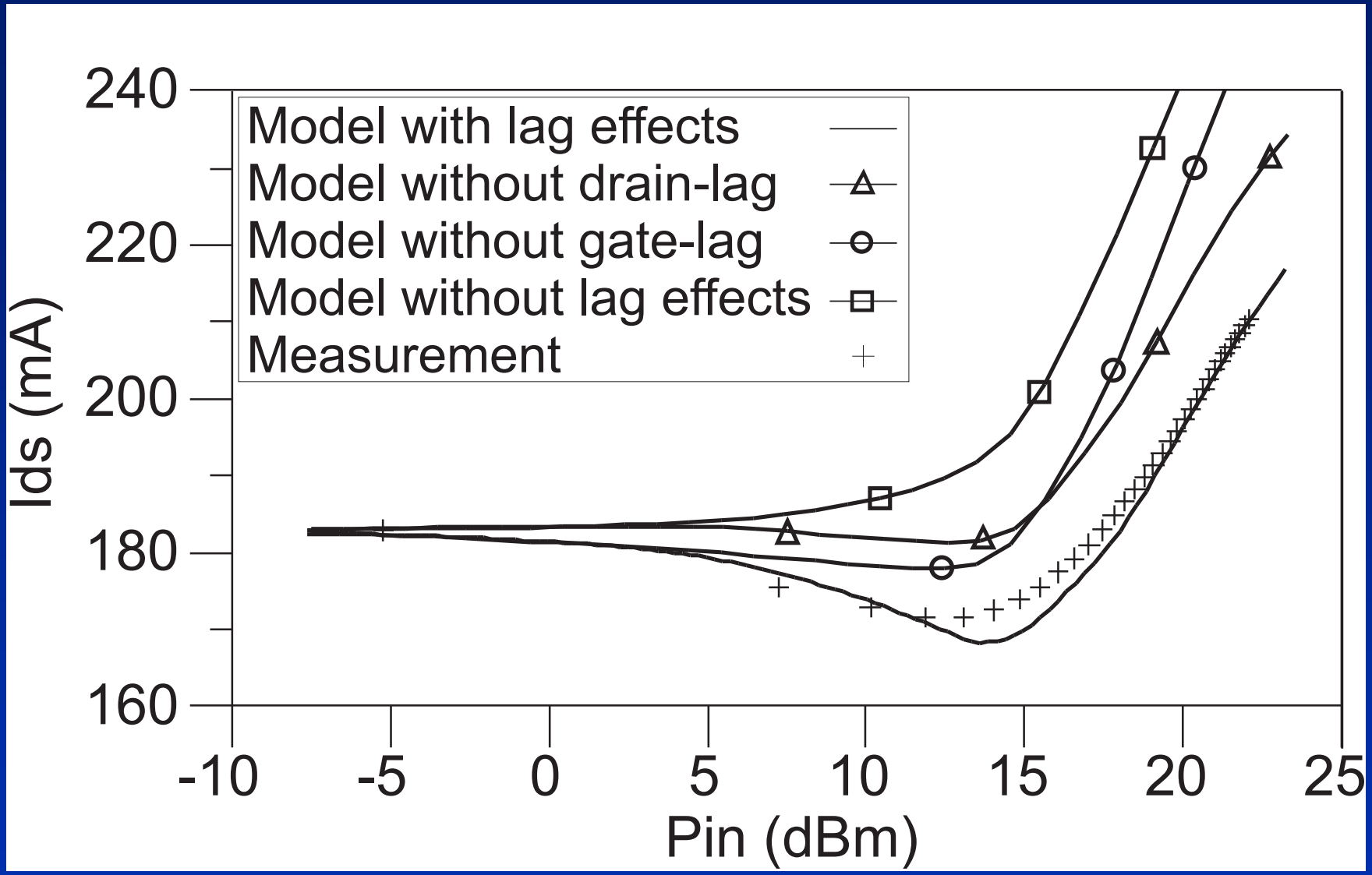
Model with lag effects
Model without drain-lag
Model without gate-lag
Model without lag effects
Measurement
Ids (mA)
240
220
200
180
160
-10
-5
0
5
10
15
20
25
Pin (dBm)