A Smart Load-Pull Method to Safely Reach Optimal Matching Impedances of Power Transistors

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Abstract — **This paper presents a new method to find optimal load impedances of power transistors with a VNA based Load-Pull measurement setup. Most of load pull setups find the optimal load impedance of a device under test (DUT) for a given available input power. If the optimal impedance must satisfy a trade off between several parameters, such as gain compression or power added efficiency, the measurement procedure may become very time consuming. Our method automatically generates a behavioral model of the DUT. Crossing-informations from this model and measurements lead us to the good impedance optimum with a limited number of iterations.**

***Index Terms* — Impedance matching, microwave measurements, modeling, semiconductor device measurements.**

I. Introduction

The optimal design of microwave power circuits requires large signal characterization and nonlinear models of transistors. To reach this goals, load-pull characterizations of microwave power transistors are needed.

Basically, powermeter based or VNA based load-pull systems using computer controlled tuners generate constant output power load impedance location of a device under test at a constant available power. However, the problem is that the input impedance of the transistor varies versus the load impedance and the available power. As a consequence, the input power (really driving the device) is modified and the nonlinear behavior of this device is also modified. Consequently, the behavior and the performances of the transistor cannot be obviously and accurately compared for 2 differents load impedance. This is particularly problematic if the desired comparison criterium is the gain compression.

An automatic available power control loop can be implemented in the algorithm controlling the load-pull set-up. The measurement time cost is increased but remains acceptable. Nevertheless, the optimal load impedance moves versus input power level. As a consequence, an input power sweep must be achieved for a great number of load impedances. Characterizing the ultimate power performances of a semiconductor technology either for nonlinear device modeling or for robust circuit design is important to find a set of load impedances for which the device exibits a fixed gain compression (usualy 2 or 3 dB). This kind of charaterization requires sweeping available power measurements, in order to determine the small signal gain, for a great number of load impedances. Then, optimum match can be deduced from analysis of an a posteriori processing of many measurement data.

This paper presents a new method which enables to find, by a rigourous way, optimal matching conditions with a limited number of measurements. It will be illustrated by the search for an optimal load impedance having to respect several antagonist criteria. This method is based on the automated generation and exploitation of a preliminary behavioral model of the transistor under test. The use of this behavioral model let us focus on the load impedance location close to the searched optimum. A predictive algorithm, based on a recursive process including both the automated generation of the model, the results obtained with it, and the measurement verification measurement is explained. The number of iteration is deduced from the model accuracy. In our measurement examples, the optimum will be found with only two iterations.

II. VNA Based Load-Pull Measurements

The measurement setup is based on the use of a VNA and a computer controlled tuner. In this part, our setup is described, and then we warn the reader on the measured waves we have to consider in this work : the pseudo wave normalized on an arbitrary complex impedance.

A. The measurement setup

The measurement setup is given in figure 1. This bench is based on the use of a VNA having pulse operation mode [1]. The bench has been automated with Scilab [2]. The calibration procedure includes a classical 12 error terms for power wave ratio corrections and a power calibration at the fundamental operating frequency. The load impedance can be controlled either with an automatic tuner or an active loop.

The calibration and the measurements here require a full four channels VNA. The power calibration enables for each measured point, the simultaneous measurement of the four calibrated absolute power waves : a1, b1, a2 and b2 at the fundamental operating frequency.

Most actual commercial VNAs enable receiver mode operation in order to access those four waves such as the Agilent PNA E8364B [3], the Anritsu 37100C [4] or the Rohde & Scharz ZVA [5].

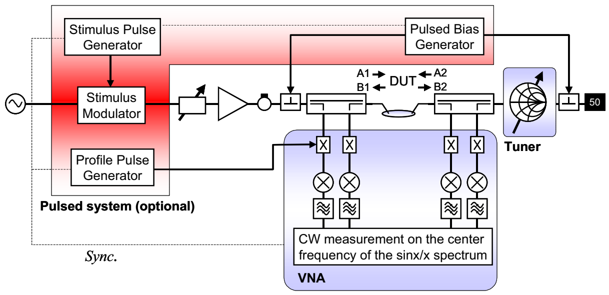

Fig. 1.The VNA based Load-Pull measurement setup.

B. Power waves or pseudo waves ?

Usually, people works with power wave [6] defined as follow :

$$a_i = \frac{v_i + Z_{ref}.i_i}{2.\sqrt{\Re\{Z_{ref}\}}} \text{ and } b_i = \frac{v_i - Z^*_{ref}.i_i}{2.\sqrt{\Re\{Z_{ref}\}}} \quad (1)$$

But this formulation can be used only if the reference impedance is real. Thus another kind of wave has been introduced in [7] such as :

$$a_i = \frac{v_i + Z_{ref}.i_i}{2} \text{ and } b_i = \frac{v_i - Z_{ref}.i_i}{2} \quad (2)$$

Those voltage waves, also called pseudo-wave enable the use of complex reference impedance [7] [8] [9]. It allows us to vanish mathematically the a_2 wave on an arbitrary loading impedance equal to the reference impedance. This property will be used in the modeling part of this paper.

Considering a 50 ohms environment, there is no difference between the use of power waves or pseudo waves for wave's ratio measurements. The type of measured waves is defined during the power calibration which enables the relationship between a and b waves and the measured power with a power meter. In our measurement setup, we consider 50 ohm power waves. We have to transform our measured waves before starting any modelling process.

III. AUTOMATED BEHAVIORAL MODELING OF THE DUT

The main idea of this paper consists on automatically generating a preliminary model of the transistor under test. This model uses the large signal S parameter formalism introduced in [10] but limited here to the measured fundamental operating frequency.

A. From B-waves expansion to large signal S parameters

Let us consider the describing function of the transistor under test b-waves :

$$b_i = F^i_{NL}\left(\Re\{a_1\},\Im\{a_1\},\Re\{a_2\},\Im\{a_2\}\right) \quad (3)$$

where $\Re$ and $\Im$ denote respectively the real and the imaginary part. According to :

$$\Re\{a_i\} = \frac{a_i + a_i^*}{2} \text{ and } \Im\{a_i\} = \frac{a_i - a_i^*}{2.j} \quad (4)$$

Equation (3) can be written as following :

$$b_i = F^i_{NL}\left(a_1, a_1^*, a_2, a_2^*\right) \quad (5)$$

All measurements are done at a single CW frequency. Concerning measured data, first at all we will have to transform our 50 ohm power waves to an arbitrary impedance pseudo waves. Then, assuming that the transistor under test looks like a time invariant system, we normalize the phase of the four waves such as a1 becomes real.

Therefore,

$$b_i = F^i_{NL}\left(|a_1|,\Re\{a_2\},\Im\{a_2\}\right) \quad (6)$$

Our measured data do not include neither modulated signal nor source-pull characterization. Thus, we neglect the a_1 derivative in (6) and (7). Normalizing the waves with an arbitrary impedance vanish a_2 for the selected impedance. The first order Taylor expansion of the describing function around a_2=0 is a MacLaurin expansion and lead us to :

$$\begin{aligned} b_i\left(|a_1|,\Re\{a_2\},\Im\{a_2\}\right) &= F_{NL\,i}\left(|a_1|,0,0\right) \\ &+ \frac{\partial\left\{F_{NL\,i}\left(|a_1|,0,0\right)\right\}}{\partial\left\{\Re\{a_2\}\right\}}.\Re\{a_2\} \\ &+ \frac{\partial\left\{F_{NL\,i}\left(|a_1|,0,0\right)\right\}}{\partial\left\{\Im\{a_2\}\right\}}.\Im\{a_2\} \end{aligned} \quad (7)$$

It defines kernels of the b-wave describing function such as :

$$\begin{aligned} b_i\left(|a_1|\right)\Big|_{a2\approx 0} &= H^0_i\left(|a_1|\right) + H^{1R}_i\left(|a_1|\right).\Re\{a_2\} \\ &+ H^{1I}_i\left(|a_1|\right).\Im\{a_2\} \end{aligned} \quad (8)$$

we can write (8) as :

$$b_i\left(|a_1|\right)\Big|_{a2\approx 0} = S_{i1}\left(|a_1|\right).a_1 + S_{i2}\left(|a_1|\right).a_2 + T_{i2}\left(|a_1|\right).a_2^* \quad (9)$$

This formulation was used in [11].

B. MacLaurin first order expansion for DC current

During load-pull characterization, DC voltage are fixed. Therefore, we have to model the behavior of the DC current accounting the RF available power (a1 level) and the load impedance mismatch (a2 value). The model principle is similar to (8) and leads us to :

$$\begin{aligned} I_{DC\,i}\left(|a_1|\right)\Big|_{a2\approx 0} &= J^0_i\left(|a_1|\right) + J^{1R}_i\left(|a_1|\right).\Re\{a_2\} \\ &+ J^{1I}_i\left(|a_1|\right).\Im\{a_2\} \end{aligned} \quad (10)$$

We have to identify the J kernels as we have done for the RF part. Notice that in the bias model, all the variables are real.

C. S-parameters and current kernels extraction

A preliminary model of the transistor under test can be obtained from wave's measurements during a power sweep and, at least, 3 different impedances. The use of 3 load impedances implies exact model results for those identifing impedances. Considering more than 3 identification impedances implies a least square on the kernels values.

The first impedance will be our reference impedance. Thus the a2 wave will be vanished for this impedance and it justify the MacLaurin expansion. Once the first impedance mesurement is done (a complete power sweep up to 3 or 4 dB gain compression), all the next waves measurements matched on, at least, two other loading impedances, will be transformed into pseudo waves normalized on the refrence impedance (the first impedance). Those matching impedances are located on a constant VSWR circle such as :

$$\left|a_2^k\right| = \left|b_2^k\right| \cdot \frac{\text{VSWR-1}}{\text{VSWR+1}} \tag{11}$$

k is the number of matching impedance. Pratically, we select a VSWR between 1.3 and 1.6.

For three impedances measurements, the selected argument values of a2 are 0° and 90° (orthogonality is well suited for the system identification) as explained in [10]. If we desire much more impedances (N) for the identification, one can choose :

$$\text{Arg}\left(a_2^k\right) = k.360° / N \tag{12}$$

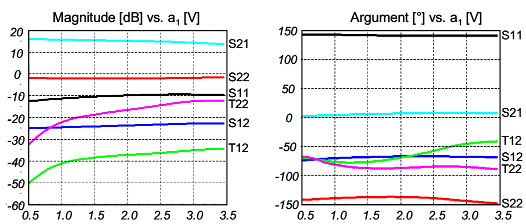

Fig. 2. Large Signal S parameters extracted with 3 loading impedances at 1.2575 GHz. The normalization impedance is Zref = 48.3+j.5.4. Location of the 3 impedances used for extraction is illustrated on figure 3.

Considering all the impedance measurements, model kernels are deduced for each value of a1 by inverting the linear system written in (9) and (10).

Figure 2 illustrates large signal [S] parameters, normalized at Zref=48.3+j.5.4, measured on a HBT Gaas transistor (those parameters will be used in the "first step model" described in the fourth part of this paper). Notice that the T terms can be neglected while a1 goes to 0. The small signal transistor model can be considered as a classical S parameters values.

D. Checking the model's behavior

Once the model is identified, we have to simulate it. Our first order MacLaurin expansion is a linearization of the transistor under test. The relations are linear, so we don't need any balance algorithm in order to find out the corresponding four waves. Indeed, from :

$$b_2 = S_{21}.a_1 + S_{22}.a_2 + T_{22}.a_2^* \tag{13}$$

we can deduce :

$$b_2 = \frac{\left[\left(1 - S_{22}^*.\Gamma_{Load}^*\right).S_{21}\right].a_1 + \left[T_{22}.\Gamma_{Load}{}^*.S_{21}^*\right].a_1^*}{\left(1 - S_{22}^*.\Gamma_{Load}^*\right).\left(1 - S_{22}.\Gamma_{Load}\right) - \left|T_{22}\right|^2.\left|\Gamma_{Load}\right|^2} \tag{14}$$

One can notice that the formula fits the well known relation in the linear case ($T_{ij} = 0$) where :

$$b_2 = \frac{S_{21}.a_1}{\left(1 - S_{22}.\Gamma_{Load}\right)} \tag{15}$$

The two other waves are calculated as :

$$a_2 = \Gamma_{Load}.b_2 \quad \text{and} \quad b_1 = S_{11}.a_1 + S_{12}.a_2 + T_{12}.a_2^* \tag{16}$$

IV. Measurement Examples

This part describes our new method with an example. We have to find the best load impedance of a transistor in order to reach an output power (Pout) higher than 3500mW, a dissipated power (Pdissip) lower than 1400 mW and a maximum power added efficiency (PAE).

A. First step model

Measurements start with at least 3 different matching conditions (numbered 1 to 3 in figure 3) in order to generate a preliminary model : the first step model. It enables to let us focus on the area of interest on the smith chart.

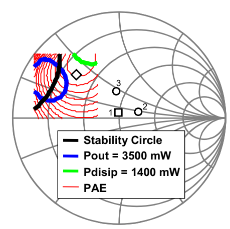

Fig. 3. Fifty ohms smith chart representation. The first step model is identified around 50 ohms with 3 load impedances. The reference impedance used for the normalization (square : Zref = 48.3+j.5.4) and two others which are orthogonals and located on a constant VSWR=1.35 circle.

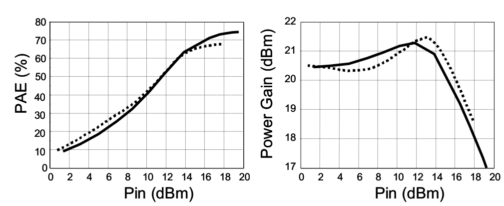

Fig. 4. Measurements (solid) and "first step model" (dashed) comparison for Zload = 14.7+j.18.49. This model is not accurate enough for optimal matching search. A 'second step model' will be automatically generated.

Once the area of interest has been located, we can check the accuracy of our 'first step model' in this area. On figure 3, the diamond corresponds to the next loading impedance measurement in order to compare the 'first step model' with the measurements.

Then, if the accuracy is not sufficient (as show on figure 4), we have to begin again the modeling process but with impedances located into the area of interrest. This is the second iteration of our predictive algorithm, which lead us to a 'second step model'.

B. Second step model

The second step model is identified in the area of interest using measurements on six load impedances in order to increase the model accuracy within the VSWR=1.35 circle. For this purpose, the model is a 2^{nd} order MacLaurin expansion based on (7) and (11). The optimal load impedance can be found from this second step model as illustrated on figure 5.

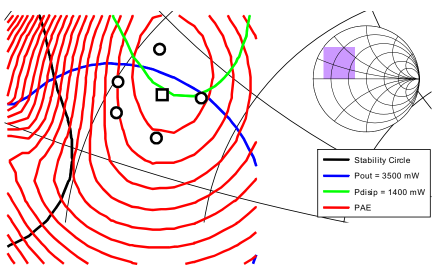

Fig. 5. Fifty ohms smith chart representation. PAE contour lines and constraint lines for output power (Pout) and dissipated power (Pdissip) obtained from the second step model. This model has been identified with the normalization impedance Zref= 14.70+j.18.49 (square) and 5 maching impedances (circles) located on the constant VSWR=1.35 circle.

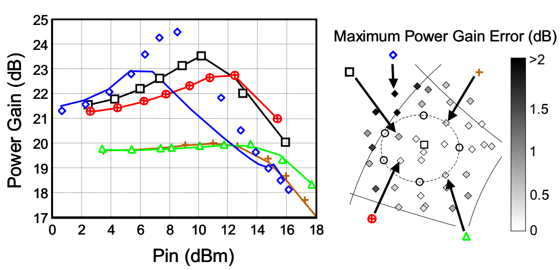

Fig. 6. Power gain curve (left) and maximum gain error between model and measurement accounting the loading impedance up to 3 dB compression gain (right). On the left, measurements (solid) and model (dots) power gain comparison for non identified impedances. If the model optimum loading impedance is located within the identification constant VSWR circle (here 1.35 around Zref=14.70+j.18.49), we don't need any more measurement to locate it more accurately.

A large number of measurements curves had been done in order to overview the second step model accuracy. Results are illustrated on figure 6. The worst matching prediction, located outer the constant VSWR identification circle is included in the power gain curves. Notice the large power gain value is due to the close stability circle.

V. Conclusion

A new load-pull characterization method, which enables to reduce the number of measurements iterations to find the optimal load impedance within targeted operating conditions and defined constraints, has been presented. This method uses the large signal S parameter formalism truncated at a single frequency. It automatically generates a preliminary behavioral model of the transistor under test. This novel approach does not require any simultor or balanced algorithm and can be easily implemented in commercial VNAs in order to perform load-pull measurements with an automated tuner.

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Outline

- Introduction
- The load-pull measurement setup
- Large signal S parameters Mc Laurin expansion for the DUT modeling
- Application : a predictive algorithm to reach optimal matching impedance
- Conclusion

Motivation

- What is THE optimal load impedance ?
  - Pout max @ Pav, Pin or Gcomp fixed
  - Several parameters trade off

    (In this paper : Pout>3500mW / Pdisip<1400mW / PAE=max)

- Reduce the number of load impedance measurement
  - Iterative method for Pout max @ fixed Pav
  - Predictive algorithm based on a automated behavioral modeling

Pros & Cons

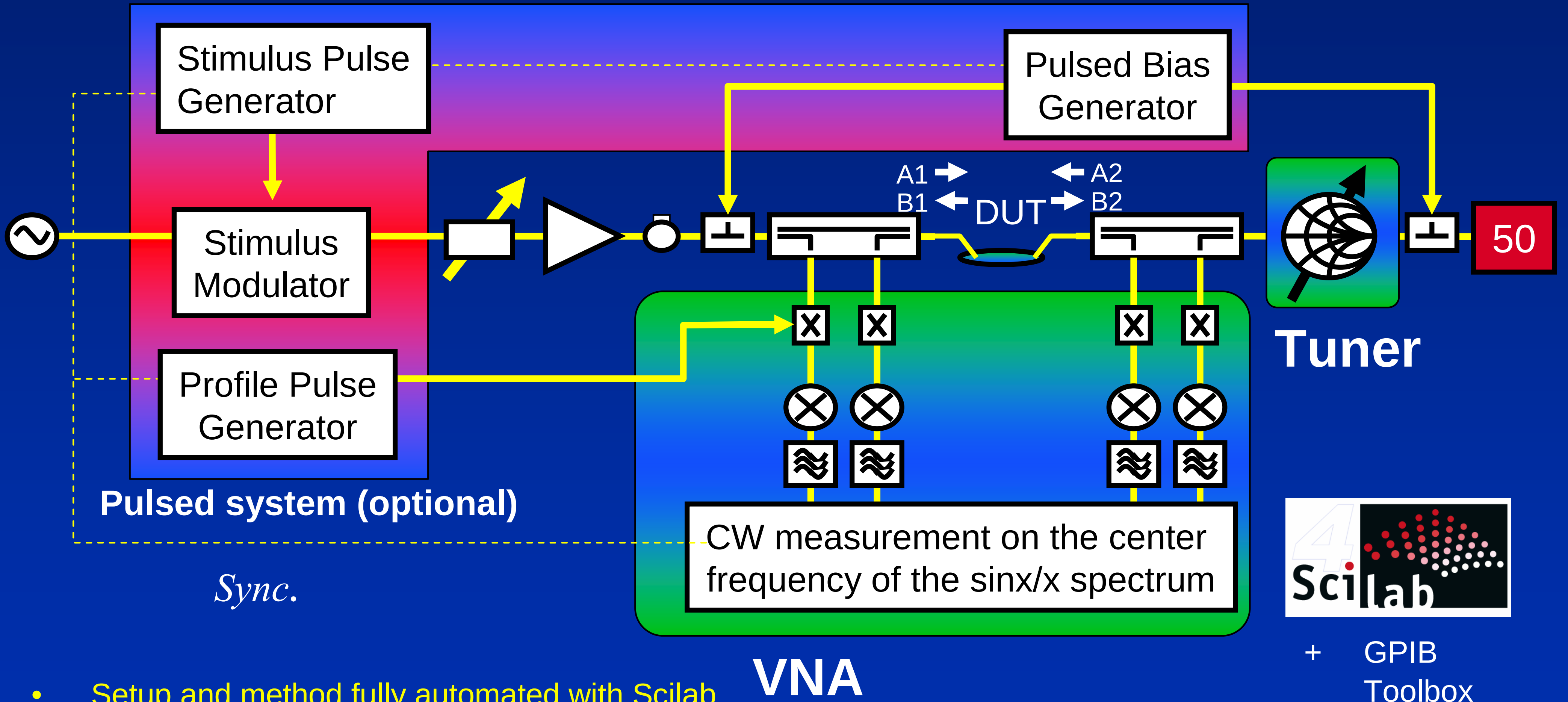
- Pros for the “Smart Load-Pull Method”
  - Takes the advantage of the Nonlinear S parameters analysis
  - Only 3 or 6 impedance measurements are enough to get a good accuracy on the DUT’s behavior up to VSWR=1.6
  - Usable for all commercially available 4 couplers VNAs

- Cons for the “Smart Load-Pull Method”
  - Requires a 4 couplers VNA
  - Not usable for high VSWR
  - The approach presented here is limited to 1 frequency CW LP measurements. Measurements of the phases (LSNA) is required to take into account harmonics behavior (PHD model).

1. Load-Pull Measurement Setup

1.1 Overview

One CW frequency measurements



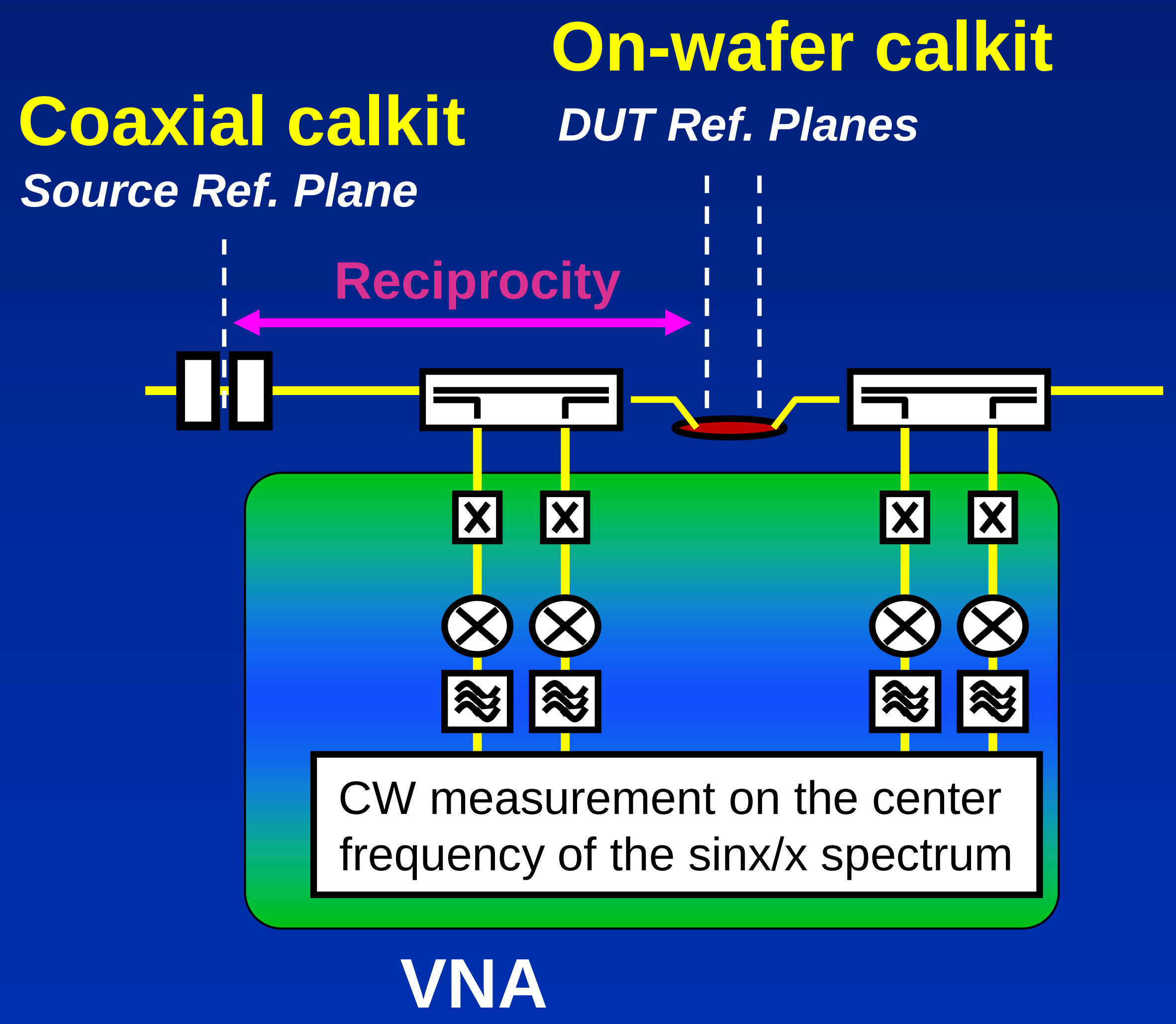
- Setup and method fully automated with Scilab (free open-source clone of Matlab : www.scilab.org)
- Our application was tested with a Wiltron 360B and a Focus iTuner

+ GPIB Toolbox
+ Winsocket Toolbox

1. Load-Pull Measurement Setup

1.2 Calibration

- On-wafer ref. plane
  - Classical 12 error terms calibration procedure (SOLT, LRM or TRL)
  - → Enables wave ratio measurements (S param)
- Coaxial ref. plane
  - 1 coaxial port 4 error terms method
  - 3 terms comes from a SOL method
  - 1 term come from the power calibration (standard = powermeter)
  - Assuming reciprocity implies the knowledge the e10 error term within the on-wafer calibration



1. Load-Pull Measurement Setup

1.3 Waves Measurements

Power calibration let us assume a definition of the measured waves

		Power calibration	Zref
Power-waves (Kurokawa)	$a_i = \frac{v_i + Z_{ref}^{*}.i_i}{2.\sqrt{\Re\{Z_{ref}\}}}$ $b_i = \frac{v_i - Z_{ref}^{*}.i_i}{2.\sqrt{\Re\{Z_{ref}\}}}$	Power (50 ohms)	Real
Voltage-waves	$a_i = \frac{v_i + Z_{ref}.i_i}{2}$ $b_i = \frac{v_i - Z_{ref}.i_i}{2}$	Voltage (50 ohms)	Complex

The measured and corrected quantities are V_i and I_i in this paper.

We can use any wave definition according to the definitions just above.

Our “Smart Load-Pull Method” requires a complex Zref, thus Voltage wave formulation will be use in the modeling part.

2. Modeling of the DUT

2.1 Fundamentals

Arbitrary

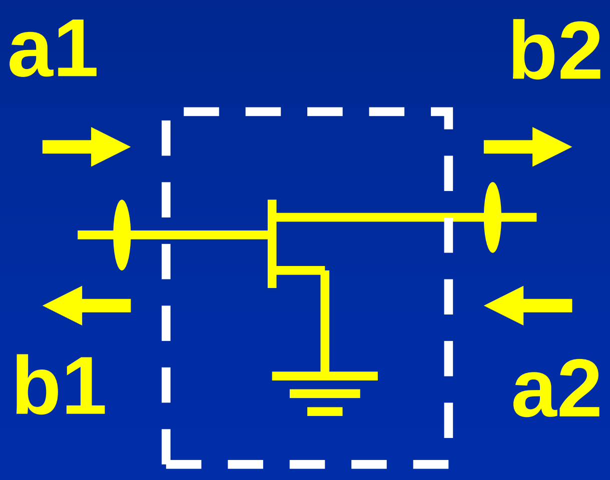
Z_{ref}

Measurements

$v_i \quad i_i$

$$a_i = \frac{v_i + Z_{ref}.i_i}{2}$$

$$b_i = \frac{v_i - Z_{ref}.i_i}{2}$$



1. Phase normalization

Each wave is multiplied by

$$e^{-j.Arg\{a_1\}}$$

→ a1 becomes real

2. Relationship

$$b_i = f_{NL}(a_1, a_2)$$

Mc Laurin expansion ($a_2 \approx 0$)

2. Modeling of the DUT

2.2 Mc Laurin Expansion for RF

$$b_i = f_{NL}\left(\Re\{a_1\},\Im\{a_1\},\Re\{a_2\},\Im\{a_2\}\right)$$

↓ ***a_1 = real & $a_2 \approx 0$***

First Order

$$b_i = f_{NL}\left(|a_1|,\Re\{a_2\},\Im\{a_2\}\right) \longrightarrow b_i = H_i^0(|a_1|) + H_i^{1R}(|a_1|).\Re(a_2) + H_i^{1I}(|a_1|).\Im(a_2)$$

or

$$b_i = f_{NL}\left(|a_1|,a_2,a_2^*\right) \longrightarrow b_i = S_{i1}(|a_1|).a_1 + S_{i2}(|a_1|).a_2 + T_{i2}(|a_1|).a_2^*$$

→ **3 independent measurements required**

S parameter-like expression

Second Order

$$b_i = f_{NL}\left(|a_1|,\Re\{a_2\},\Im\{a_2\},(\Re\{a_2\})^2,(\Im\{a_2\})^2,(\Re\{a_2\}\Im\{a_2\})\right)$$

$$b_i = H_i^0(|a_1|) + H_i^{1R}(|a_1|).\Re(a_2) + H_i^{1I}(|a_1|).\Im(a_2) + H_i^{2R}(|a_1|).[\Re(a_2)]^2 + H_i^{2I}(|a_1|).[\Im(a_2)]^2 + H_i^{2RI}(|a_1|).[\Re(a_2).\Im(a_2)]$$

or

$$b_i = f_{NL}\left(|a_1|,a_2,a_2^*,a_2^2,a_2^{*2},a_2.a_2^*\right)$$

$$b_i = S_{i1}(|a_1|).a_1 + S_{i2}(|a_1|).a_2 + T_{i2}(|a_1|).a_2^* + T_{i2}'(|a_1|).a_2^2 + T_{i2}''(|a_1|).a_2^{*2} + T_{i2}'''(|a_1|).a_2.a_2^*$$

→ **6 independent measurements required**

2. Modeling of the DUT

2.3 Mc Laurin Expansion for DC

About the biases…

- Constant DC voltages
- DC currents fitted with Mc Laurin expansion

First Order

$$I_i = f_{NL}\left(|a_1|, \Re\{a_2\}, \Im\{a_2\}\right) \longrightarrow I_i = J_i^0\left(|a_1|\right) + J_i^{1R}\left(|a_1|\right).\Re\left(a_2\right) + J_i^{1I}\left(|a_1|\right).\Im\left(a_2\right)$$

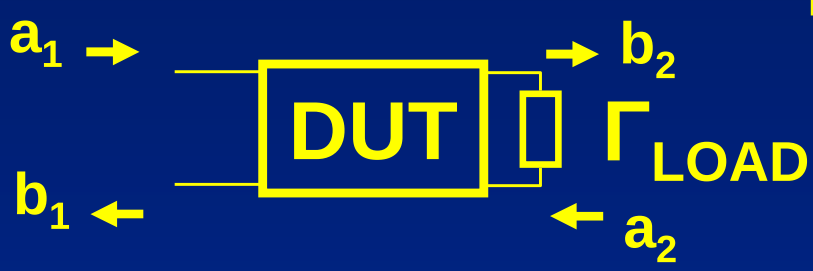
Second Order

$$I_i = f_{NL}\left(|a_1|, \Re\{a_2\}, \Im\{a_2\}, \left(\Re\{a_2\}\right)^2, \left(\Im\{a_2\}\right)^2, \left(\Re\{a_2\}.\Im\{a_2\}\right)\right)$$

$$I_i = J_i^0\left(|a_1|\right) + J_i^{1R}\left(|a_1|\right).\Re\left(a_2\right) + J_i^{1I}\left(|a_1|\right).\Im\left(a_2\right) + J_i^{2R}\left(|a_1|\right).\left[\Re\left(a_2\right)\right]^2 + J_i^{2I}\left(|a_1|\right).\left[\Im\left(a_2\right)\right]^2 + J_i^{2RI}\left(|a_1|\right).\left[\Re\left(a_2\right).\Im\left(a_2\right)\right]$$

2. Modeling of the DUT

2.4 How to extract the model parameters

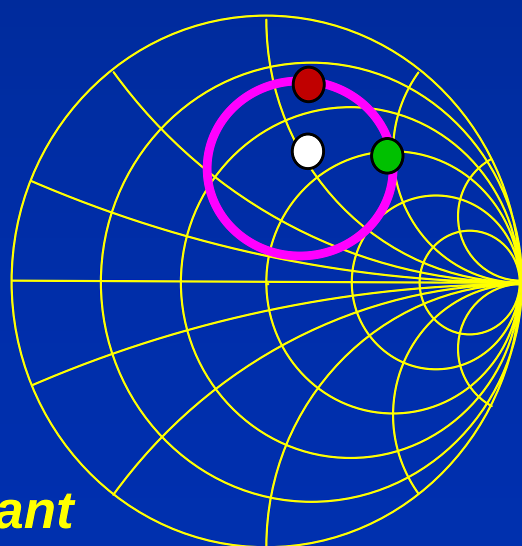


- Invert a linear system
- Maximize the rank of the system

1st order

$$b_1 = S_{11}.a_1 + S_{12}.a_2 + T_{12}.a_2^*$$
$$b_2 = S_{21}.a_1 + S_{22}.a_2 + T_{22}.a_2^*$$

- $a_2=0$ (Zref)
- $a_2=k$
- $a_2=k.\exp(90°)$
- $abs(a_2)=k$

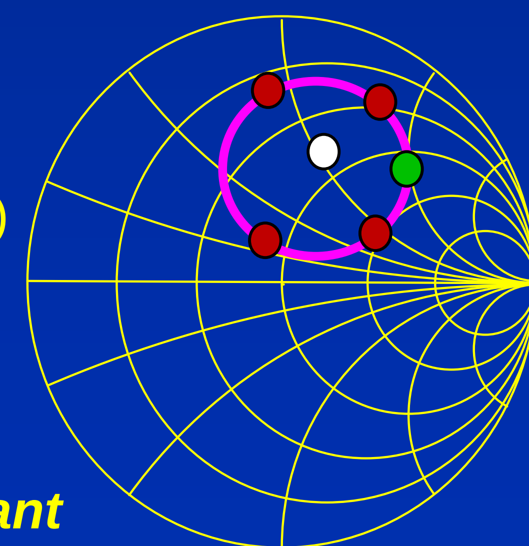


@abs(b_2)=constant

2nd order

$$b_1 = S_{11}.a_1 + S_{12}.a_2 + T_{12}.a_2^* + T'_{12}.a_2^2 + T''_{12}.a_2^{*2} + T'''_{12}.a_2.a_2^*$$
$$b_2 = S_{21}.a_1 + S_{22}.a_2 + T_{22}.a_2^* + T'_{22}.a_2^2 + T''_{22}.a_2^{*2} + T'''_{22}.a_2.a_2^*$$

- $a_2=0$ (Zref)
- $a_2=k$
- $a_2=k.\exp(i.72°)$
- $abs(a_2)=k$



@abs(b_2)=constant

2. Modeling of the DUT

2.5 Using the model…

$$b_1 = S_{11}.a_1 + S_{12}.a_2 + T_{12}.a_2^*$$

$$b_2 = S_{21}.a_1 + S_{22}.a_2 + T_{22}.a_2^*$$

$$a_1, b_1, a_2, b_2 = f_{NL}(a_1, \Gamma_{LOAD})$$

Pin, Pout, PAE,…

$$I_{DC1}, I_{DC2} = f_{NL}(a_1, \Gamma_{LOAD})$$

Linear

$$a_1 = a_1$$

$$b_2 = \frac{S_{21}.a_1}{(1 - S_{22}.\Gamma_{LOAD})}$$

$$a_2 = \Gamma_{LOAD}.b_2$$

$$b_1 = S_{11}.a_1 + S_{12}.a_2$$

Nonlinear : order 1

$$a_1 = a_1$$

$$b_2 = \frac{(1 - S_{22}^*.\Gamma_{LOAD}^*).S_{21}.a_1 + (T_{22}.\Gamma_{LOAD}^*.S_{21}^*).a_1^*}{(1 - S_{22}^*.\Gamma_{LOAD}^*).(1 - S_{22}.\Gamma_{LOAD}) - |T_{22}|^2.|\Gamma_{Load}|^2}$$

$$a_2 = \Gamma_{LOAD}.b_2$$

$$b_1 = S_{11}.a_1 + S_{12}.a_2 + T_{12}.a_2^*$$

Nonlinear : order 2 or more

$$a_1 = a_1$$

$$b_2, a_2 = \ldots$$

$$b_1 = S_{11}.a_1 + S_{12}.a_2$$

b_2 and a_2 solved simultaneously with balancing algorithm like 'Newton-Raphson'

3. Application

Algorithm of the Smart load-pull

Repeat

1. Perform 3 or 6 impedance measurements
2. Calculate the model kernels
3. Calculate the optimal load impedance from the model and the user criteria
4. Measure the calculated optimal load impedance

Until model is accurate enough

- Limited to 1 CW Load-Pull measurements
- This program could be easily embedded into commercial VNAs

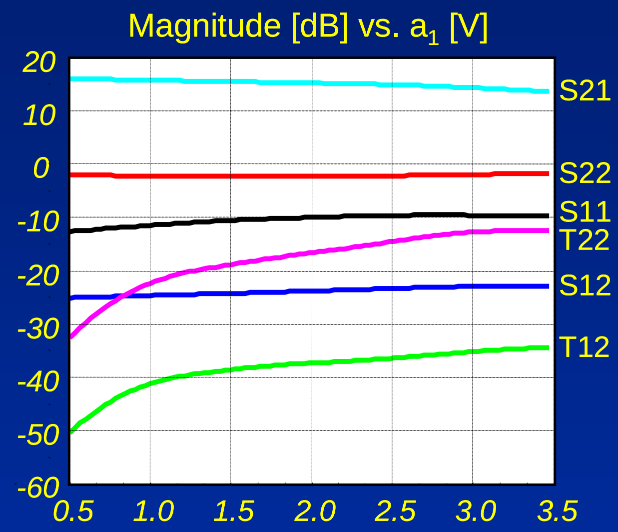
3. Application

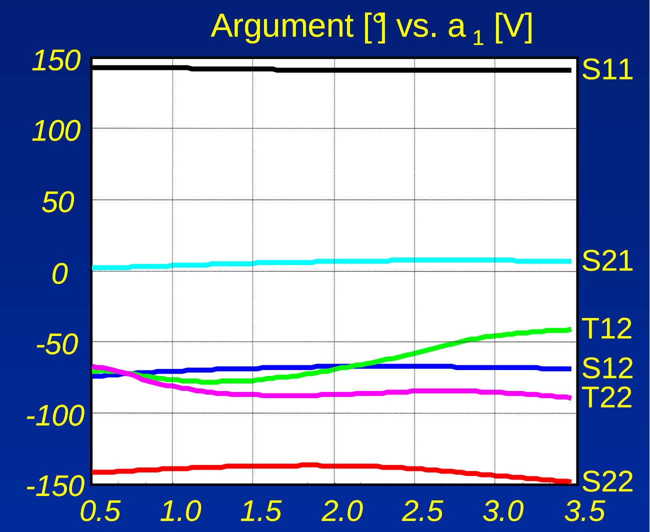
3.2 First Step Model

Example

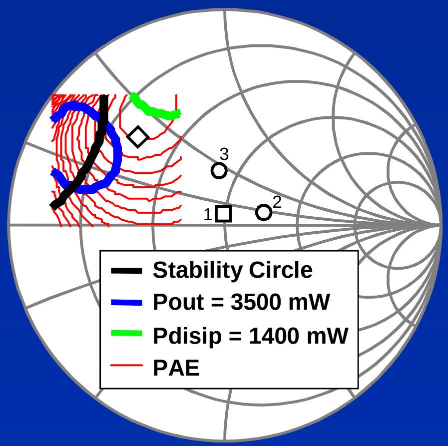
- Pout >3500 mW
- Pdissip <1400 mW
- PAE = MAX

Step one : first order model

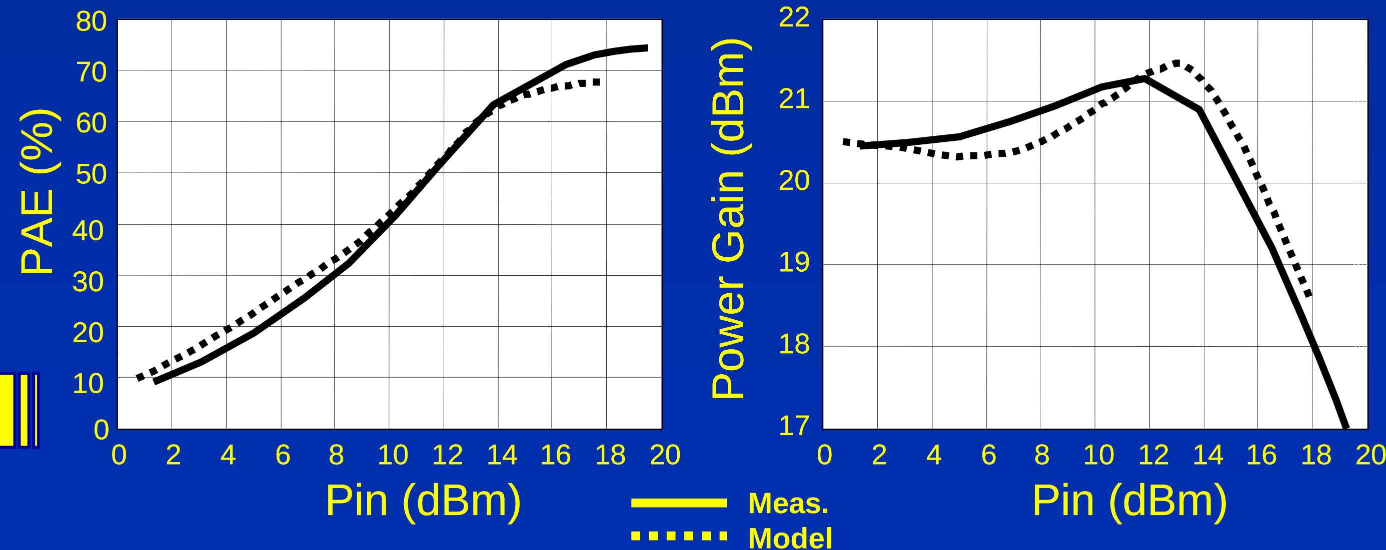




1. Measure 3 impedances (1 to 3)
2. Locate the area of interest
3. Compare measurement and model into this area



Vanishing a_2 @ Imp. #1 → Zref = 48+j.5



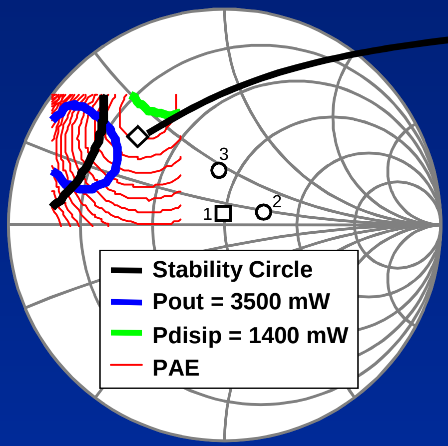
The first model is not accurate enough @ Z=14+j.18

3. Application

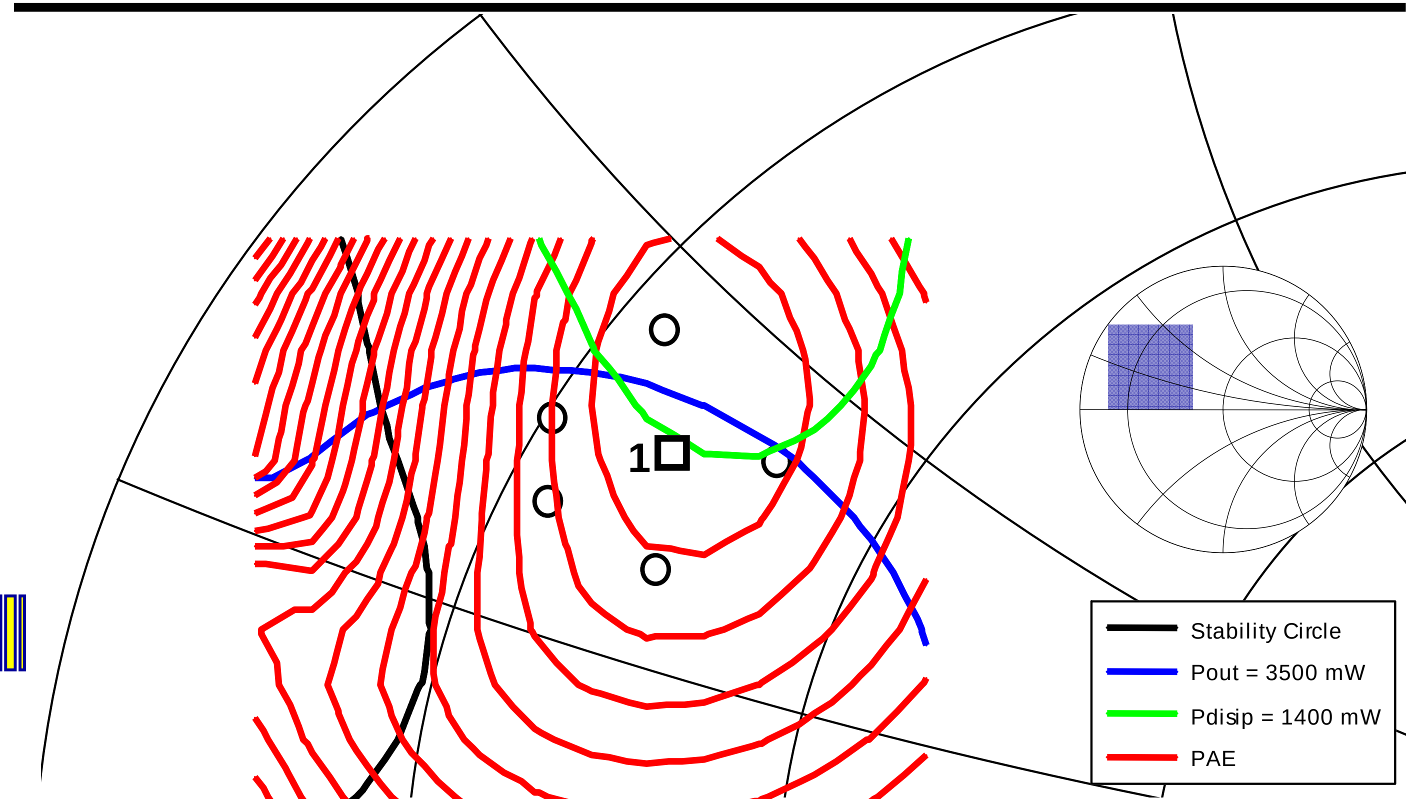
3.3 Second Step Model

Step two : second order model

Previous first order model
obtain with Zref ≈ 50 Ohms



Vanishing a_2 @ Imp. #1 → Zref = 14+j.18



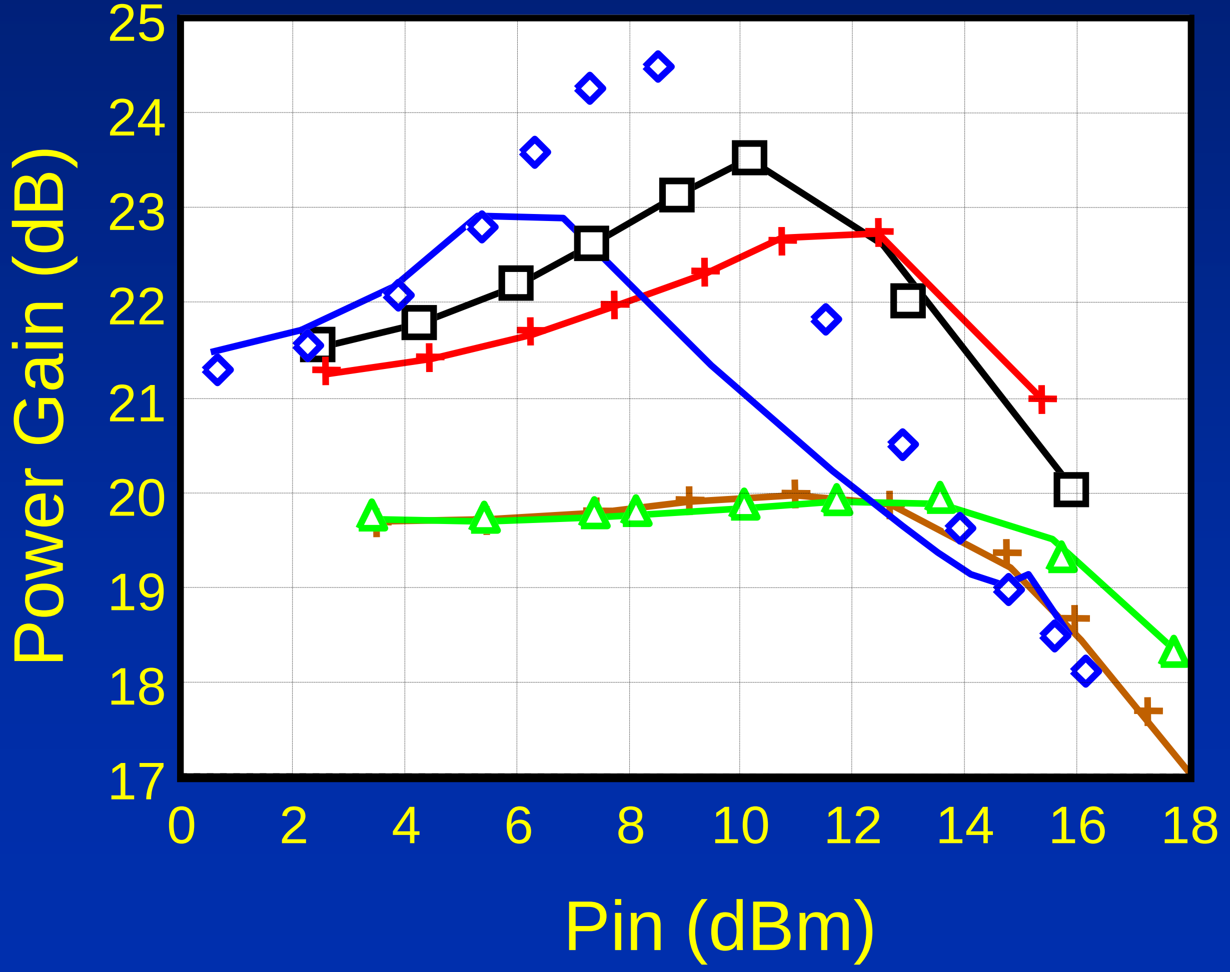
The best load impedance is located into the identification area.

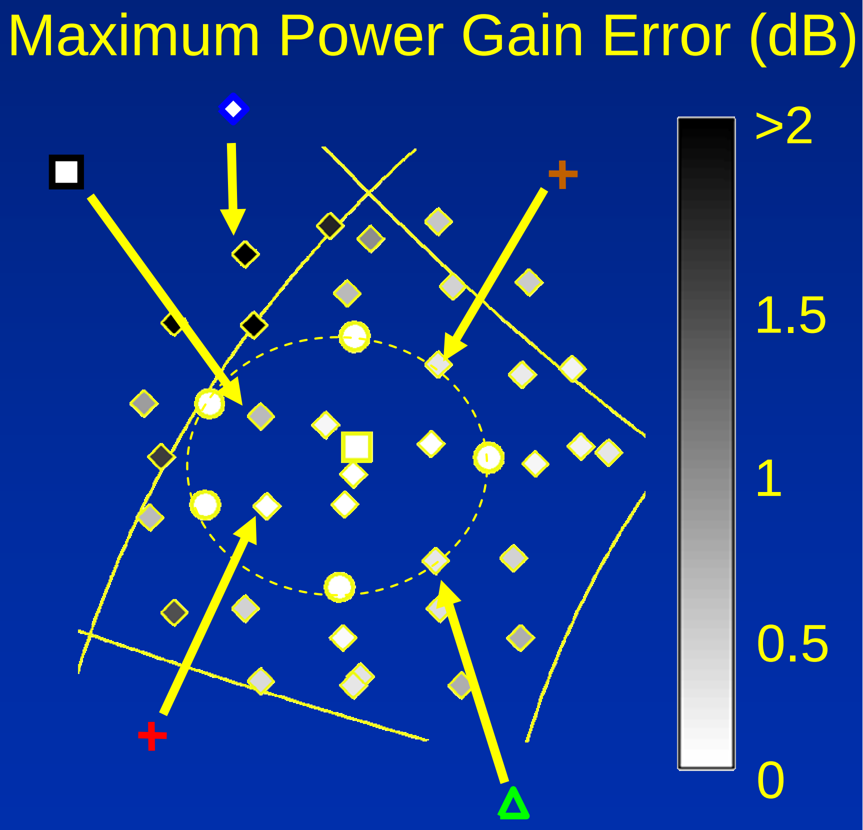
The model is accurate enough in order to estimate the best load impedance

The optimal load impedance For a complex criteria has been reached with 9 measurements

3. Application

3.4 Validity of the model





Conclusion

- A single tone CW load-pull measurement setup based on commercially available VNA was presented
- A new predictive algorithm for load pull measurements was presented and fully explained
- This algorithm take the advantage of Large signal S parameters and works like a “light version” of the PHD model
- The model do not need simulator and the complete method could be easily implemented in commercial VNA
- Considering harmonics implies the use of the complete PHD model and require a LSNA technology instead of a VNA one.