Design of GaN-based Balanced Cascode Cells for Wide-band Distributed Power Amplifier

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***Abstract*— This paper reports on the design of a cascode GaN HEMT cell dedicated to 4-18GHz flip-chip distributed power amplifier. The active device is a 8x50µm AlGaN/GaN HEMT grown on SiC substrate. The GaN-based die which integrates the active cascode cell and its matching elements is flip-chipped via electrical bumps onto an AlN substrate. The matching elements of the balanced cascode cell are composed of series capacitances on the gate of both transistors with additional resistances to insure stability and bias path. The series capacitor on the gate of the 1st transistor is added for the distributed amplifier optimisation while the series capacitor on the gate of the 2nd transistor is dedicated to the power balance of the cascode cell.**

I. INTRODUCTION

These last years, AlGaN/GaN high electron-mobility transistor (HEMT) technology has established itself as a strong contender for such applications because of its large electron velocity (>10^7 cm/s), wide bandgap (3.4eV), high breakdown voltage (> 50V for f_T =50GHz) and sheet carrier concentration (ηs >10^{13} cm^{-2}). Due to the superior electronic properties of the GaN material and the possibility to use SiC substrate demonstrating high thermal conductivity (3.5 W/cm.K), power densities as high as 30 W/mm @ 4GHz [1] as well as output power of 500W @ 1.5GHz [2] have already been achieved. More recently [3], 750 W output power of a packaged single-ended GaN-FET has been reported under pulsed conditions for L/S band applications. This paper addresses the design and optimization of a GaN HEMT cascode cell to be integrated in an optimized distributed power amplifier operating in the 4-18GHz frequency band [4].

II. BALANCED CASCODE CELL ON GAN DIE

The device considered in this study is a coplanar AlGaN/GaN HEMT processed on a SiC wafer on which a thin film of gallium nitride has been grown by MOCVD technique. The active device is a 400µm HEMT (8x50µm) of 0.15µm gate length. Pulsed (I-V) and pulsed (S) measurements have been performed to derive the non-linear model for power amplifier design [5].

The cascode cell presented in this paper is dedicated to the design and optimization of a 4-18GHz flip-chip distributed power amplifier based on GaN HEMT technology.

At first, the design procedure of the distributed power architecture requires to optimise the power performance of the cascode cell on the 4-18GHz bandwidth [6]. Indeed, the cascode configuration enables to ideally sum the output voltage Vds of each transistor at the same drain current so that to obtain twice the output power of a single transistor. Unfortunately, a classical cascode cell does not meet these conditions because the input voltage of the second transistor (Vgs2) limits the output voltage swing (Vds1) of the first transistor. To resolve this problem, an additional series capacitor Ca1 is placed on the gate of the second transistor T2 with the main purpose to fix the power matching between transistors (figure 1). This capacitor Ca1 and the input capacitance Cgs of the second transistor act as a frequency independent tension divider between Vds1 and Vgs2.

$$Ca1 = \frac{Cgs}{\left(\left|\frac{Vds1}{Vgs2}\right| - 1\right)}$$

This initial capacitor value of Ca1 is then optimised under large signal conditions using non-linear simulations of the cascode cell close to 1dB compression in order to synthesize the required ratio between the optimum large signal control voltages Vds(T1) and Vgs(T2).

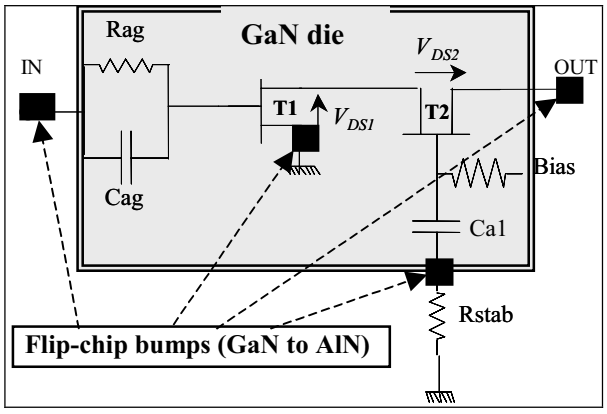

Fig. 1 Schematic of the power cascode cell (GaN die flip-chipped onto AlN)

This method has been applied to design the layout of an optimized balanced cascode cell integrating the two (8x50µm) GaN HEMTs.

At first, for a better transfer from transistor T1 to transistor T2, the drain pad of T1 has been connected to both part of the source metallisation of T2. The transistor T1 is grounded onto the AlN substrate through its air-bridge playing the role of an electrical bump. The balance capacitor Ca1 of 0.19pF is integrated on the GaN die in series with the gates of T2 and connected to the AlN through an electrical bump (Fig.1).

An additional resistance Rstab (Fig. 1) of 15Ω has been added in series with Ca1 but integrated onto the AlN substrate. This resistor is required to stabilize the cascode cells which are known to be very prone to oscillations. In addition with Rollet criterion, the Figure 2 shows the simulated normalized determinant function (NDF) checking the intrinsic stability of the active cascode cell. To implement such a necessary stability analysis, the electrical device models have been modified to enable the open loop analysis[7]. The stability of the cascode cell is one of the most important design issue.

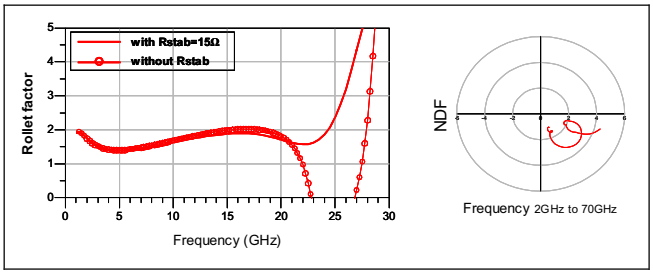

Fig. 2 (a) Influence of Rstab on Rollet factor (b) NDF of the cascode cell.

Once the power balance of the cascode cell has been optimised by the addition of Ca1 and its intrinsic stability ensured by the addition of Rstab, the cascode cell has to be optimised for wideband power operation within a distributed amplifier. Given the required maximum frequency of 18GHz for the distributed amplifier, it is essential to adopt a capacitively coupled distributed architecture [8] in order to meet the conditions of input matching and cut-off frequency of the artificial input gate line. Therefore, the capacitive coupling has been integrated into the cascode cell by adding a series capacitance Cag of 0.3pF on the gate of T1 (Fig.1).

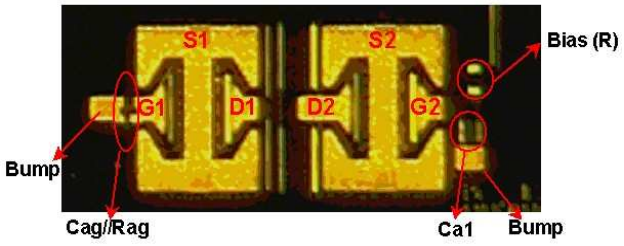

Fig. 3 Photograph of the GaN cascode cell

Moreover, even if the input voltage division due to Cag in series with Cgs induces a reduction of the linear gain of the cascode cell, it makes possible an easier power matching within the distributed architecture up to the maximum frequency of the bandwidth. The series capacitor Cag coupling the cascode cell to the distributed gate line are shunted by implanted resistors Rag of 500Ω in order to supply the gate bias path since there is no gate current flowing through the transistors. Figure 3 shows a photograph of the GaN die integrating the cascode cell and its capacitive and resistive matching elements.

III. Passive Part on AlN Substrate

A specific AlN die (Fig.4) has been designed to separately test the balanced cascode cell while another AlN die has been designed to integrate the distributed architecture [4].

The AlN integrates the stability resistance Rstab and the gate bias pads of the 2nd transistor (V_{BIAS_G2}). The gate bias of the 1st transistor (V_{BIAS_G1}) and the drain bias (V_{BIAS_D}) are supplied by the on-wafer probes. Notice that the drain bias voltage V_{BIAS_D} is twice the bias level of a single transistor.

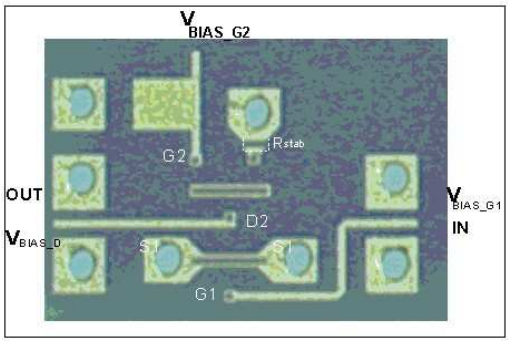

Fig. 4 Photograph of the AlN die designed to flip-chip the GaN cascode. (Input and output lines, DC bias paths, Electrical bumps, Via-Holes)

The AlN circuit also integrates all the via-holes that permit to ground the transistors and the matching elements. The dimensions of the AlN chip are less than (2.5x1.7) mm².

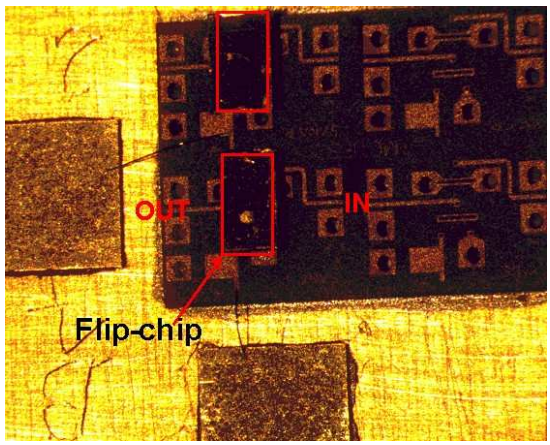

Fig. 5 Photograph of two GaN cascode flip-chipped onto AlN substrate for on-wafer measurements.

IV. Simulation Results

The design of the cascode cell has been performed with the help of the ADS simulation software. Figure 6 shows a comparison of the maximum available gain from 4 to 18GHz between the balanced cascode cell and a single device also integrating the gate coupling Cag and Rag required by the

distributed architecture. As expected, the cascode cell enables to reach higher gain from the beginning of the bandwidth up to the maximum frequency at 18GHz. In the same conditions, Figure 7 shows the comparison of the power characteristics of the balanced cascode cell compared to the single device demonstrating that cascode cell enable higher output powers.

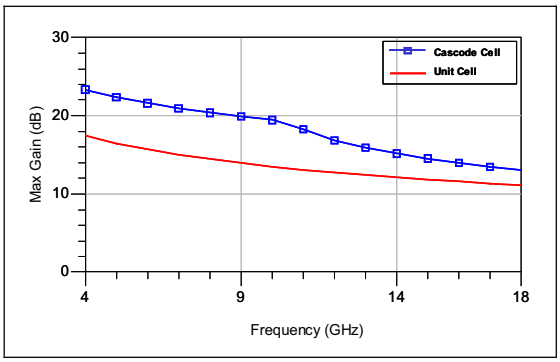

Fig. 6 Comparison of maximum available gain on 4-18GHz between the balanced cascode cell and a single transistor with input (Cag // Rag) cell.

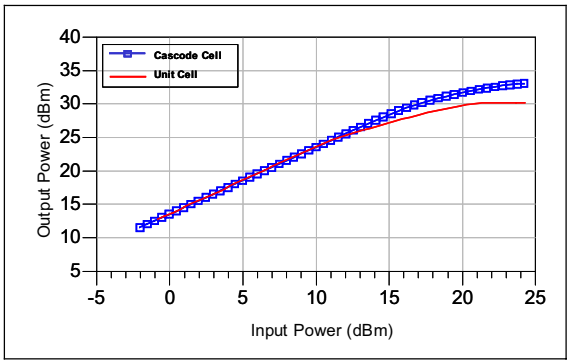

Fig. 7 Comparison of the output power versus input power for the cascode cell and a single transistor with input (Cag // Rag) cell.

In order to check the power optimisation of the cascode cell, Figure 8 shows the simulated intrinsic load lines of the two transistors T1 and T2 of the cascode cell at 10.24GHz in the same load conditions as those used for the load-pull power measurements presented in the next section.

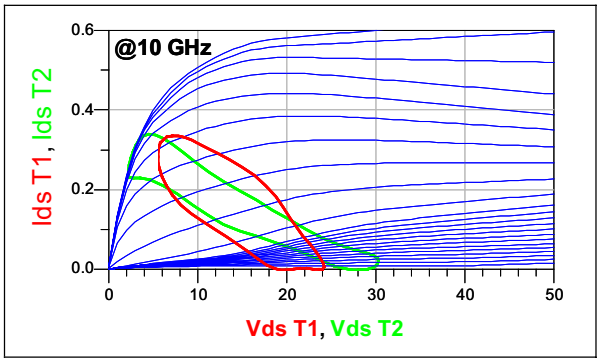

Fig. 8 Intrinsic load lines of each transistor of the cascode cell @ 10.24GHz

V. Measurements

A. Scattering Parameters Measurements:

In order to check the accuracy of the linear and nonlinear modeling of the cascode cell, on-wafer scattering parameters measurements have been performed in the 0.5-20GHz bandwidth as shown on Figure 9. The comparison of simulated and measured S-parameters demonstrates a good agreement and therefore the model accuracy. It is interesting to see that the gain is flat in the beginning of bandwidth and it is not the case for a single transistor.

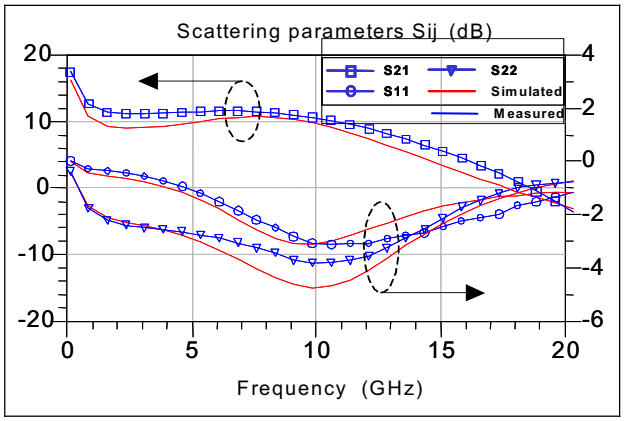

Fig. 9 Comparison between simulated and measured scattering parameters of the balanced cascode cell at V_{BIAS_D}=30 V, V_{BIAS_G1}= - 6 V, and V_{BIAS_G2}=9 V

B. Large Signal Measurements :

On-wafer pulsed Load-pull measurements of the cascode cell have been performed in order to check and compare the optimum power state optimised from nonlinear simulations with power measurements. During the power load-pull characterization, the pulses were 10µs width according to a 10% duty cycle. Both RF signals and biases were pulsed.

1) Measurement Setup

The load-pull measurement setup is based on the use of a VNA including a receiver mode test-set which enables pulsed signal measurements. The synoptic of this pulsed measurement setup is shown on Figure 10. The calibration of this system proceeds in 3 stages :

First of all, a 12 error terms relative calibration is done at the DUT reference plane (under probe). This calibration enables us to measure wave ratios as S-parameters but not the injected power into the DUT.

The second stage consists in carrying out a one port calibration at the coaxial reference plane when the VNA is in 'Reverse' mode. This coaxial calibration is enhanced by the use of the power standard : a power-meter with profile capabilities. This complete calibration enables the system to measure absolute waves at the coaxial reference plane.

The last stage consists in assuming that the '2 ports like' located between our two reference plane is reciprocal. Thus, the errors terms from the full coaxial reference plane calibration make it possible to complete the first calibration

stage in order to measure the absolute wave at the tip of the wafer probes and thus the injected power at the input of the DUT. Generation and measurement of the pulsed bias signals are performed using a pulsed generator and a scope.

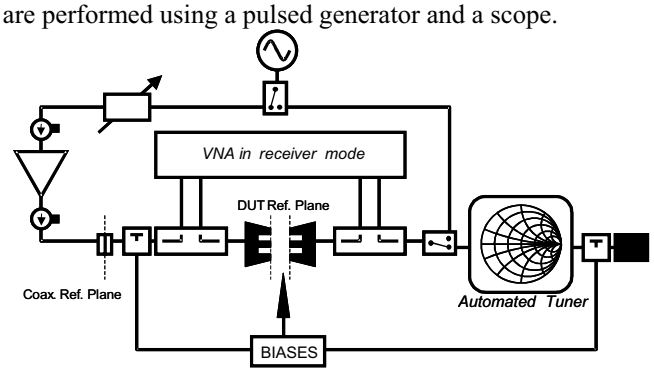

Fig. 10 On-wafer Pulsed Load-Pull Measurement Setup

2) Measurement Results

Figure 11 shows the comparison between simulations and load pull power measurements at 10.24GHz. Both loads are tuned for maximum output power matching at this frequency. The optimum load impedance for maximum output power of the cascode cell is (20+j12) at a bias level of V_{BIAS_D}=30V, V_{BIAS_G1}= -6V and V_{BIAS_G2}=9V.

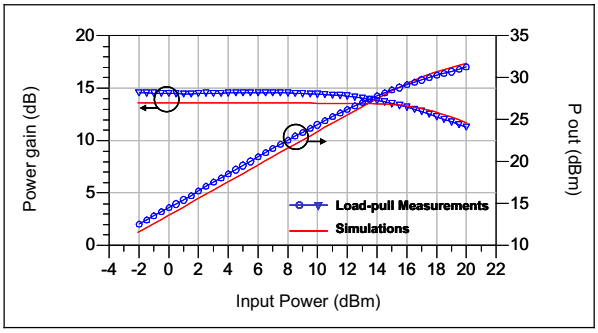

Fig. 11 Comparison between simulated and measured large signal results for the cascode cell with (20+j.12) load impedance @ 10.24 GHz

A very good agreement is obtained between power measurements and simulation even if a small shift of 1dB is observed on the small signal gain. The balanced cascode integrating the gate coupling capacitance of the distributed architecture yields 1.3W output power.

VI. Conclusions

The design method of a power balanced GaN cascode cell has been reported for the wideband power optimization of a capacitively coupled distributed amplifier. After the flip-chip mounting of the balanced GaN cascode onto AlN substrate, the nonlinear model and power simulations were compared to pulsed power measurements. The cascode cell designed onto the GaN chip integrates specific passive matching elements such as the series MIM capacitors (Ca1, Cag) on the gate of each transistor to ensure the optimum power balance over wide bandwidths. Additional resistors (Rag, Rstab) are necessary for ensuring the DC bias and the stability. This paper demonstrates that the cascode cell is well suited to the power optimization of distributed architecture over wide bandwidths since it enables higher gain and high power as well as easier output power matching since its optimum power load is twice the optimum load of a single device.

Acknowledgment

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