

Large Signal Modeling for RF GaN Power HEMTs.

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Abstract

This presentation deals with the nonlinear modeling of European GaN power HEMTs involved in the KORRIGAN consortium. The main activity of the modeling workpackage is to release nonlinear models used in applications expected for TRM modules such as LNA, Power Amplifiers and Switches at both S and X bands. The measurement setups and the complete modeling process will be presented. It includes the parameters extraction of the small signal model, a table based approach for nonlinear HEMTs models, an analytic approach for nonlinear models and some modeled parasitic effects such as thermal effects and trapping effects (gate and drain lag).

Introduction

The KORRIGAN (Key ORganization for Research on Integrated circuits in GAN technology) consortium, lauched in 2005, has been established in order to accelerate the development of independent GaN HEMT foundries in Europe. This project, leaded by TSA (Thalès Sytèmes Aéroportés - France), consists in 29 partners from 7 European nations. This includes several skills such as substrate growth, device processing, circuit modeling and design, circuit packaging and integration. The complete European supply chain will be evaluated at system level. For that purpose, the on-wafer GaN HEMT modeling is an essential step in order to optimize the design of the GaN MMICs.

This presentation offers an overview of circuit level HEMT characterization and modeling. First of all, the measurement setups enable the extraction of the HEMT model parameters (pulsed IV and pulsed S parameters measurement systems) and the large signal model validation (frequency or time domain load-pull measurement systems).

The modeling process starts with a linear model extracted from S parameters measurements. Then, a first nonlinear model can be obtained from the pulsed IV and the pulsed S parameters measurements. This extraction leads us to the nonlinear behavior of some intrinsic model's parameters such as C_{gs} and C_{gd} . Two different approaches will be presented: a table based one and an analytic one.

Some parasitic phenomenon can be added into the nonlinear model. This includes self heating and the gate and drain lag of the measured transistor.

Finally, the large signal response is validated through load-pull measurements.

Measurement Setups

Two kind of measurement setups are used for the transistor level modeling. The pulsed I-V and S parameters system enables the extraction of the nonlinear model parameters and the load-pull system can be use to check the validity of the model for a large signal behavior.

Pulsed IV and S parameters

The current source and the non linear capacitance parameters of the non linear models are extracted for pulsed IV measurements at room temperature. The quiescent bias point is basically the bias point expected for the final application thus fixed by the designer. The instantaneous bias point (500ns length) enables isothermal measurements of the pulsed S parameters according to the pulse period (10us length).

For thermal measurements, we can deduce the junction temperature as the chuck temperature within the RF pulse whereas there is no dissipated power ($V_{gs} = \text{pinch off}$). I-V curves can be measured at different chuck temperatures in order to elaborate a thermal dependence of several model parameters in the case of an electro-thermal model.

Load-Pull measurement setup

Load-pull setups are using automated passive tuner to create the mismatch at the output of the device under test. Benches are based either on the use of a classical VNA (in receiver mode in order to measure the four calibrated waves a_1 , b_1 , a_2 and b_2 at the DUT reference plane at the fundamental frequency) or on a large signal network

analyzer (LSNA) that makes possible to obtain the time domain voltage and current waveforms, so particularly the dynamic load line.

Small Signal models

The small signal model topology is composed of 16 linear components. On one hand, a set of 8 extrinsic parameters (L_g , R_g , C_{pg} , L_s , R_s , C_{pd} , R_d , L_d) linked to the accesses of the component and on the other hand 8 parameters represent the intrinsic part of the transistor (G_d , G_m , τ , R_{gd} , R_i , C_{ds} , C_{gs} and C_{gd}).

The linear model extraction starts from a set of extrinsic values. The intrinsic values are then deduced from S parameters measurements. The linear model is calculated with an optimization loop (simulated annealing method) with a cost function meaning that the calculated intrinsic parameters are frequency independents.

Non linear models

The nonlinear model includes 2 diodes (D_{gs} and D_{gd} modeled with the Schokley equation), 2 nonlinear capacitances (C_{gs} and C_{gd} depending of V_{gs} and V_{gd}) and the main nonlinear current source. The most critical nonlinear element is this current source. It can be either interpolated with splines (table based model) or modeled by Tajima's equations in order to provide a good agreement of measured I-V from pinch off voltage to the full conduction locus while ensuring a good coherency with the equivalent transconductance (G_m) and conductance (G_d) at small signal level.

Table based non linear models

This approach has been used for LNA in Korrigan. The main current source and the two nonlinear capacitances are directly extracted from measurements and interpolated with cubic splines. Id , C_{gs} and C_{gd} values are stored in a 3D table (Value, V_{gs} and V_{gd}). This table based model was developed in C language and has been implemented under Agilent ADS software as a dynamic library (DLL).

Analytic non linear models

This approach was commonly used for HPA applications. Thus, we can consider that the load-line is the one into the final application (leading to the maximal output power or PAE for example). According to this assumption, we can model the nonlinear capacitances as 1D capacitances: $C_{gs}=f(V_{gs})$ and $C_{gd}=f(V_{gd})$. The current source is modeled according to the Tajima's equation. Each nonlinear element was implemented under Agilent ADS with SDD boxes. The Tajima equation includes up to 14 parameters. Few of them are clearly thermal dependant if the model has to include self heating effects.

Electro thermal models

Basically, only the 2 diodes (D_{gs} and D_{gd}) and the current source are thermal dependant. Regarding the Tajima's current source only 4 parameters are thermal dependant. Therefore, the nonlinear model identification process is done for several chuck's temperatures, (junction temperature because of the isothermal pulsed measurements). Then, the thermal law is defined for each thermal dependent parameter of the global nonlinear model such as $Id_{ss}=f(\text{temperature})$.

On the other hand, a thermal simulation of the DUT can be achieved in order to obtain the thermal time response of the materials: $Z_{th}=f(\text{time})$. This simulation is performed for a constant dissipated power. Assuming that the thermal response is linear versus the dissipated power, we can design a sub circuit into ADS (multiple RC cells) that defines the relationship between the dissipated power and the temperature.

Finally, the electro-thermal model includes thermal parameters, the temperature is calculated from the dissipated power through the RC cells and this dissipated power depends on the thermal parameters. The complete model is then self consistent.

Trapping effect models

Gate and drain lags are non negligible parasitic effects for GaN HEMTs. Those effects could be analyzed as a modulation of the main current source according to the gate and drain voltages stimuli. Those effects can be included into the final nonlinear model. The main current source is the same that the one obtain for a classical nonlinear model but the command voltage is modified to take into account the trapping effect. In this case, the main current source can be written as: $Id=f(V_{gs}, V_{ds}, V_{bias}, \text{time})$. Some transients are added to the command voltages. Those transients are related to the capture or the emission of charges by the traps. The main idea consists in creating an "envelope detector-like" with given time constant for capture and emission to modulate the main current source. The model has to include as many "envelope detector" as the number of different trapping time constants.

Those trapping emission time constants can be obtained from pulsed I-V measurements. For example the drain lag time constants are obtained from a long pulse on the drain when $V_{gs}=V_{\text{pinch off}}$. In this case the self heating effects are negligible during the measurement.

Large Signal Modeling for RF GaN Power HEMTs

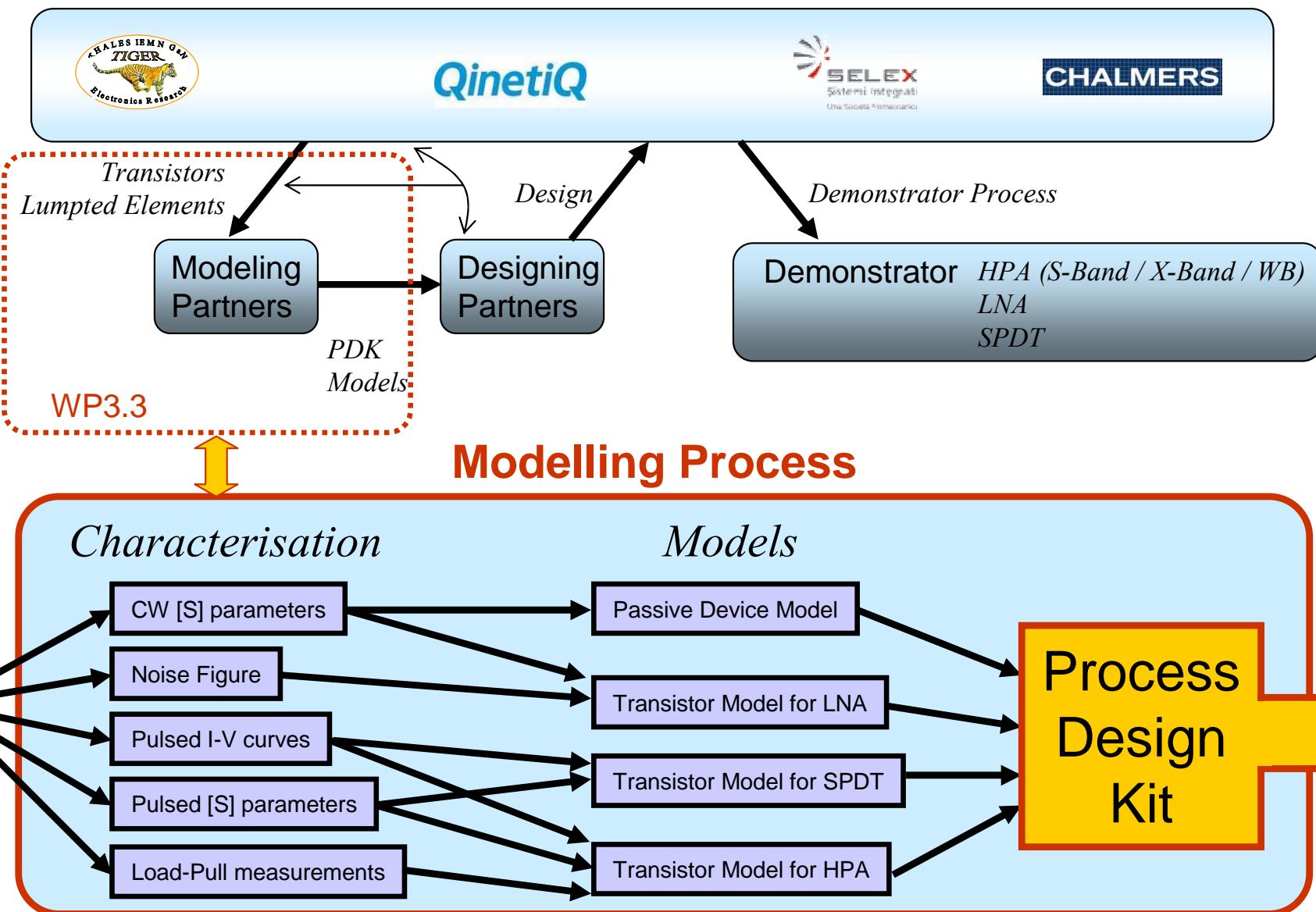
Tibault Reveyrand, Olivier Jardel, Fabien De Groote,
Christophe Charbonniaud and Raymond Quéré



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- Presentation of the 'Modeling' Workpackage
- Passive Devices Modelling
- Active Devices Characterizations
- Nonlinear Models
 - *Small signal model*
 - *I-V model*
 - *Non linear capacitances*
 - *Thermal model*
 - *Trapping effects model*
- Models for Agilent ADS
- Conclusion

Four foundries are implied in Korrigan final demonstrators



Foundry



QinetiQ



CHALMERS

Techno.

MS+CPW

CPW

MS+CPW

MS

Modeling labs



QinetiQ



CHALMERS

PASSIVE DEVICES

Foundries



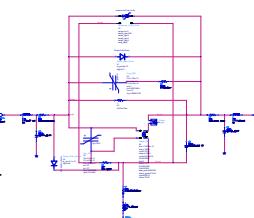
QinetiQ



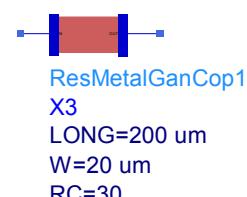
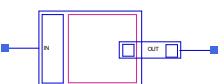
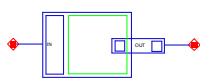
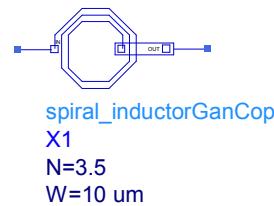
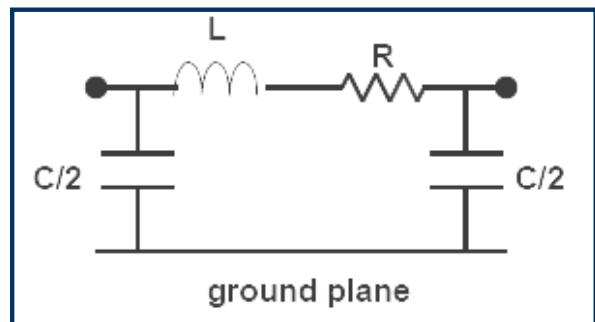
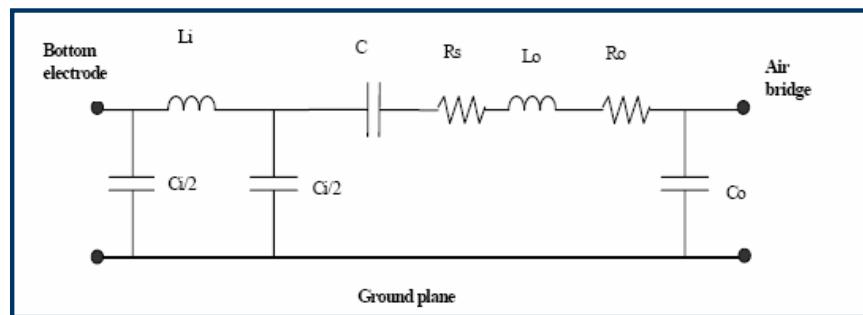
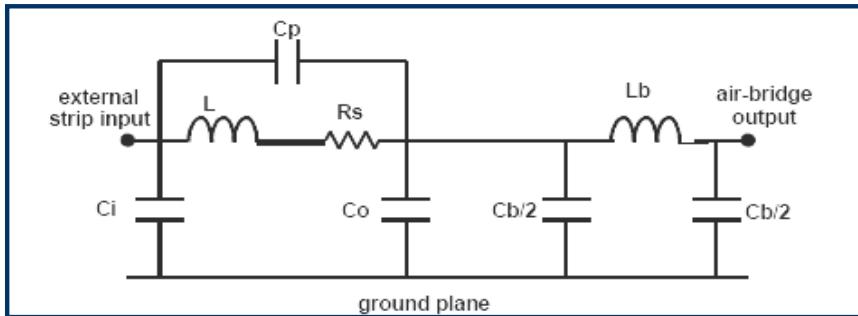
CHALMERS

- Pulsed IV measurements
- Load-Pull measurements
- Modeling

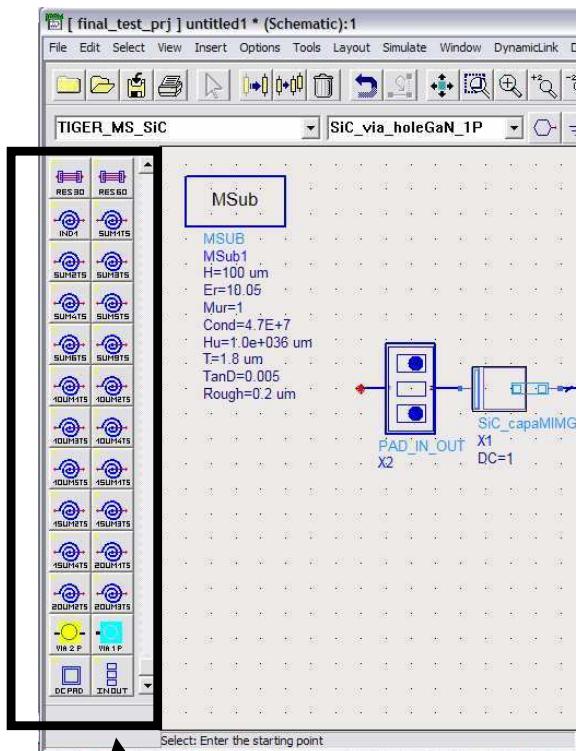
ACTIVE DEVICES



PASSIVE DEVICES MODELLING



GaAs library optimized for GaN devices

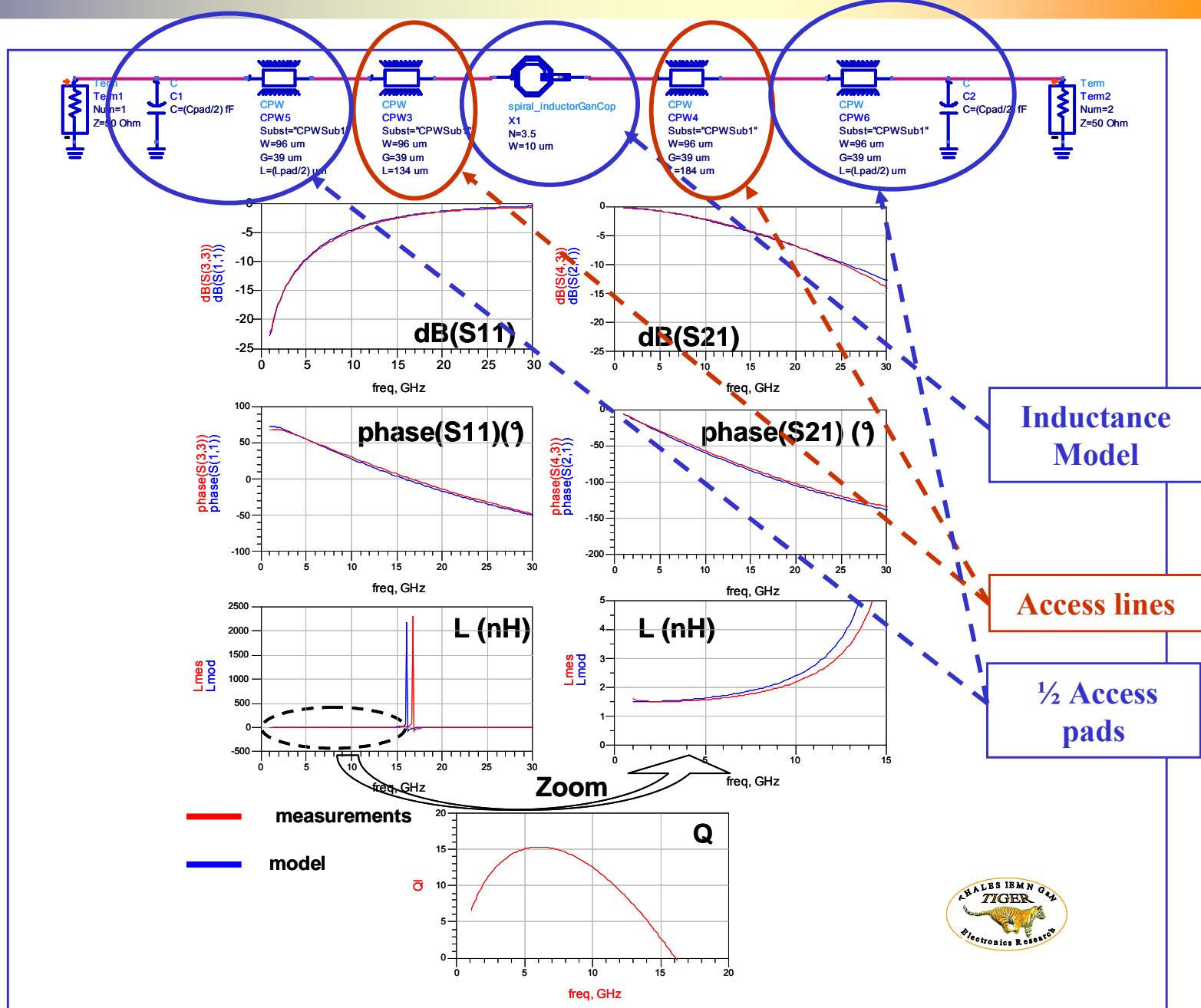


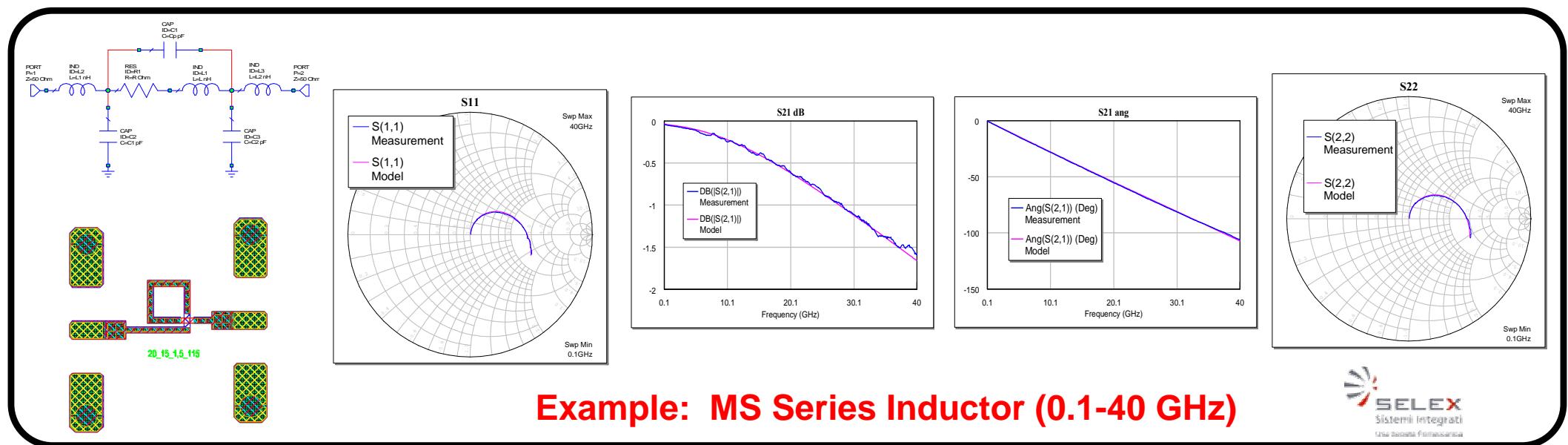
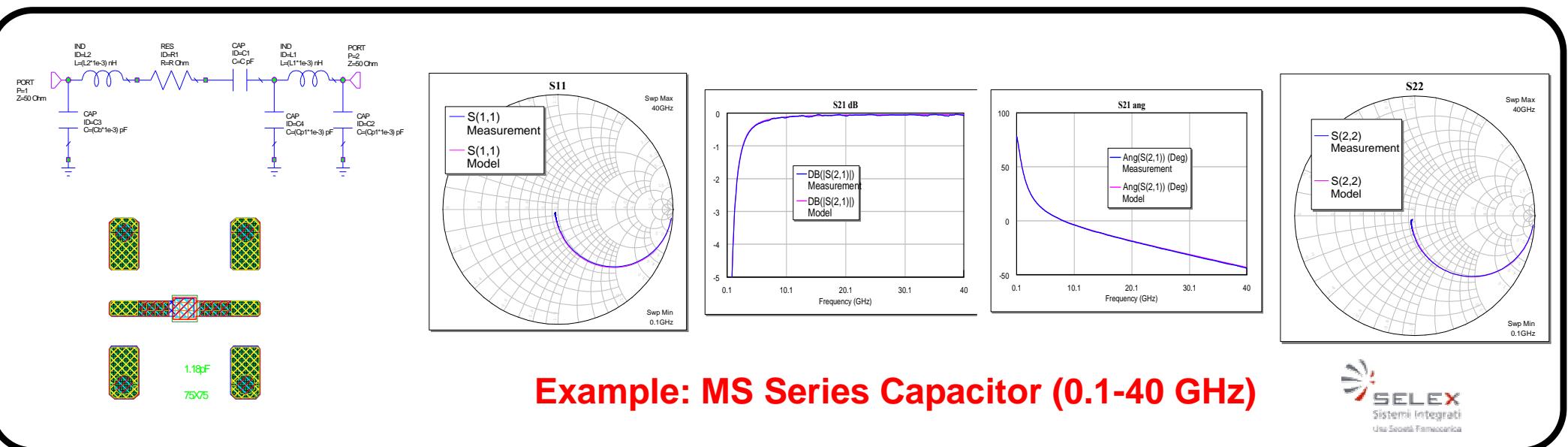
Tiger Design Kit

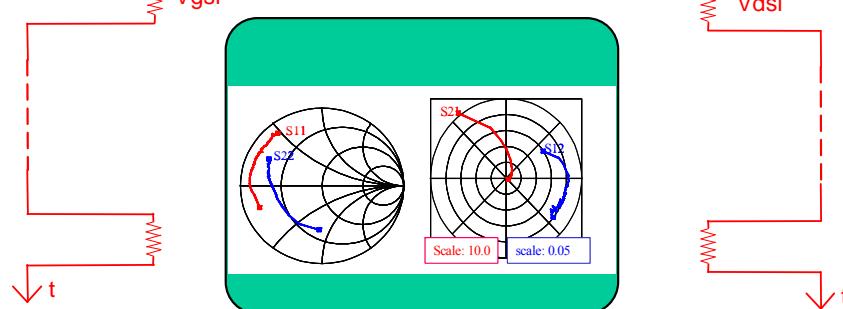
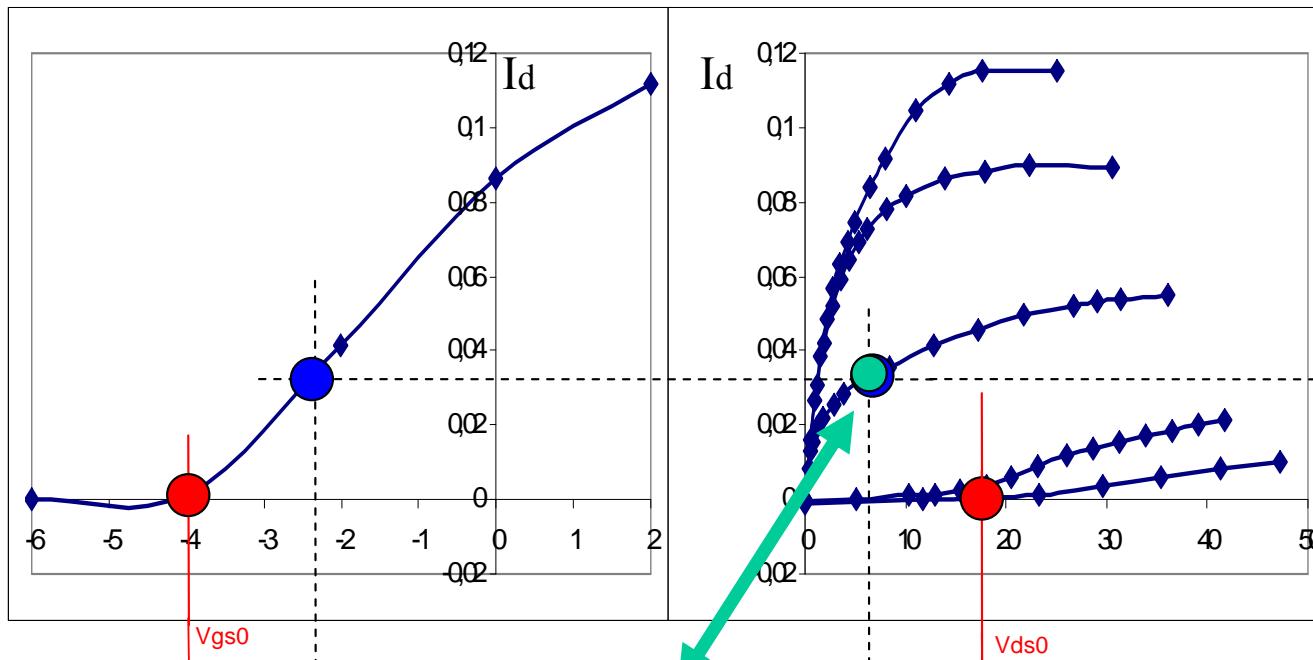


Inductance model :
 Example of comparison
 between measured
 and modelled [S]
 parameters

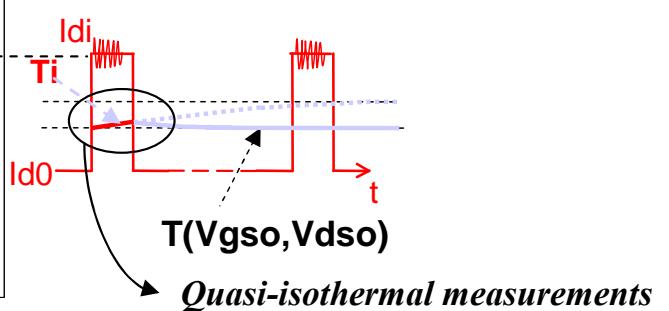
N=3.5
 W=10 μ m



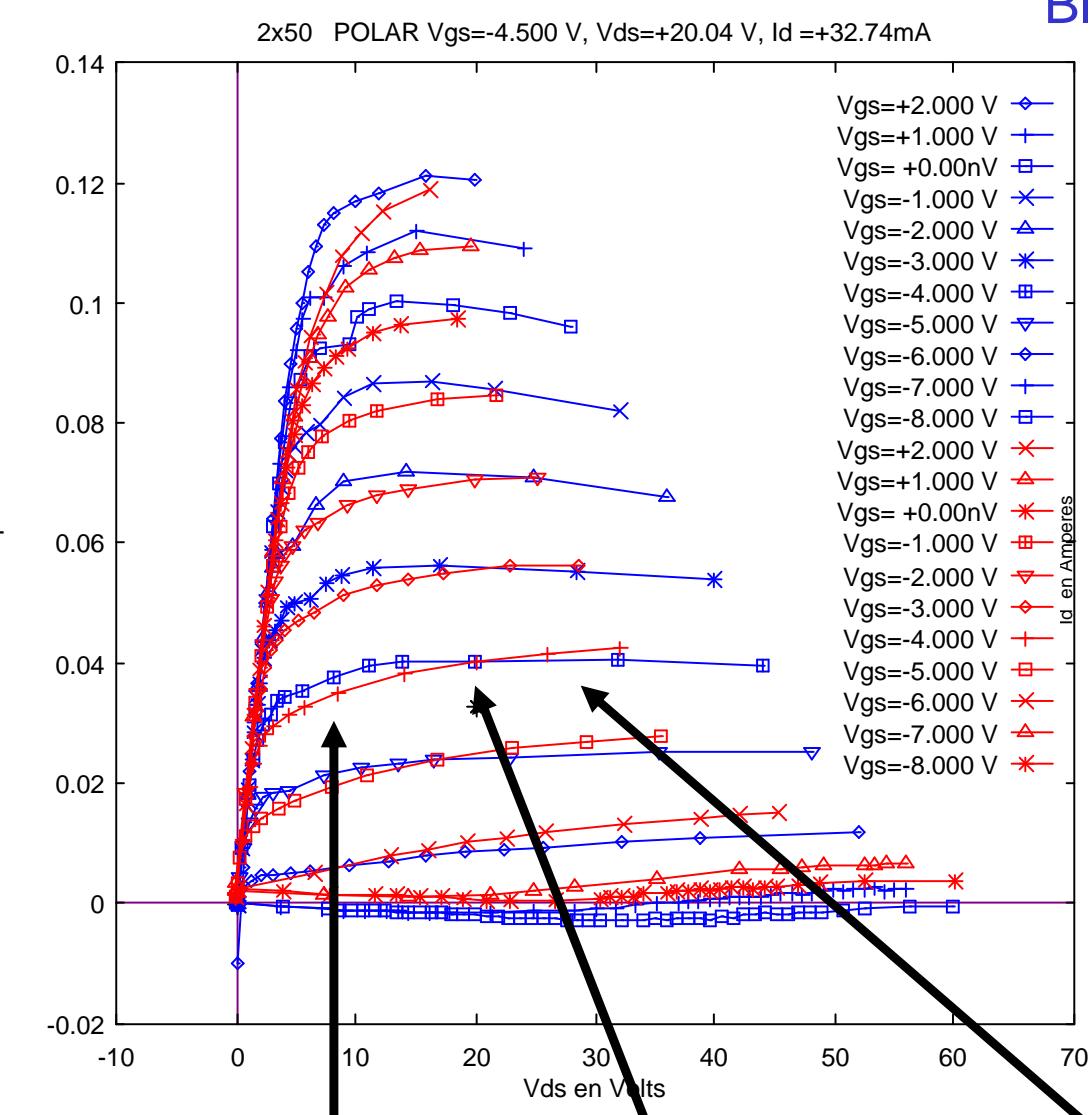




Pulsed I-V and [S] Measurement Setup



→ I-V : 2A 100 V
 → [S] : 0.5 @ 40 GHz
 → $-65^\circ\text{C} \leq T \leq 200^\circ\text{C}$

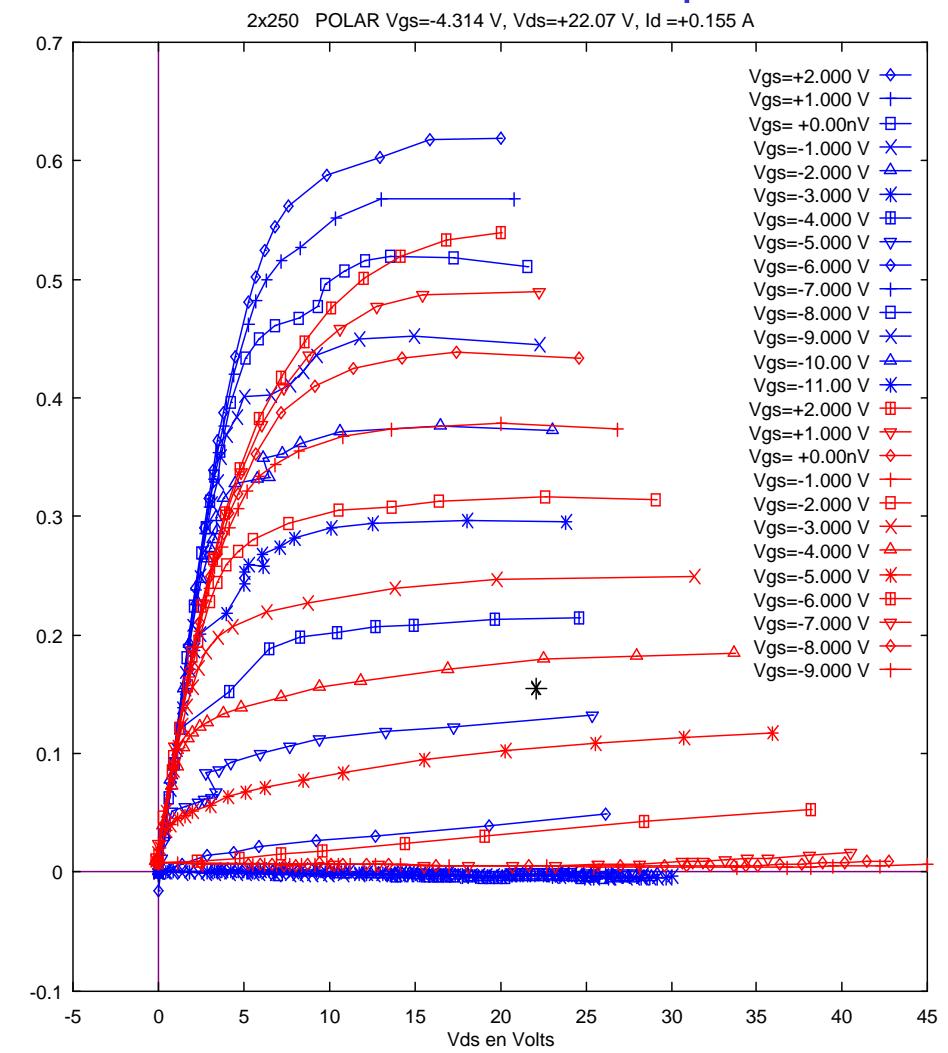


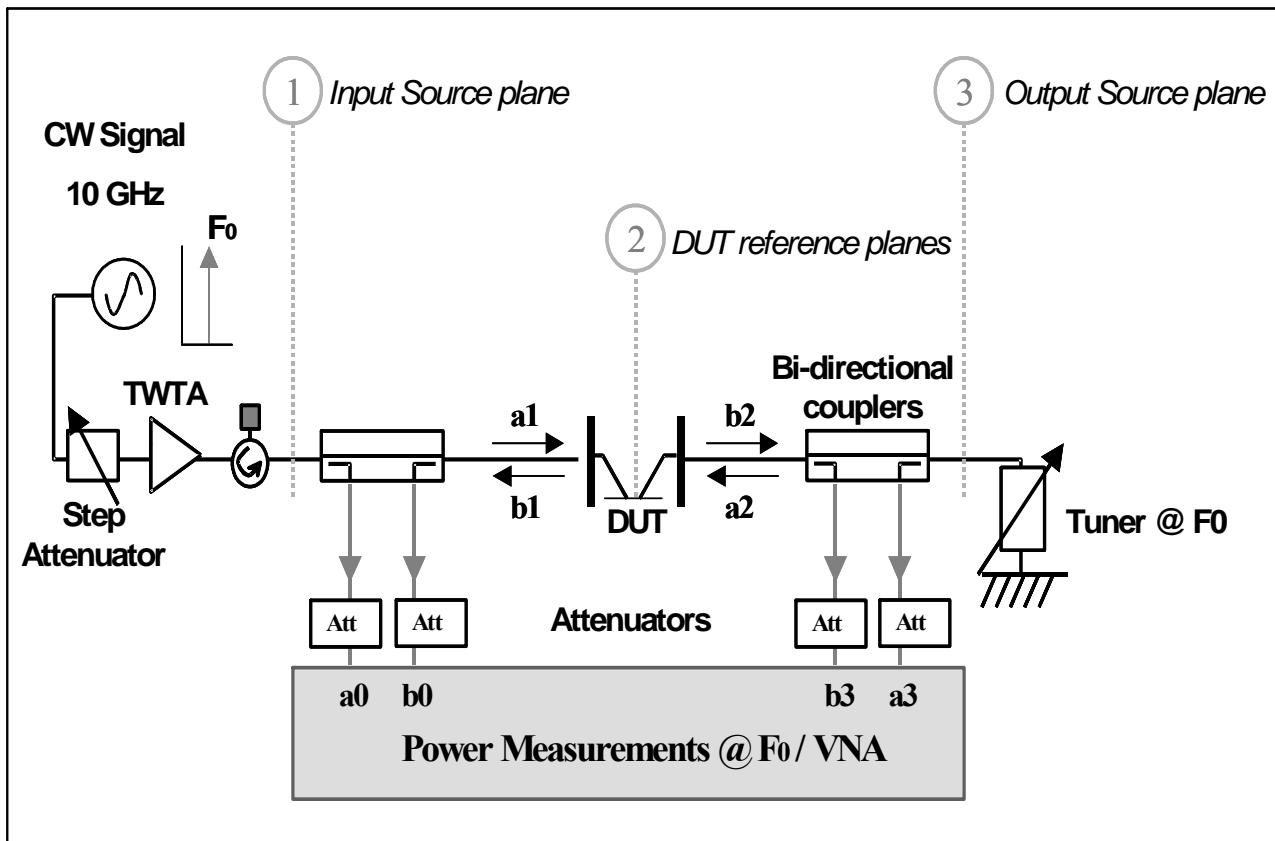
Thermal > Trapping

Thermal ~= Trapping

Thermal < Trapping

Blue network : Cold Quiescent point



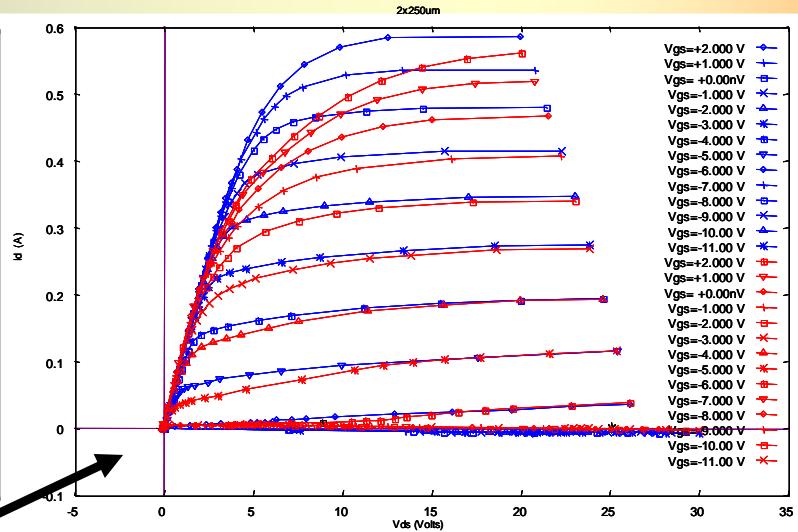
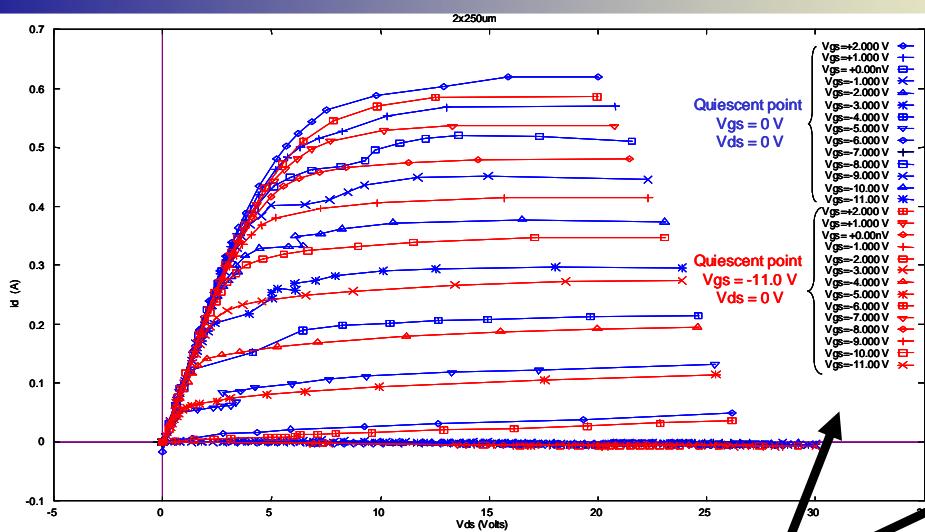


Load-Pull Measurement Setup

Measurements of the 4 absolute waves @ F_0

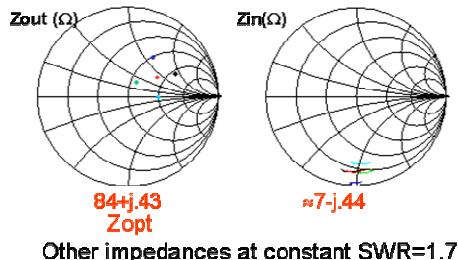
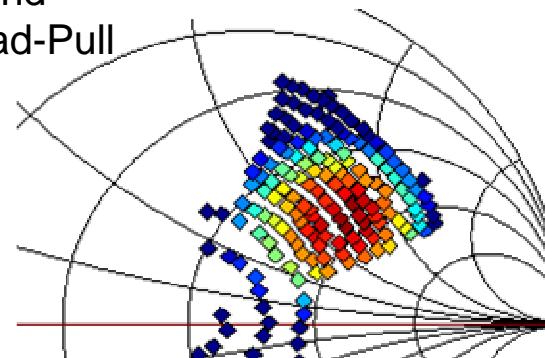


- Pulse capabilities up to 20 GHz
- Power calibration with a profile powermeter
- Passive Tuner or Active Loop

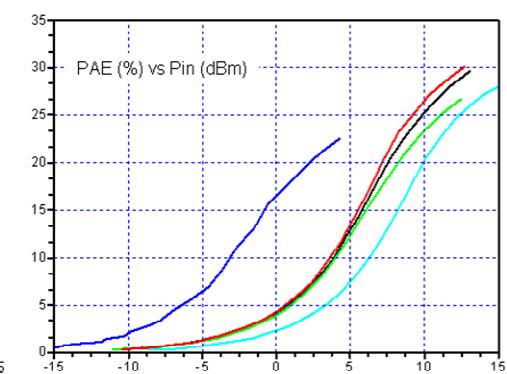
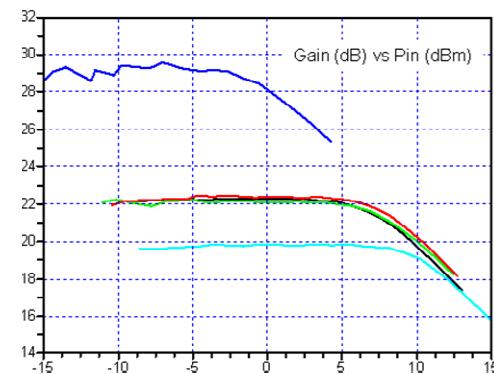
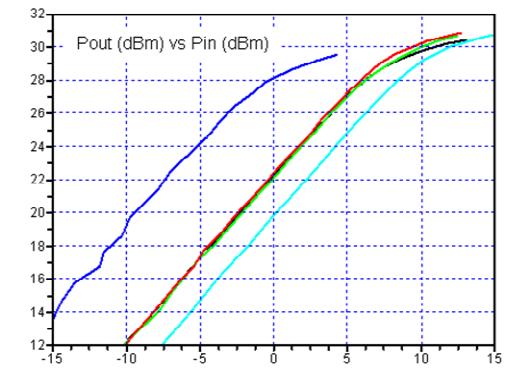


Gate and Drain Lag networks used to investigate trapping effect.

Models are extracted from hot quiescent bias point and validated through Load-Pull Measurements



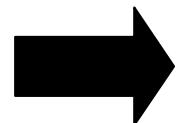
Other impedances at constant SWR=1.7



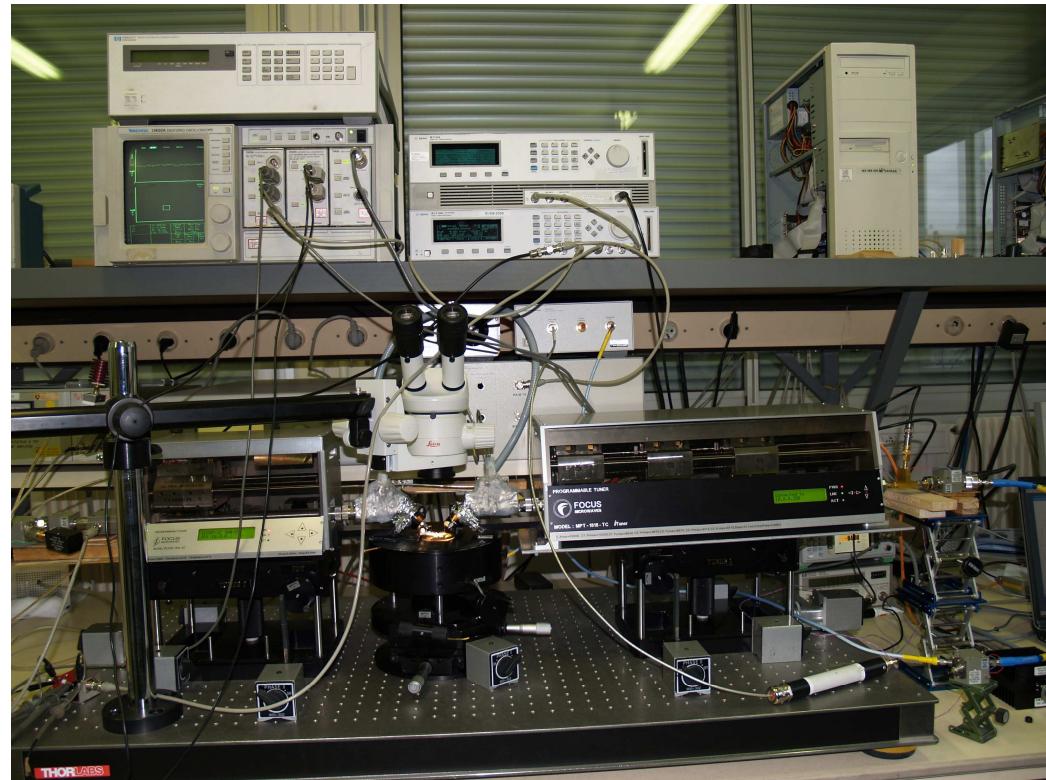
Using a LSNA for Load-pull characterizations

Calibrated instrumentation :

- Network calibration
- Amplitude calibration (Powermeter)
- Phase calibration (HPR)



Time domain waveforms

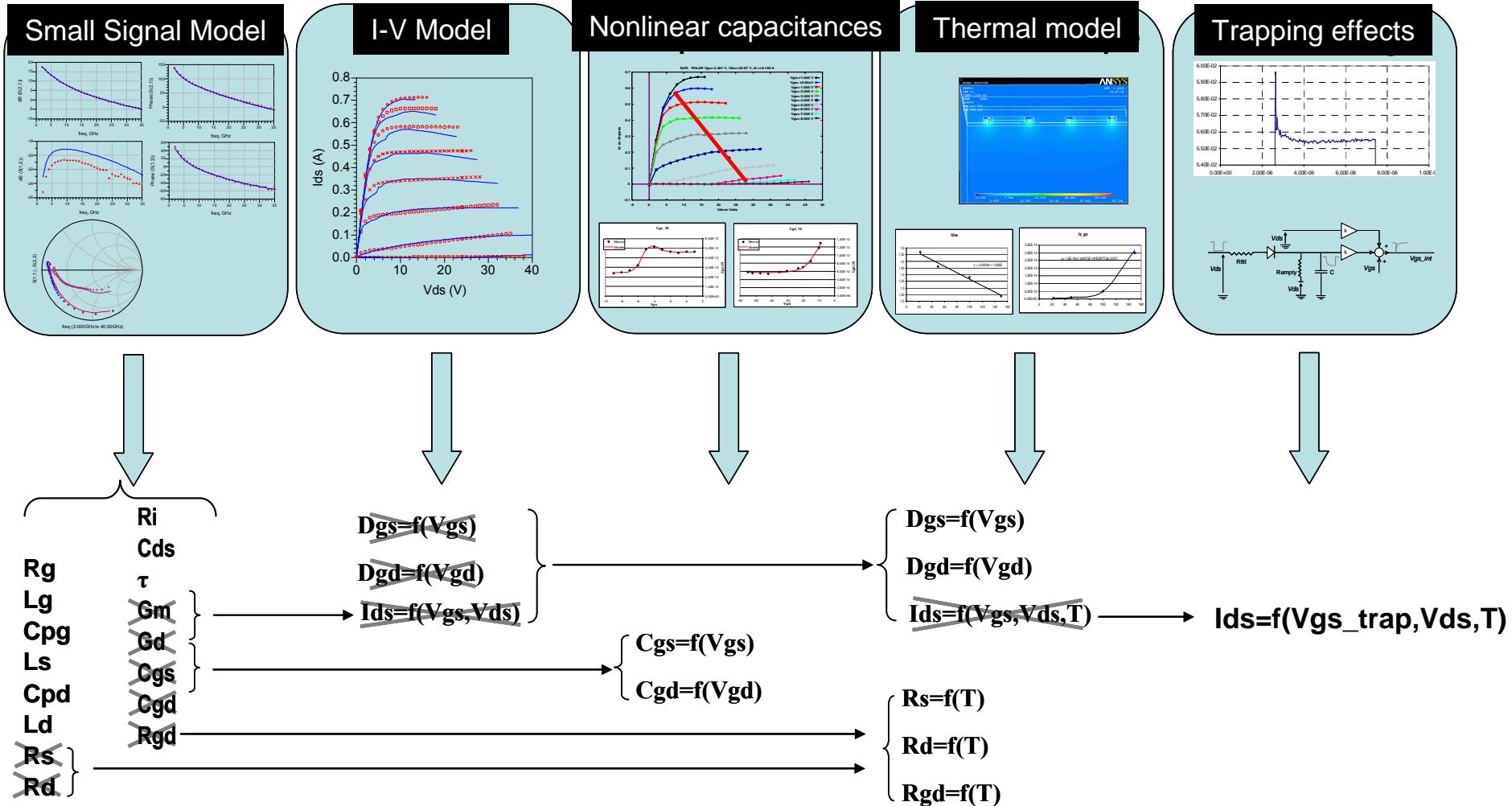


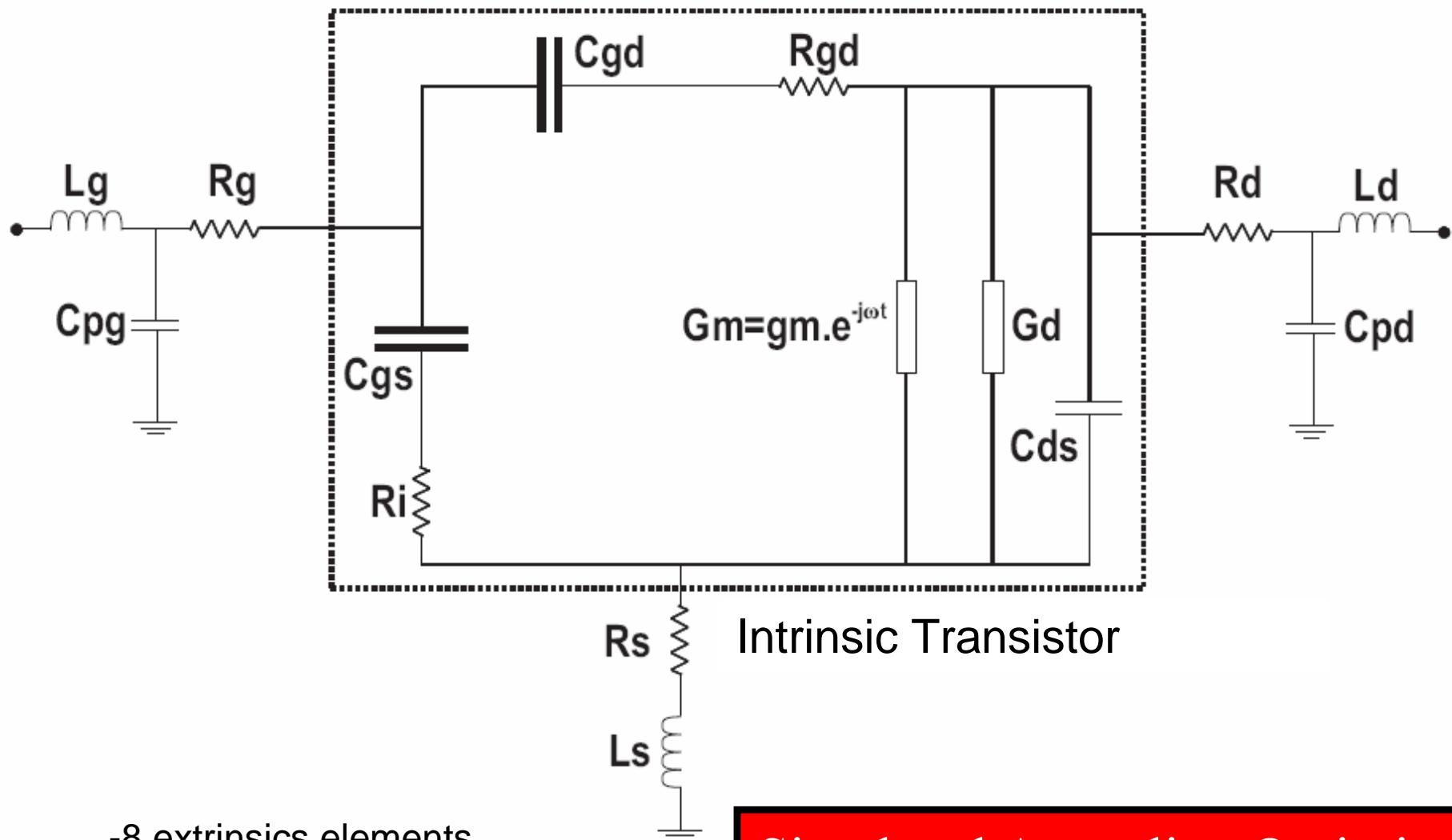
$$\begin{bmatrix} a_{1_{dst}}(f) \\ b_{1_{dst}}(f) \\ a_{2_{dst}}(f) \\ b_{2_{dst}}(f) \end{bmatrix} = |K(f)| \cdot e^{j \cdot \varphi(K(f))} \begin{bmatrix} 1 & \beta_1(f) & 0 & 0 \\ \gamma_1(f) & \delta_1(f) & 0 & 0 \\ 0 & 0 & \alpha_2(f) & \beta_2(f) \\ 0 & 0 & \gamma_2(f) & \delta_2(f) \end{bmatrix} \cdot \begin{bmatrix} a_{1_m}(f) \\ b_{1_m}(f) \\ a_{2_m}(f) \\ b_{2_m}(f) \end{bmatrix}$$

Calibration for fundamental frequency and harmonics

Modeling steps

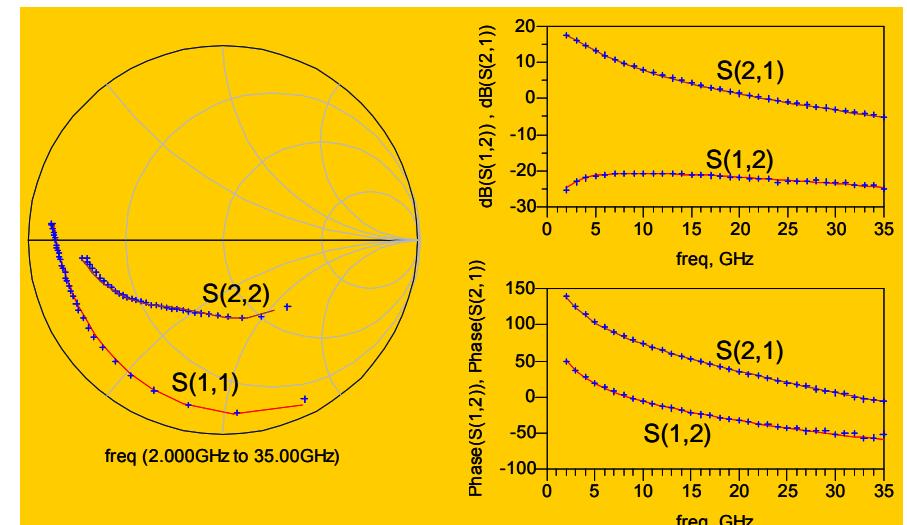
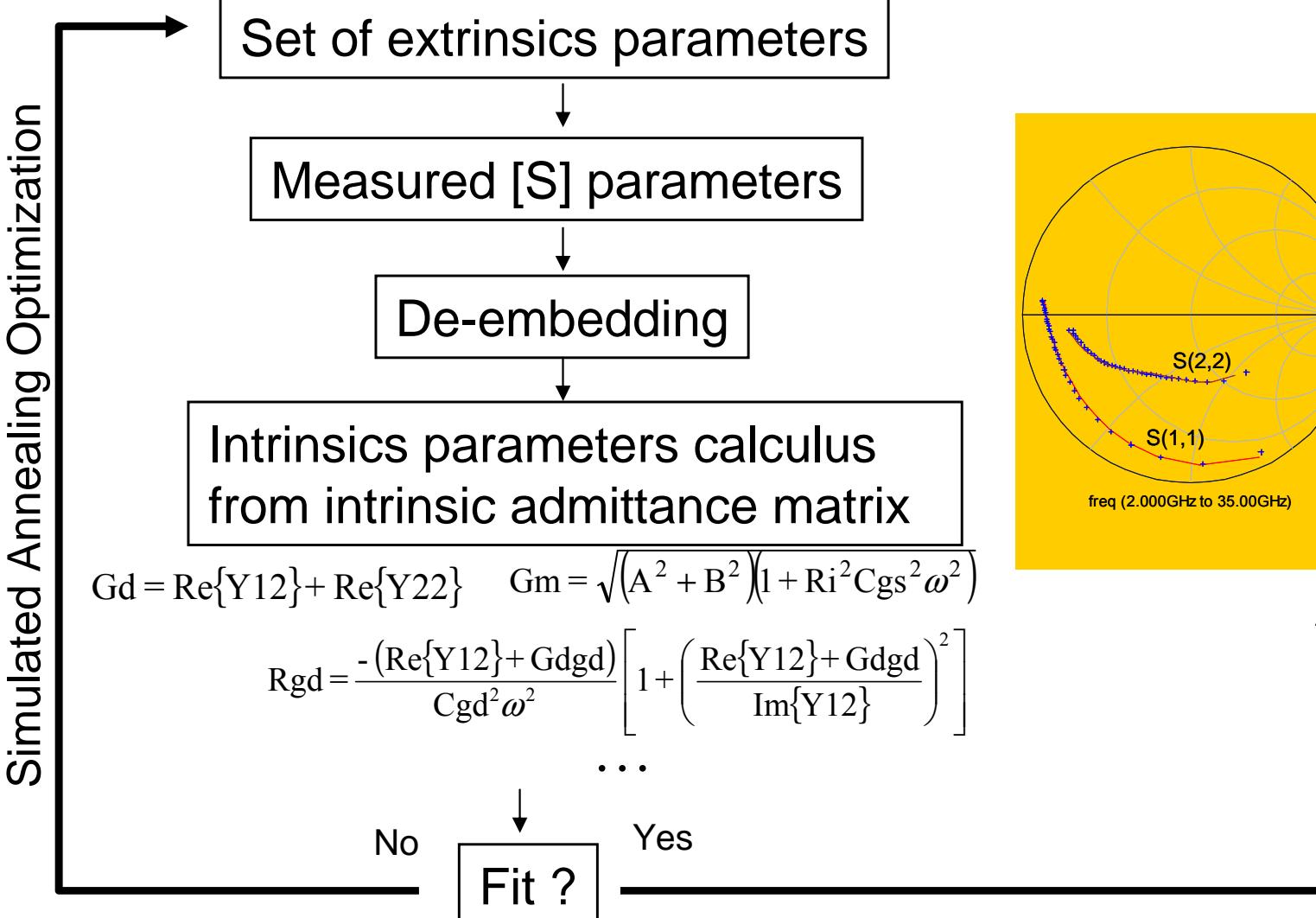
Modeling process





Simulated Annealing Optimization

Frequency dependant elements extraction

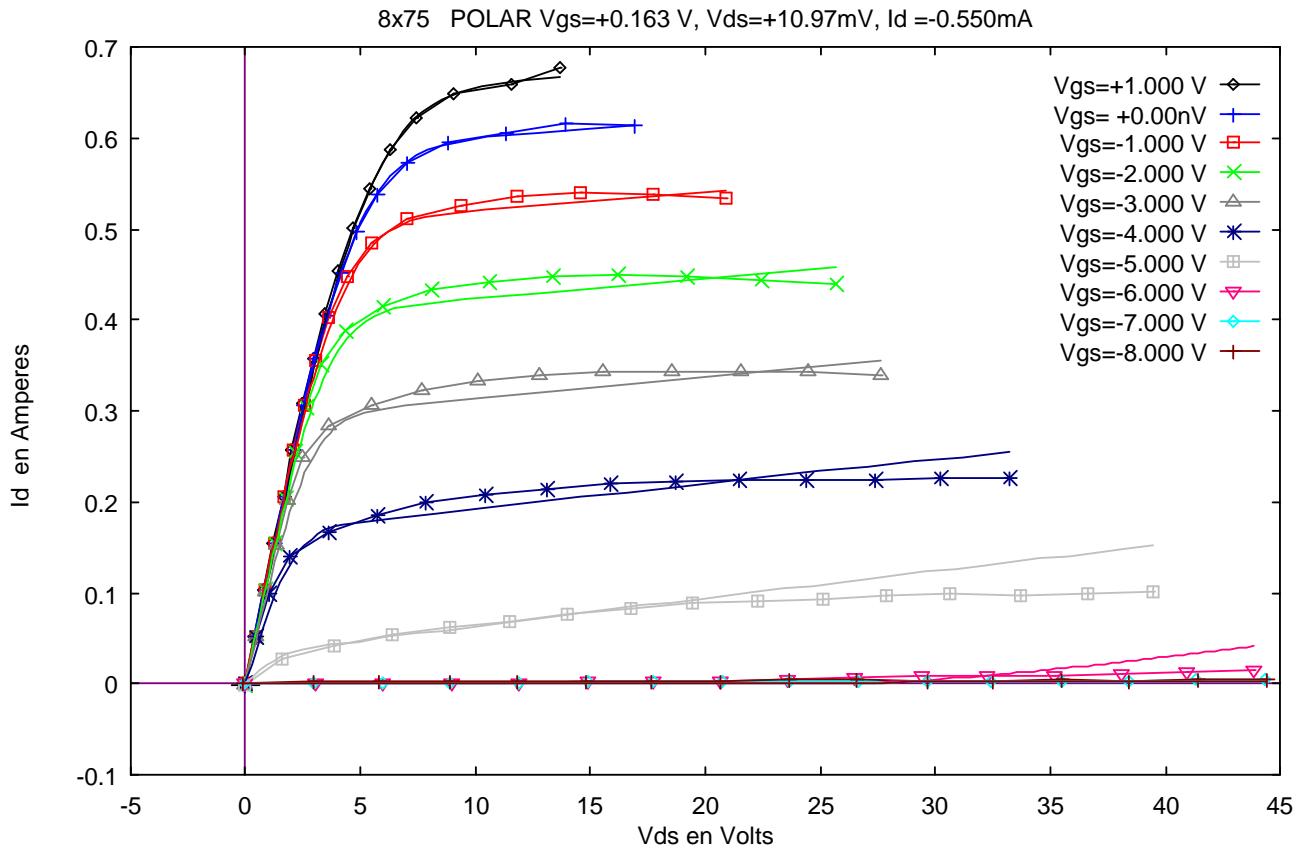


Tajima equations + Breakdown

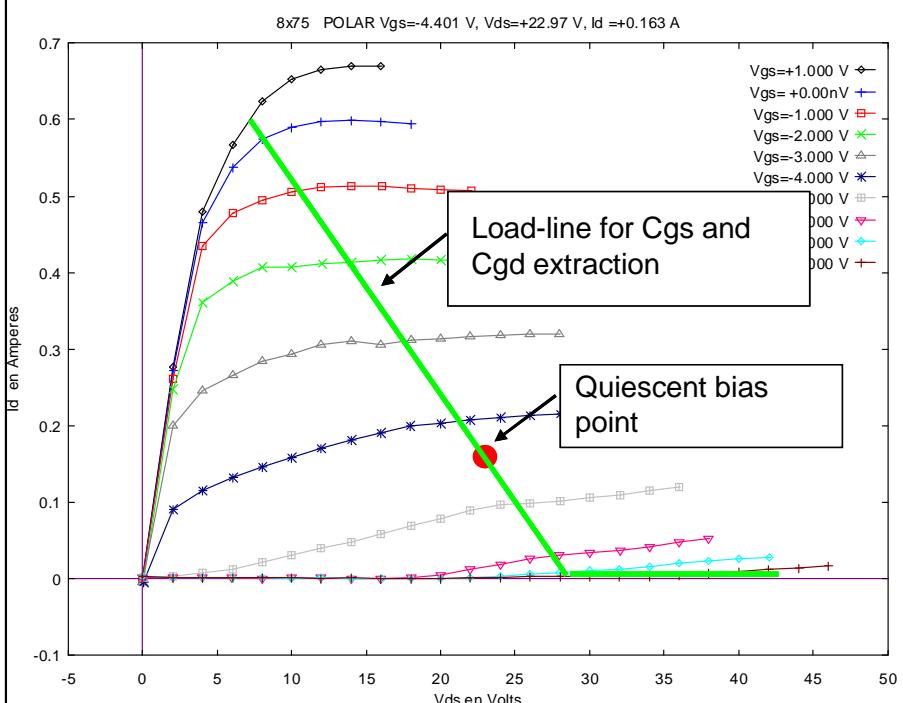
$$I_d_{Tajima} = \frac{I_{DSS}}{1 - \frac{1}{m}(1 - e^{-m})} \left[V_{GSN} - \frac{1}{m} \left(1 - e^{-mV_{GSN}} \right) \right] \times \left[1 - e^{-V_{DSN}(1-aV_{DSN}-bV_{DSN}^2)} \right]$$

$$V_{GSN} = 1 + \frac{V_{GS}(t - \tau) - V\phi}{V_P}$$

...



C_{gs} et C_{gd} extracted from [S] parameters along the optimal load-line



$$\rightarrow C_{gs} = f(V_{gs})$$

$$\rightarrow C_{gd} = f(V_{gd})$$

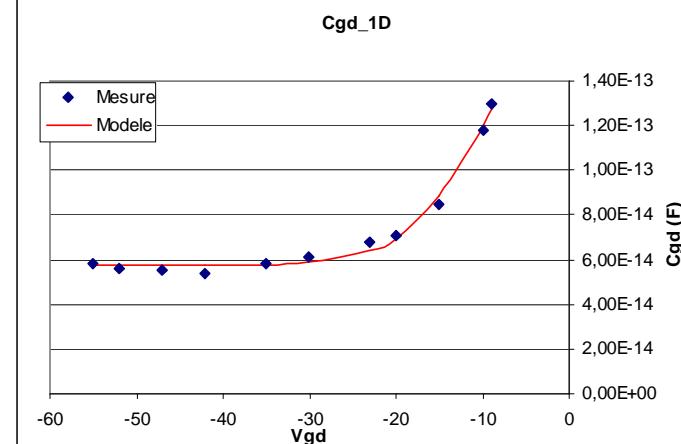
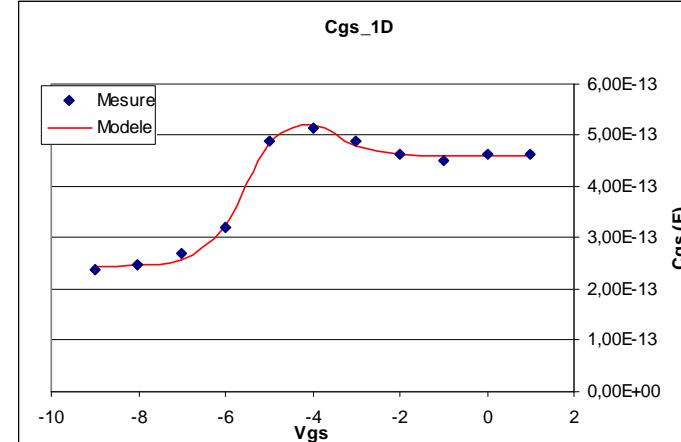


Easy for modeling



Validity of the model only for a given quiescent bias point ?

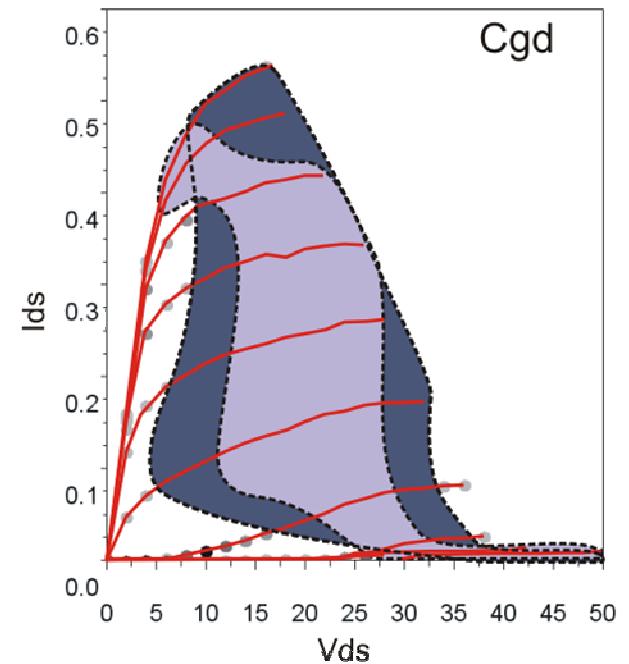
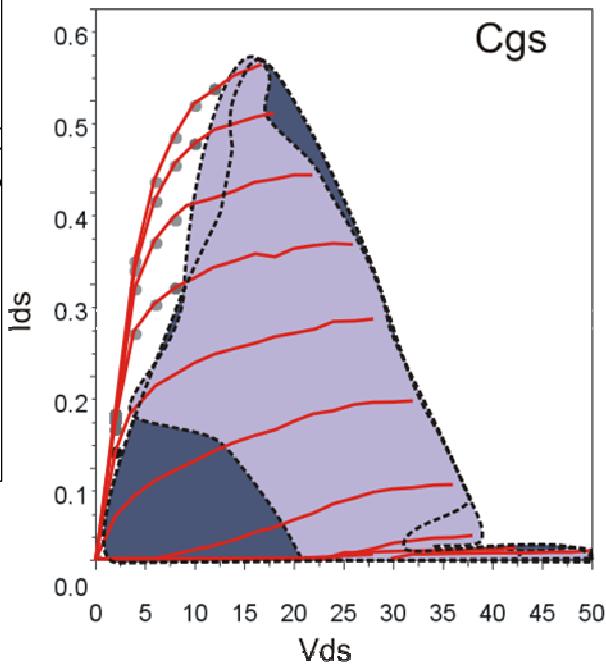
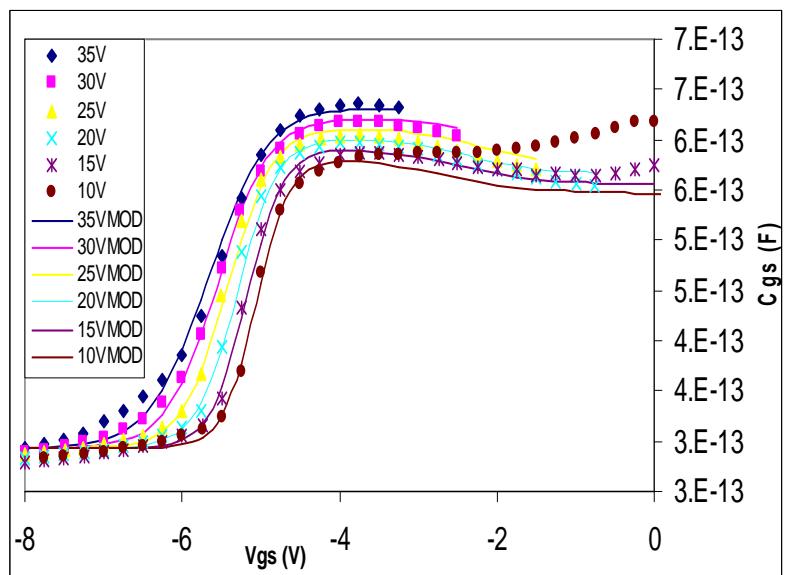
Equations



$$C_{gs} = C_0 + (C_1 - C_0) \cdot (0,5 + 0,5 \cdot \tanh(a \cdot (V_{gs} + V_m)))$$

$$- C_2 \cdot (0,5 + 0,5 \cdot \tanh(b \cdot (V_{gs} + V_p)))$$

Example: 2D Model for Cgs 2D:



→ Good agreement on a larger area



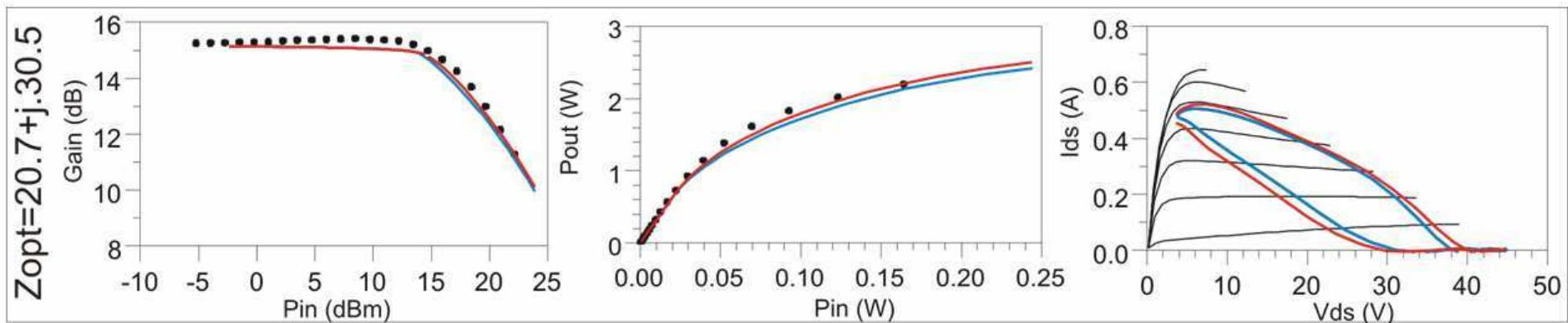
Error area < 4% with 2D model



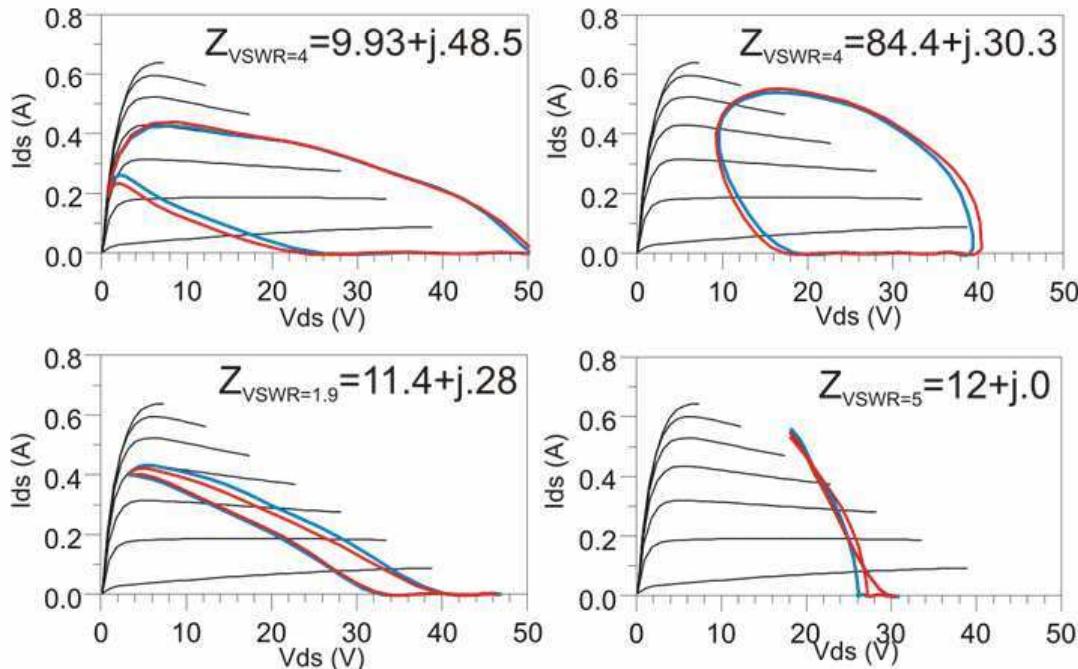
Error area < 4% with 1D model

LARGE SIGNAL SIMULATIONS : Model accuracy

- On the power optimal load impedance class AB, 25V, 10 GHz – Measurements Comparison



- On several load impedances (largest cycles)

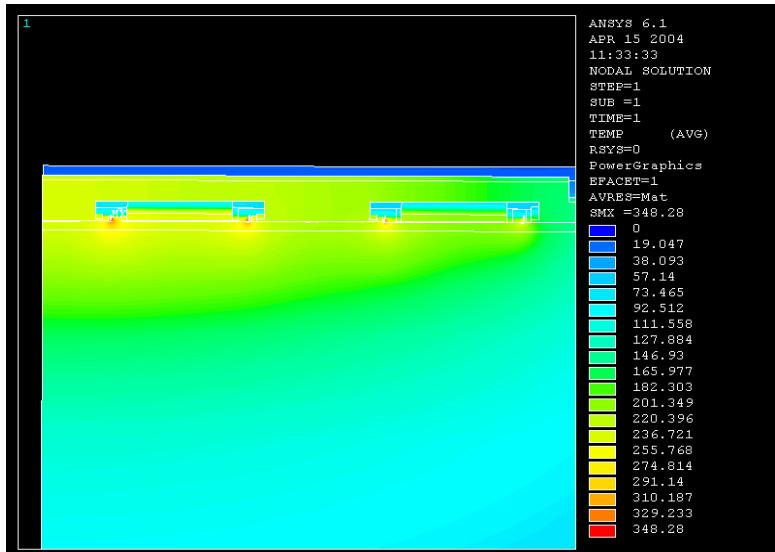


→ Good agreement of 1D model versus the 2D model

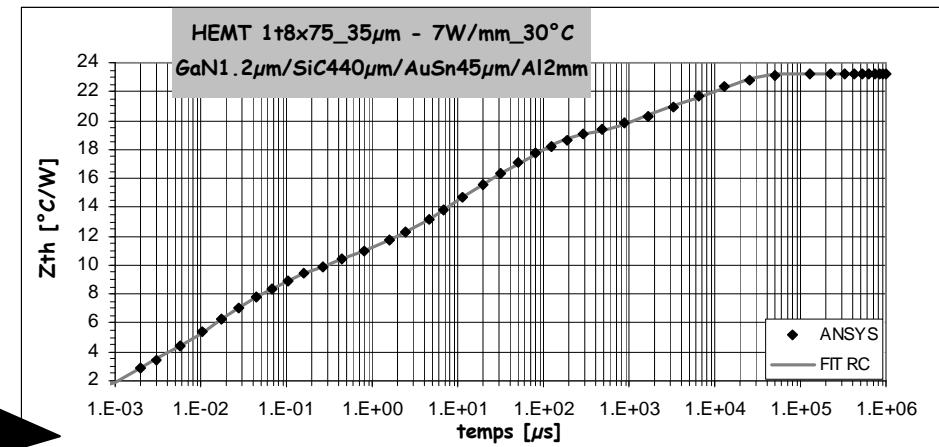
But :

- Equations too complicated (charge conservation)
- Tough modeling (number of parameters)

Thermal Simulations (3-5 lab)



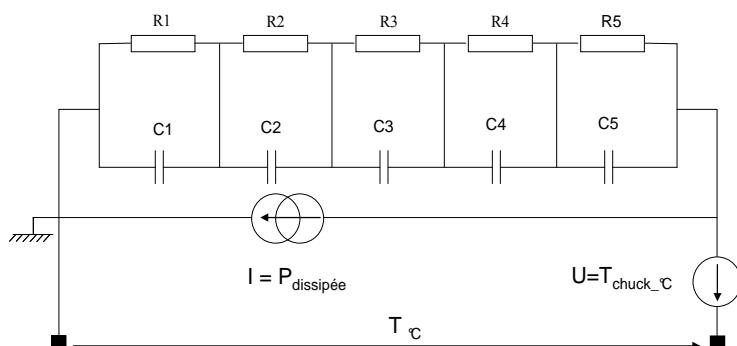
Self Heating Extraction = f(t)



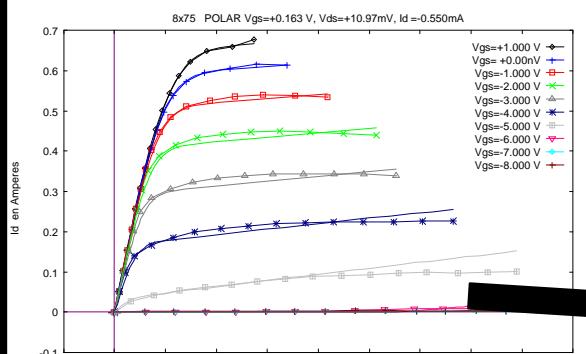
Exponential expansion :

$$TEMP = 22.8 \cdot (1 - e^{-t/\tau_1}) + 21.7 \cdot (1 - e^{-t/\tau_2}) + 7 \cdot (1 - e^{-t/\tau_3}) + \dots$$

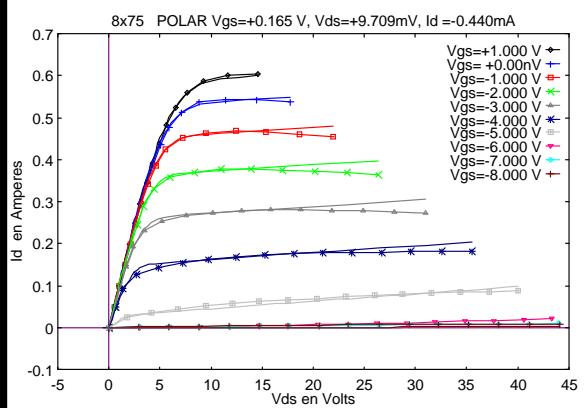
RC cells behavior



IV Modeling @ several temperatures

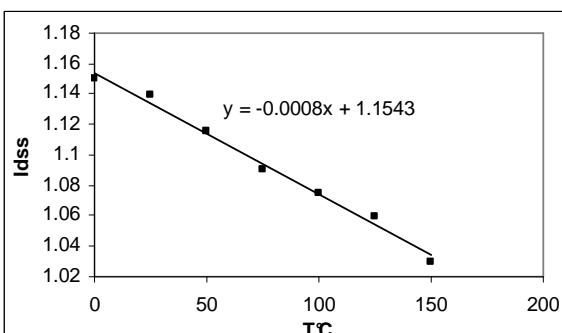
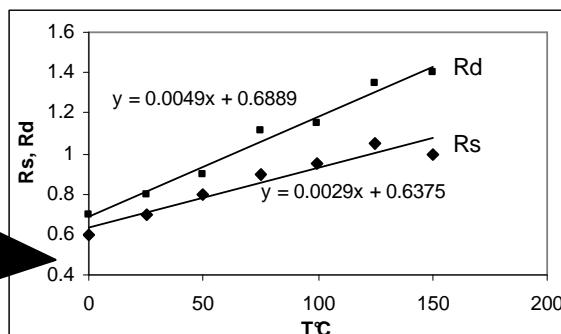


Measure / IV Model @ 25°C



Measure / IV Model @ 150°C

IV parameters versus temperature



Equations

Thermal parameters

- Access Resistances
- Current Source
- Diodes

$$Rs = Rs_0 + \alpha_{Rs} \cdot T$$

$$Rd = Rd_0 + \alpha_{Rd} \cdot T$$

$$Idss = Idss_0 + Idss_t \cdot T$$

$$P = P_0 + P_t \cdot T$$

$$Ngs = Ngs_0 + Ngs_t \cdot T$$

$$Ngd = Ngd_0 + Ngd_t \cdot T$$

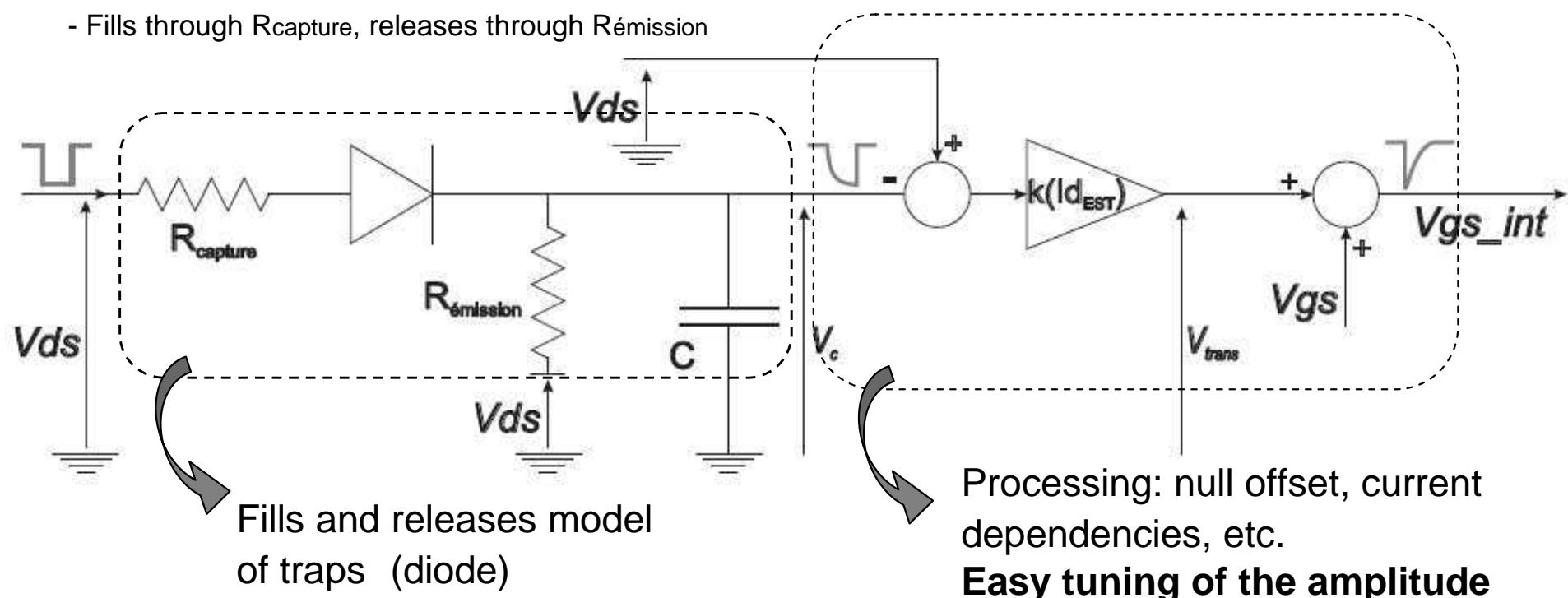
$$Isgs = Isgs_0 + Isgs_t \cdot e^{(T/Tsgs)}$$

$$Isgd = Isgd_0 + Isgd_t \cdot e^{(T/Tsgd)}$$

Gate- and drain-lag model topology (for ONE trap)

Trapping effect on the current modeled with a modification of the control voltage (= V_{gs})

- Creates transients on V_{gs} = Current transients
- Charging state of the capacitance = charging state of the traps
- Fills through $R_{capture}$, releases through $R_{émission}$

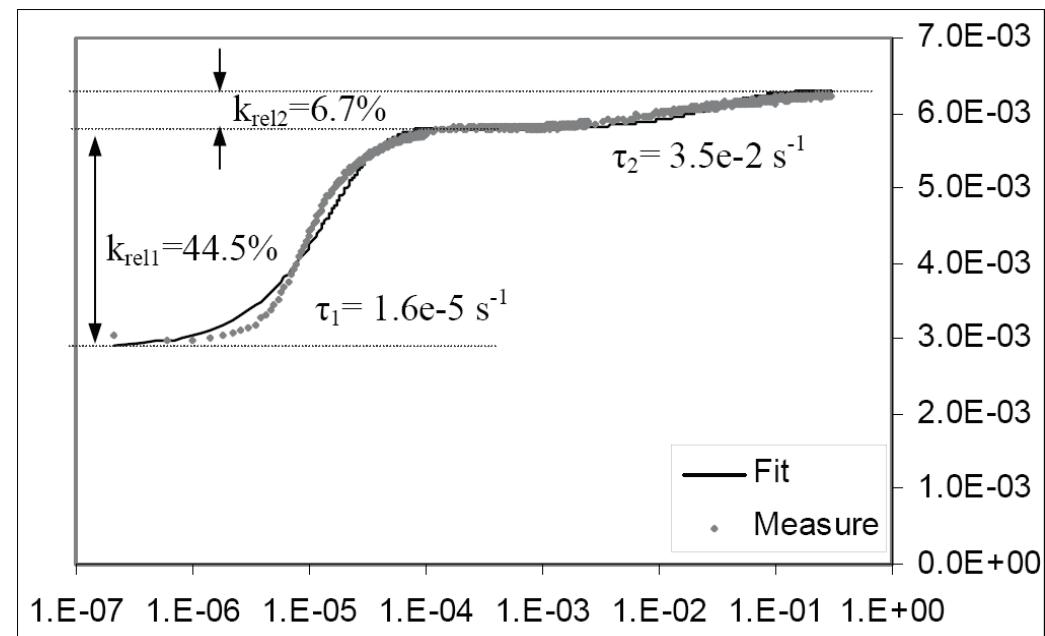
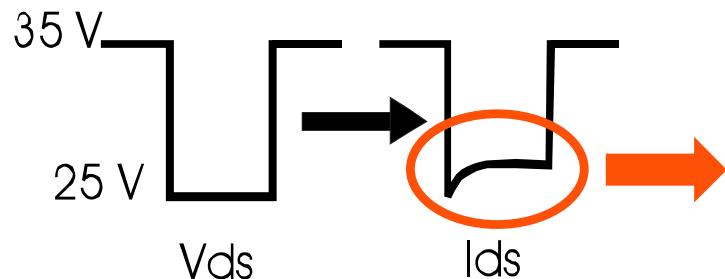


Fundamental effect : fill / release trapping time constants are different

→ modeled with an envelope detector

- Circuits number = Modeled traps number
- 3 parameters to extract per circuit : $R_{caption}$, $R_{release}$, k

Trap model parameters extraction



Current transient measurement, Negative pulse on V_{ds} (emission)

- Obtaining :
- numbers of traps
 - emission time constants
 - relative amplitude of each trap

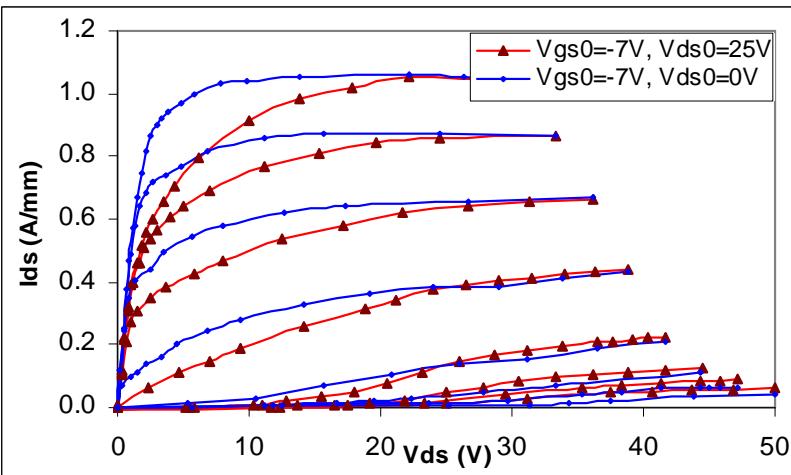


Avoid thermal effects during measurement

→ ONLY ONE MEASUREMENT TO OBTAIN ALL THOSE PARAMETERS

Influence of the drain lag model on the simulated IV characteristics

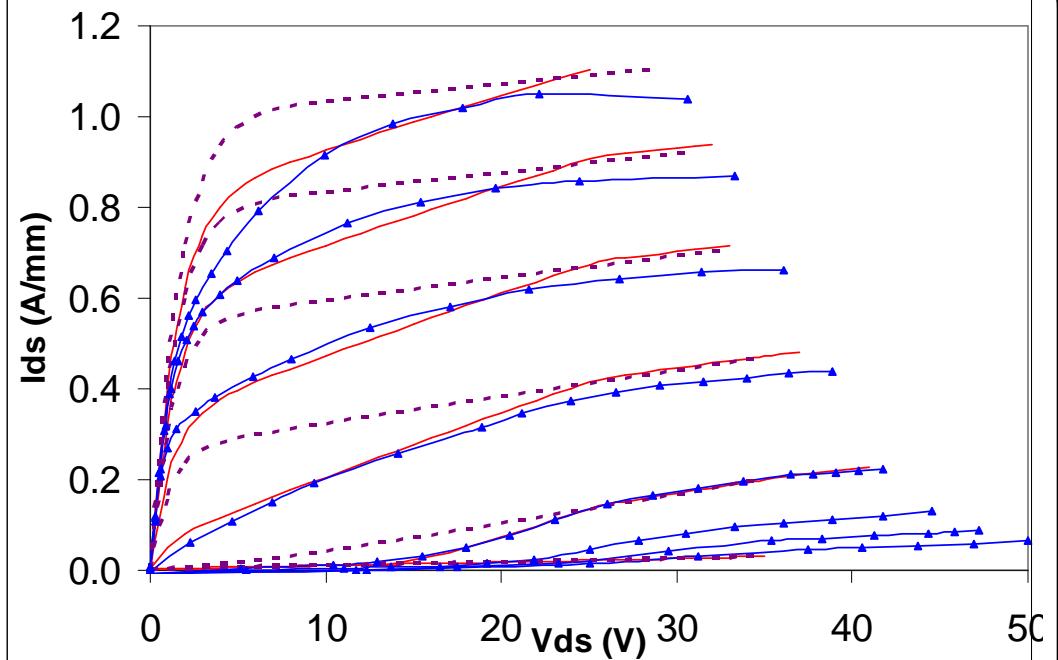
Measured Drain-lag



Pulsed measurements @ quiescent bias points :

- $V_{gs0} = -7V, V_{ds0} = 0V$ (blue)
- $V_{gs0} = -7V, V_{ds0} = 25V$ (red)

Simulations w/wo drain-lag



Simulations @ quiescent bias points :

- $V_{gs0} = -7V, V_{ds0} = 0V$ (dashed)
- $V_{gs0} = -7V, V_{ds0} = 25V$ (red)

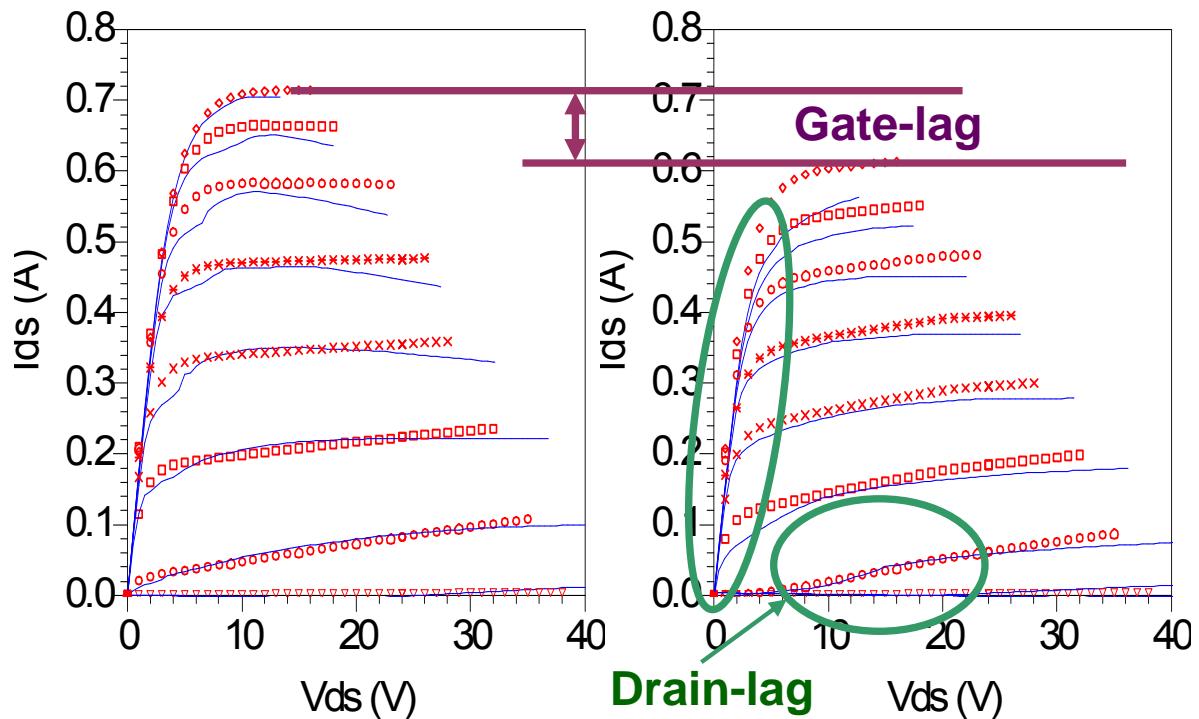
Measure @ $V_{gs0} = -7V, V_{ds0} = 25V$ (blue)

→ Trap model takes into account the changes of the I-V characteristics versus the bias point

Model Validity : IV curves

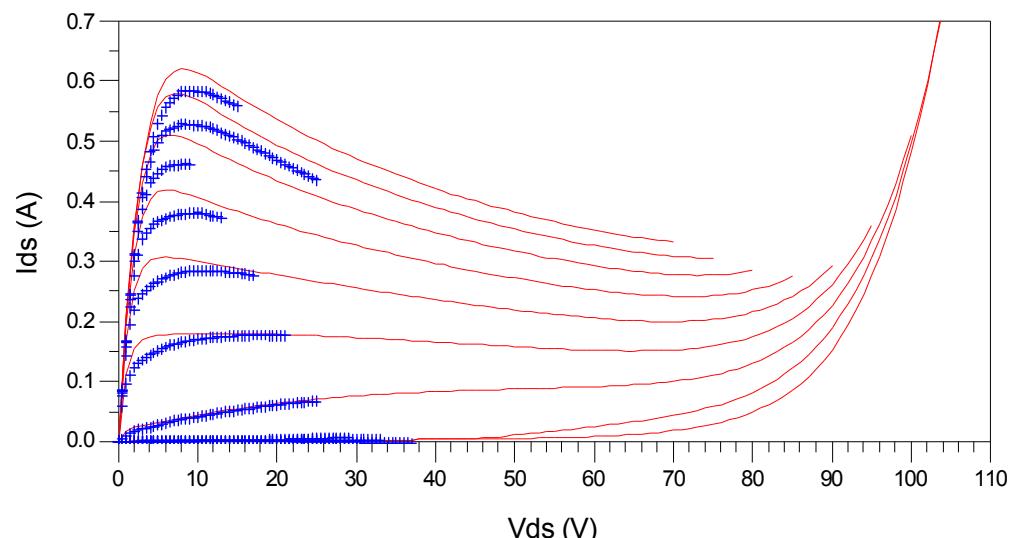
Measurement / Model Comparison
for a pulsed bias point @ several
quiescent bias points

- Current source validation
- Traps



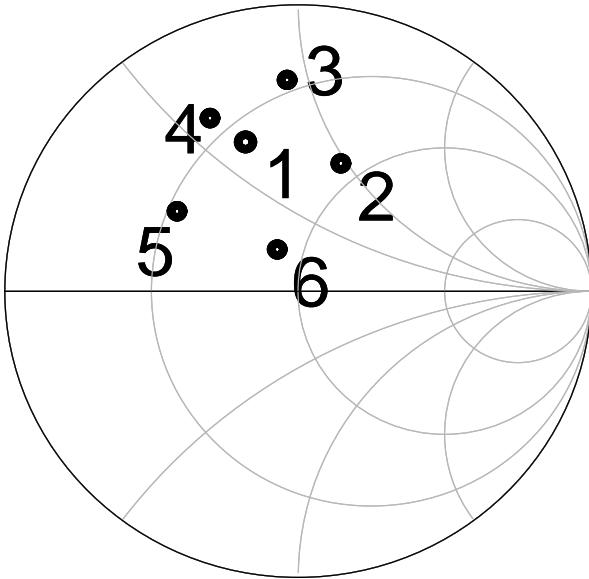
Measurement / Model Comparison
for a DC bias point

- Thermal behavior validation
- Breakdown



Model Validity : Large Signal

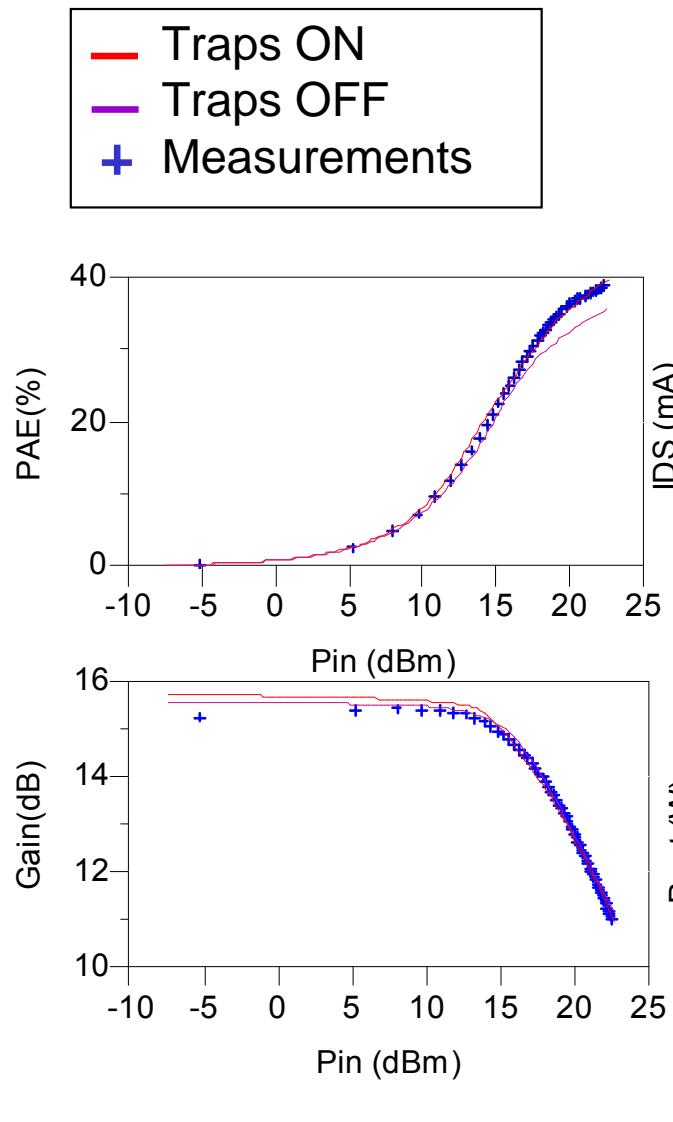
Load-Pull measurements to check the model accuracy



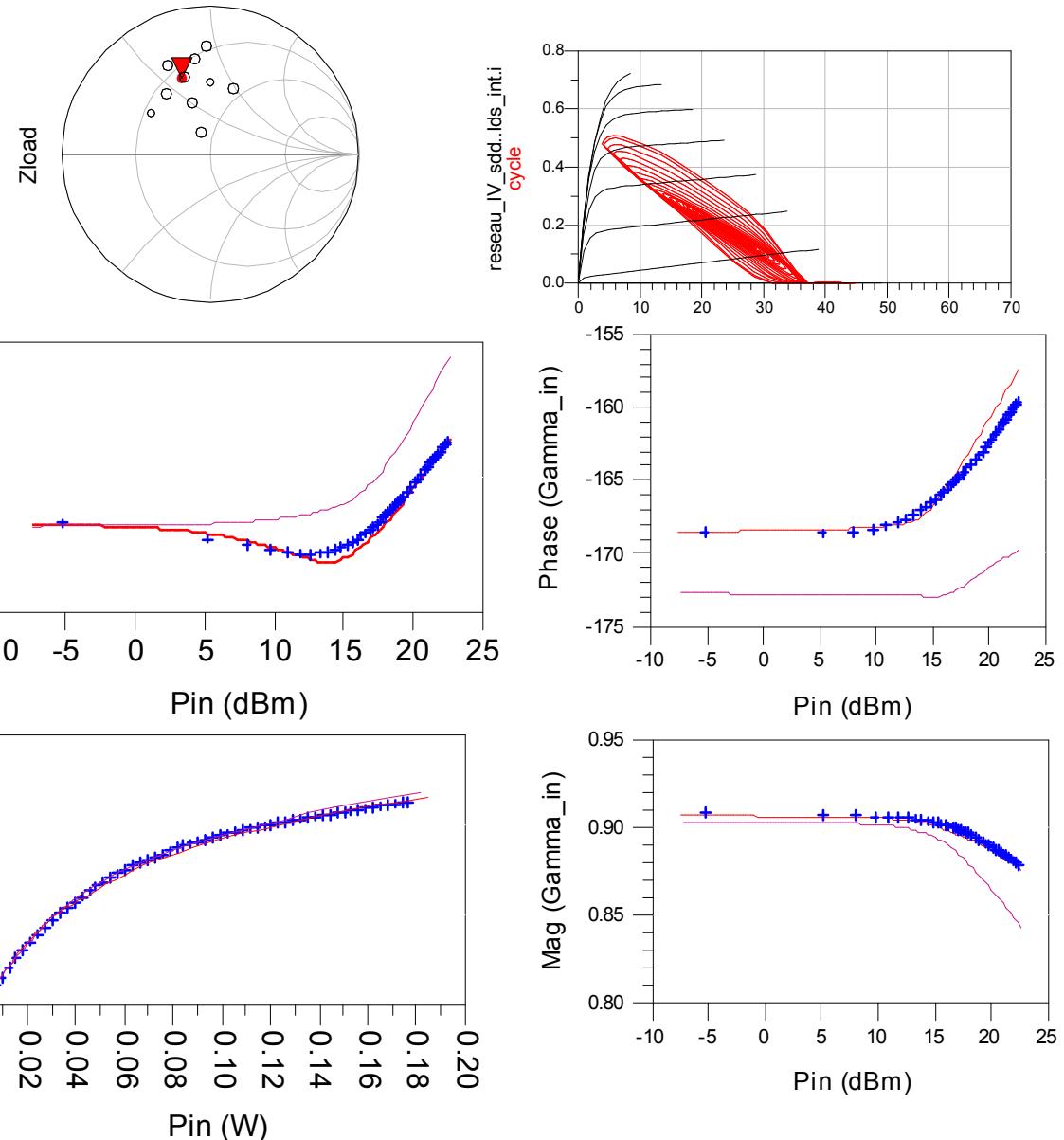
- 1 : Z_{OPT}
- 2 : $Z_2 \text{ VSWR}=2.5$
- 3 : $Z_3 \text{ VSWR}=2.5$
- 4 : $Z_4 \text{ VSWR}=1.6$
- 5 : $Z_5 \text{ VSWR}=2.5$
- 6 : $Z_6 \text{ VSWR}=2.5$

Class AB, Vds=25 V , DC Bias, CW RF, 10 GHz

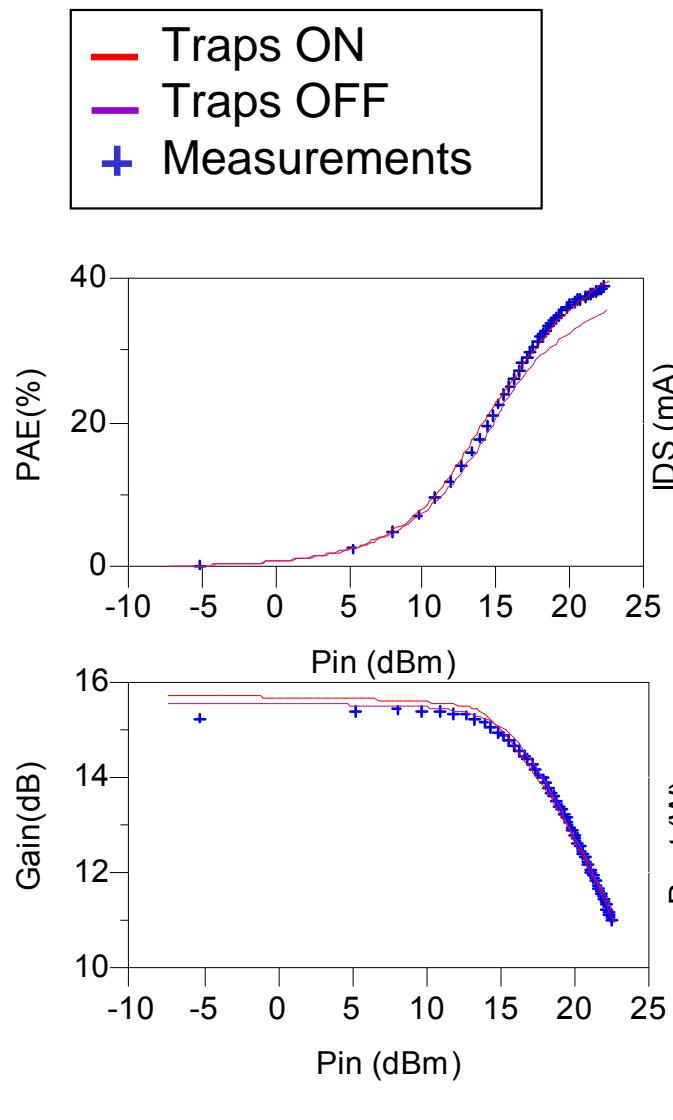
Model Validity : Large Signal



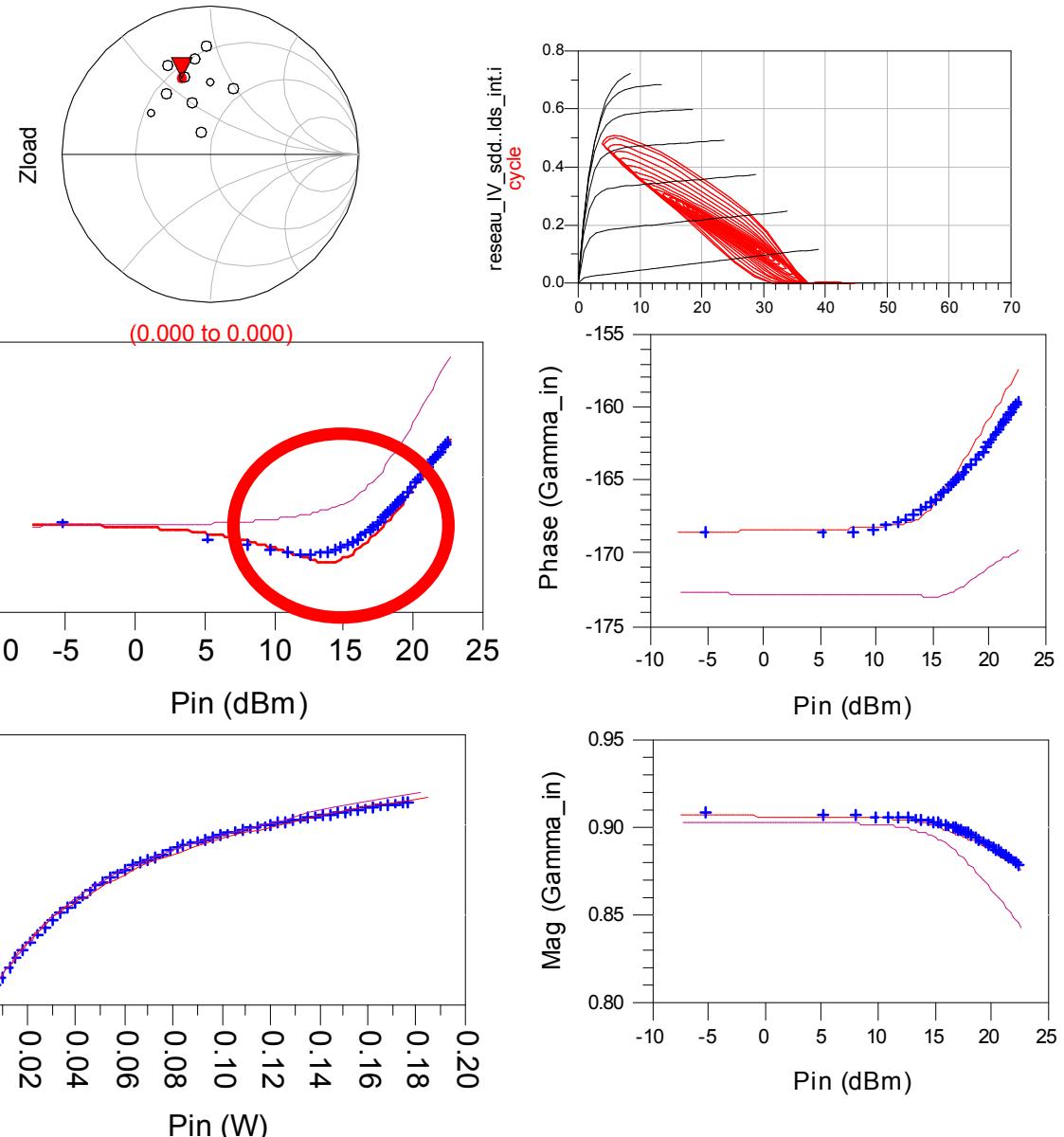
Measurements @ power optimal load impedance



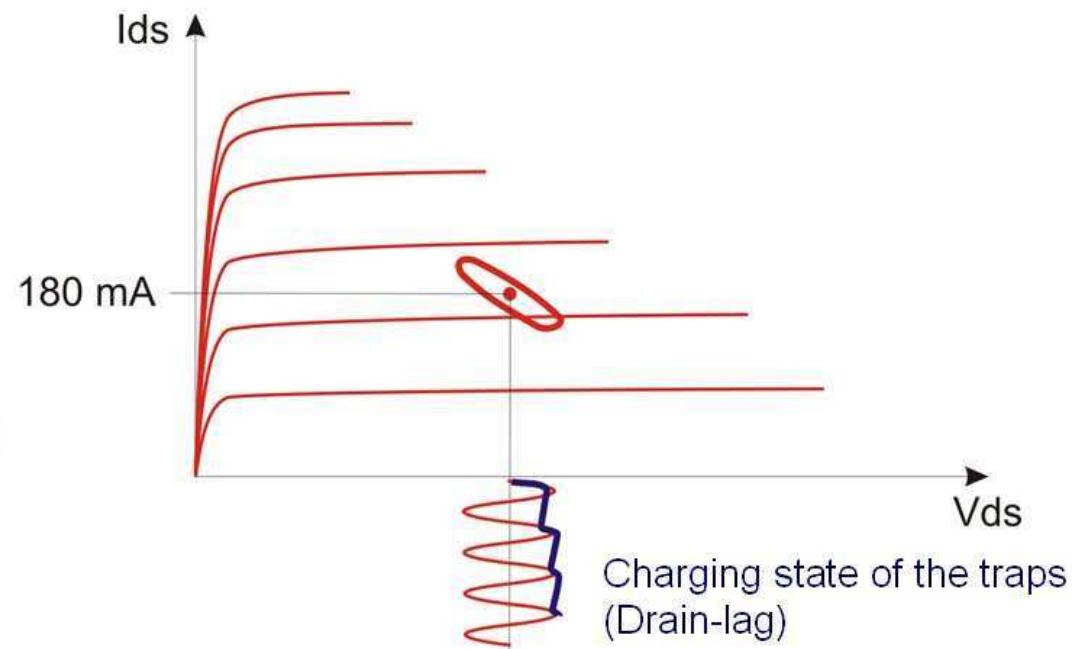
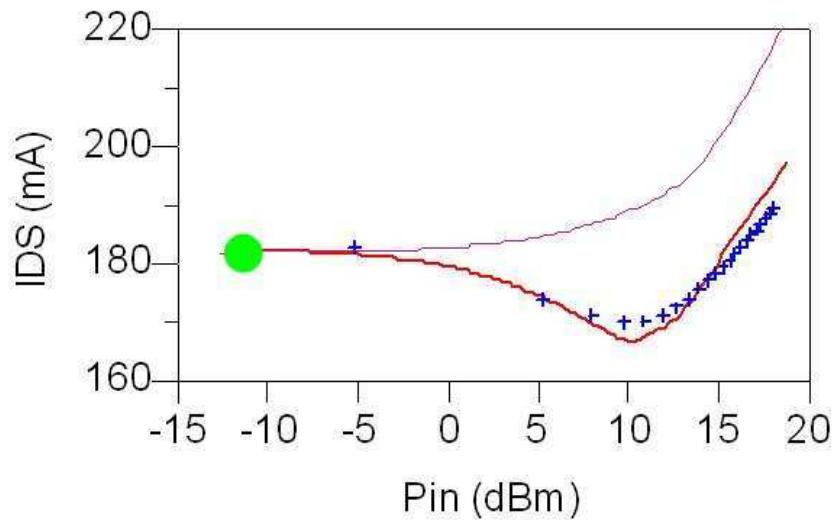
Model Validity : Large Signal



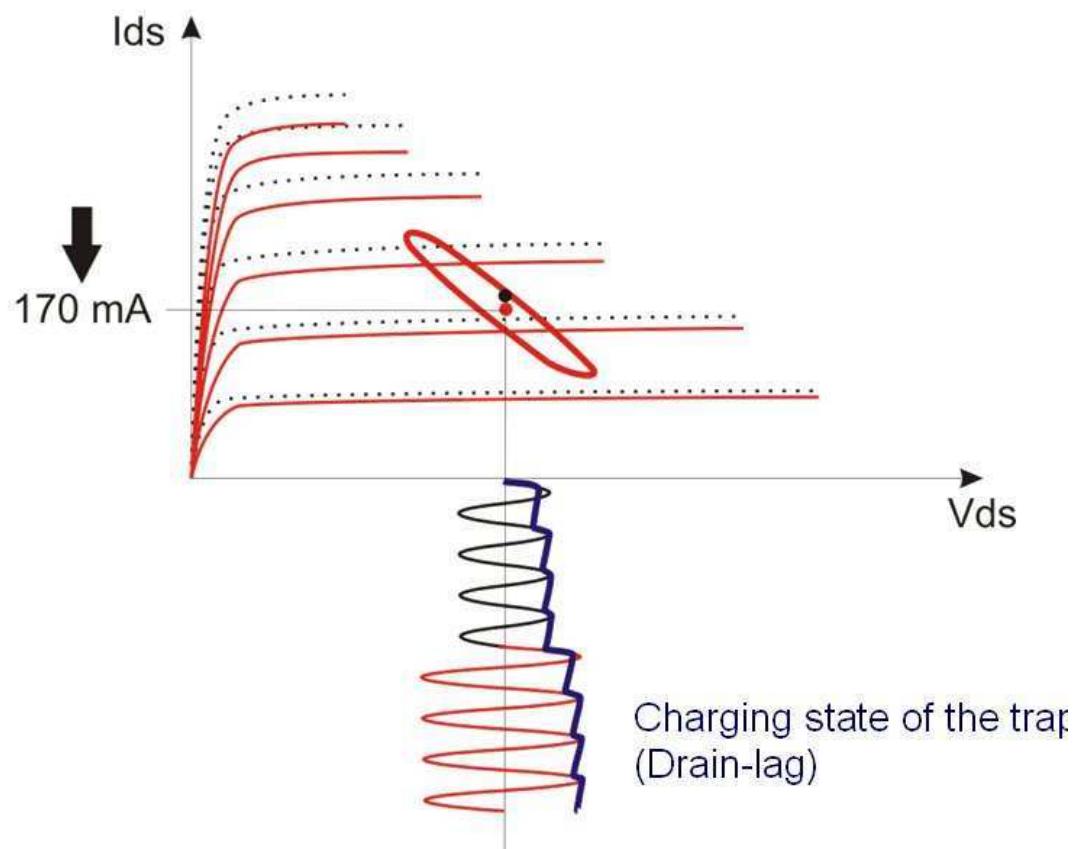
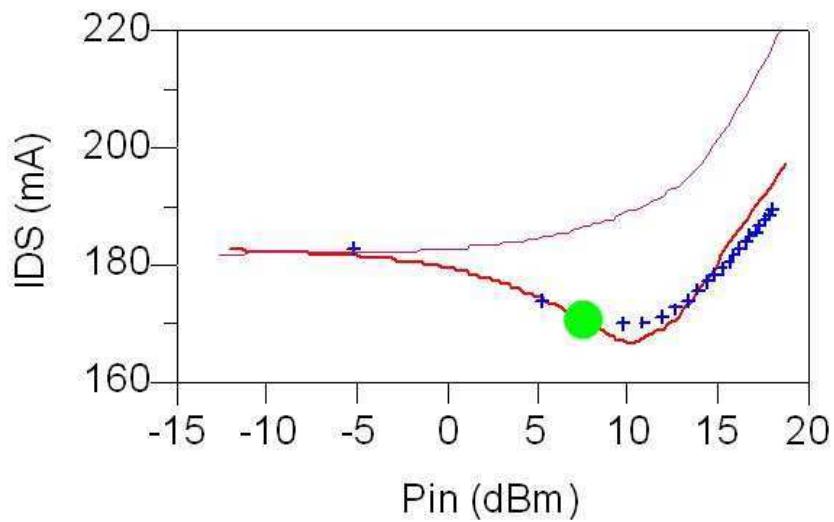
Measurements @ power optimal load impedance



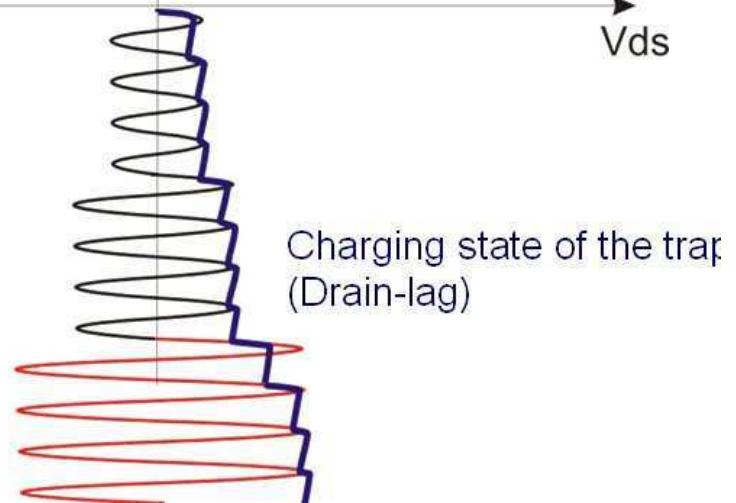
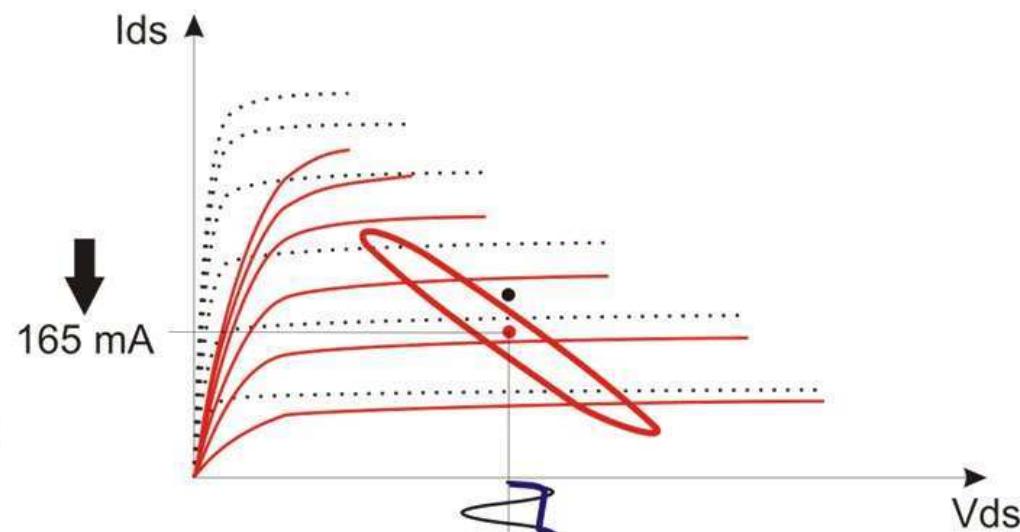
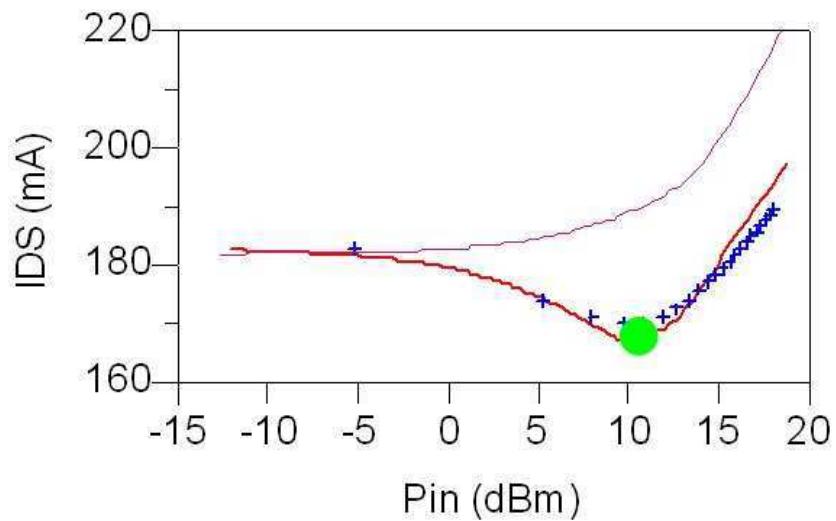
The current slope phenomenon



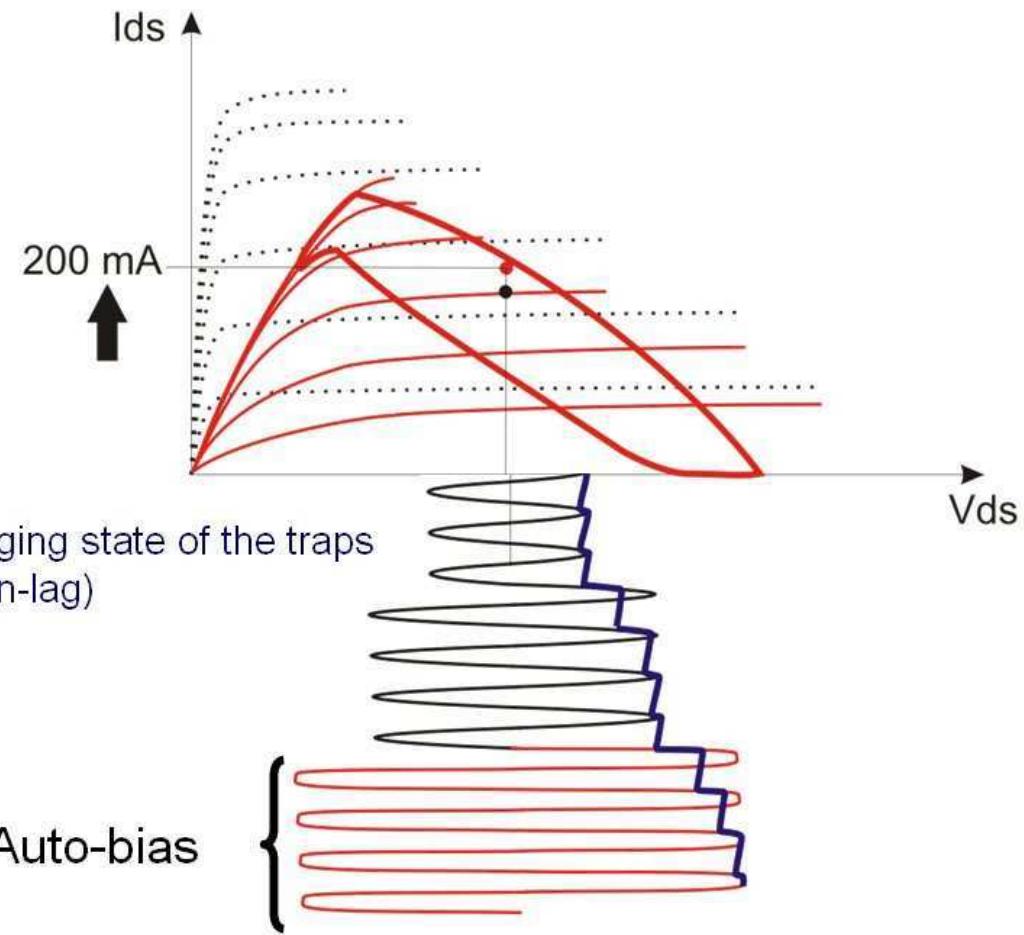
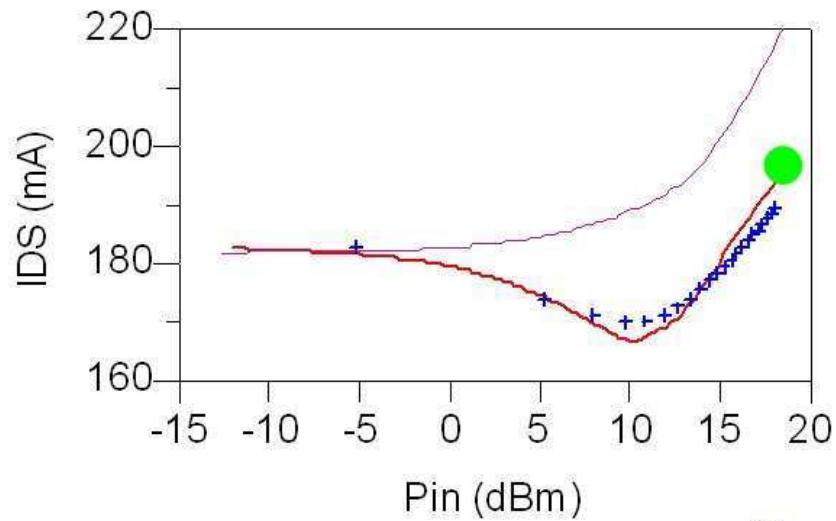
The current slope phenomenon



The current slope phenomenon

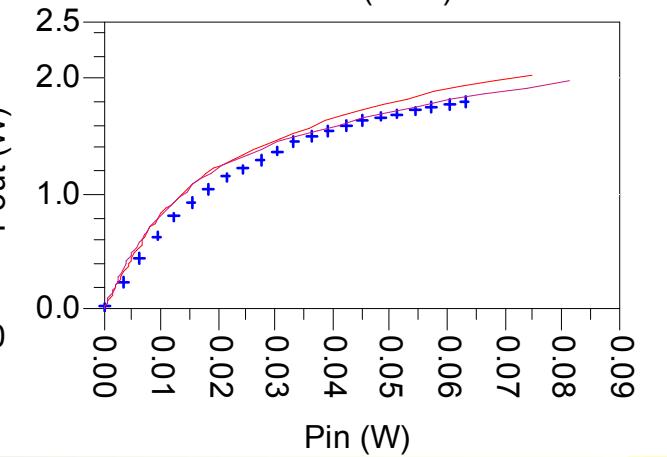
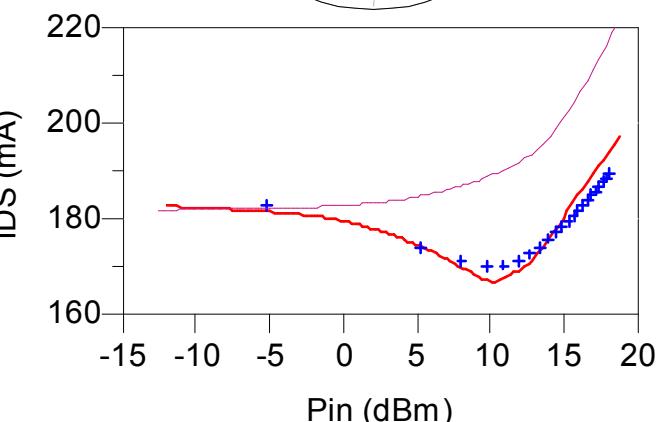
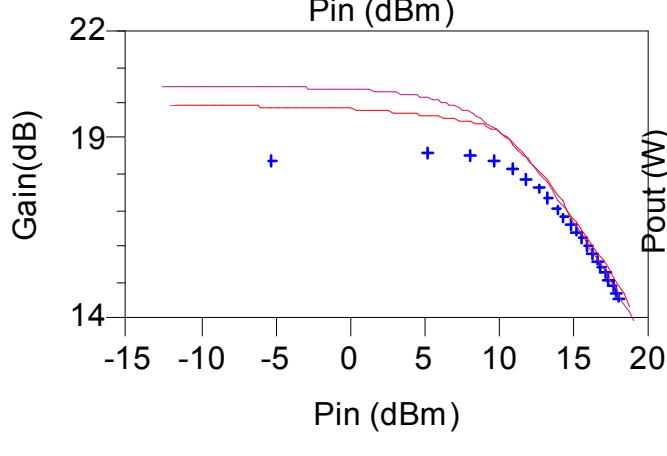
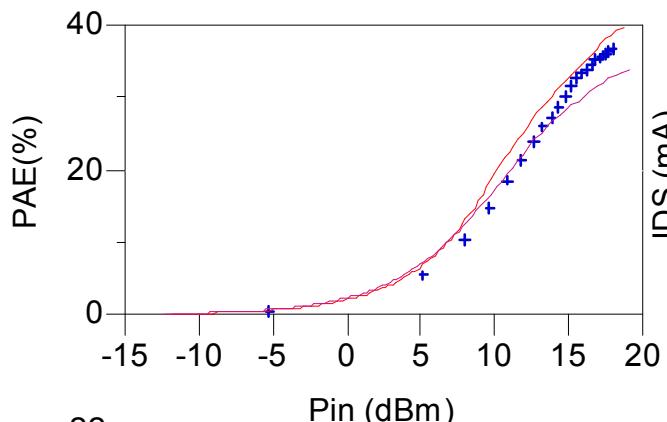


The current slope phenomenon

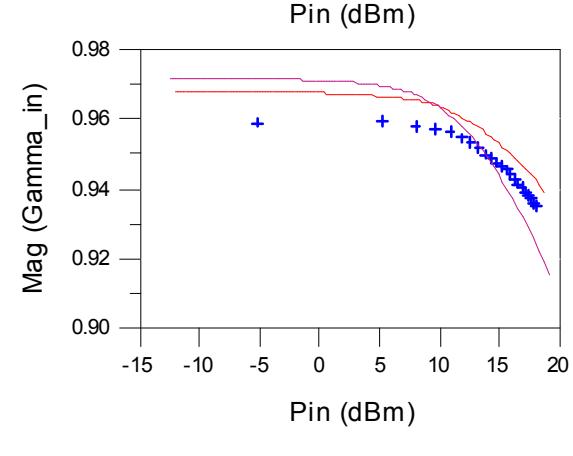
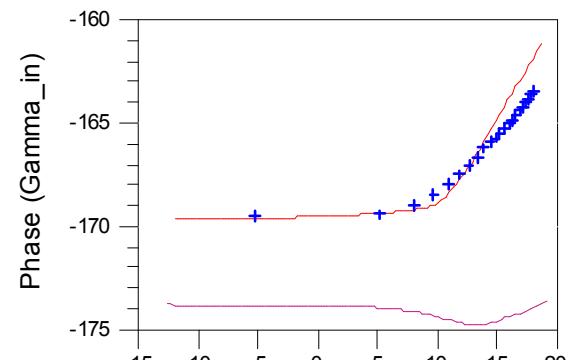
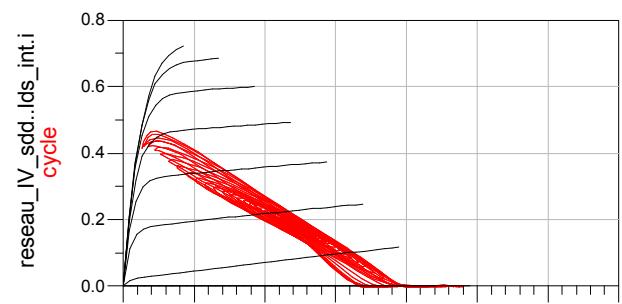
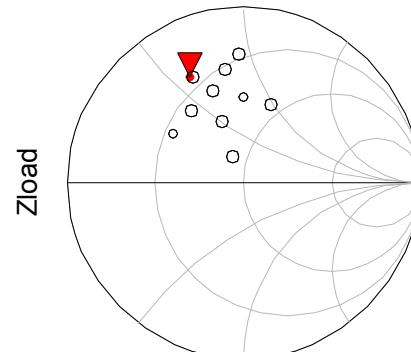


Model Validity : Large Signal

- Traps ON
- Traps OFF
- + Measurements

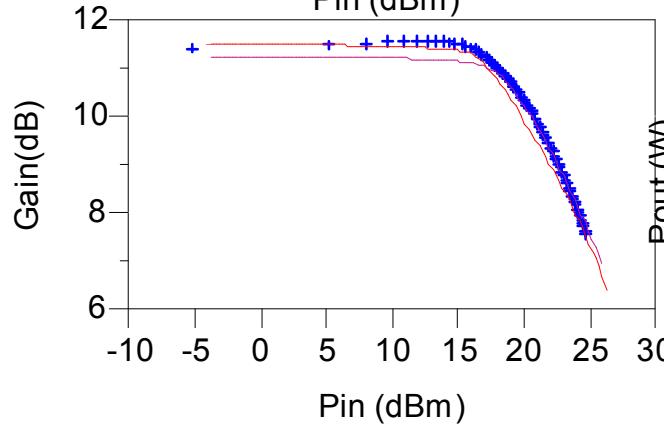
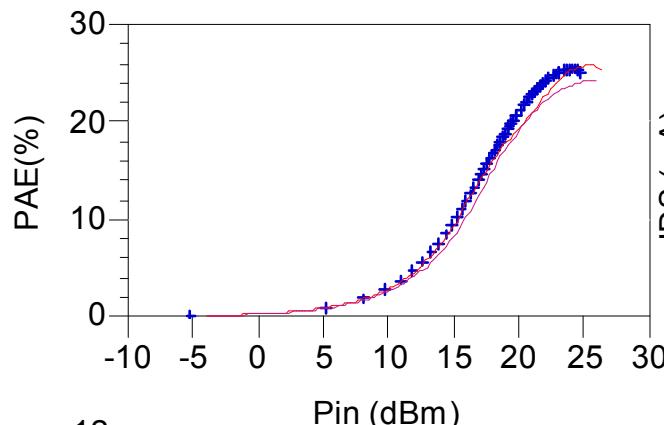


Measurements @ VSWR = 1.6

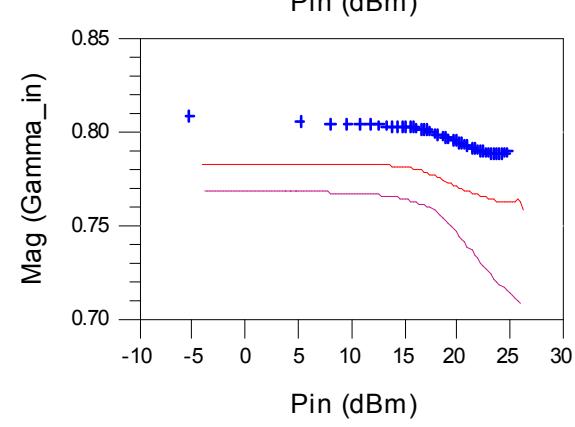
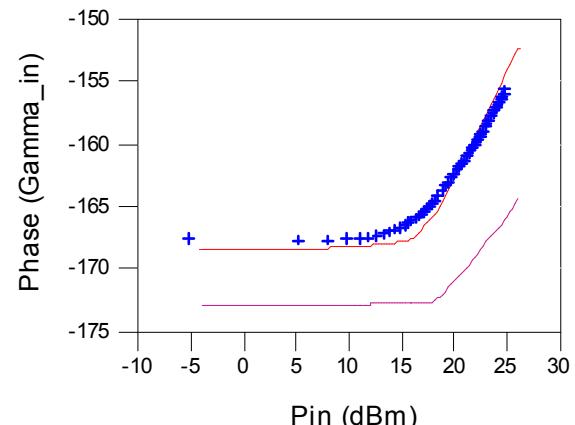
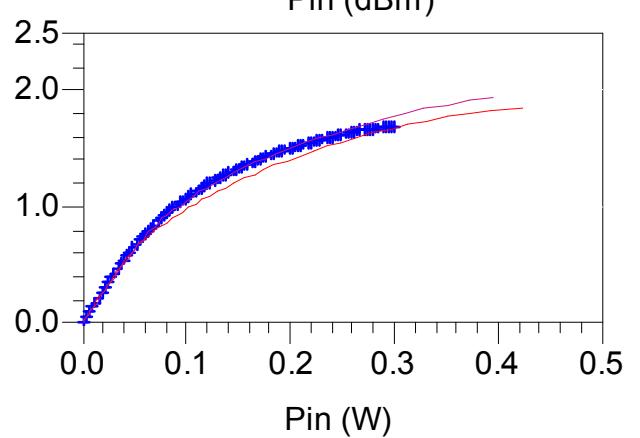
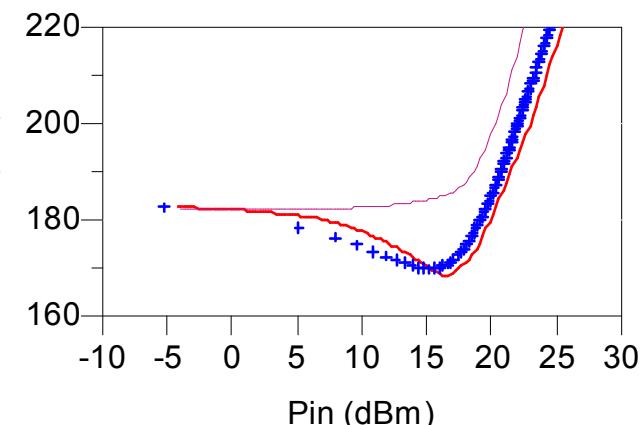
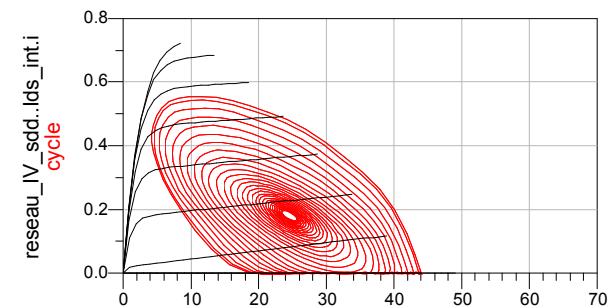
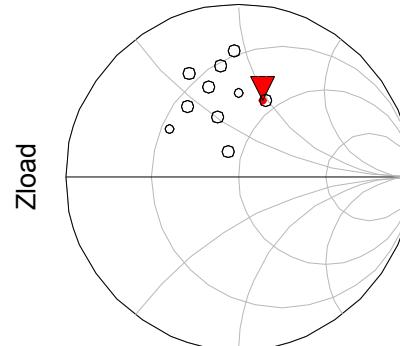


Model Validity : Large Signal

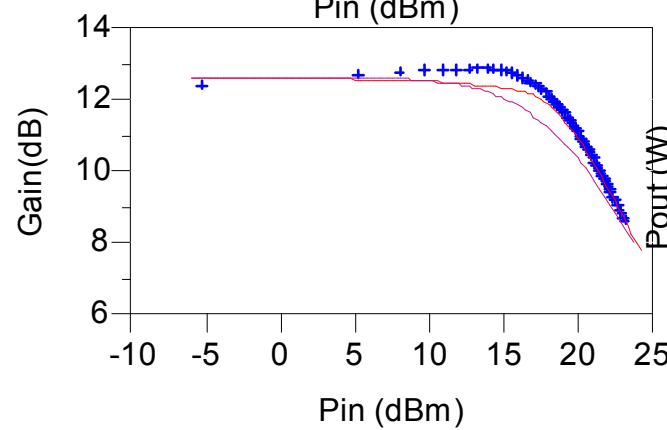
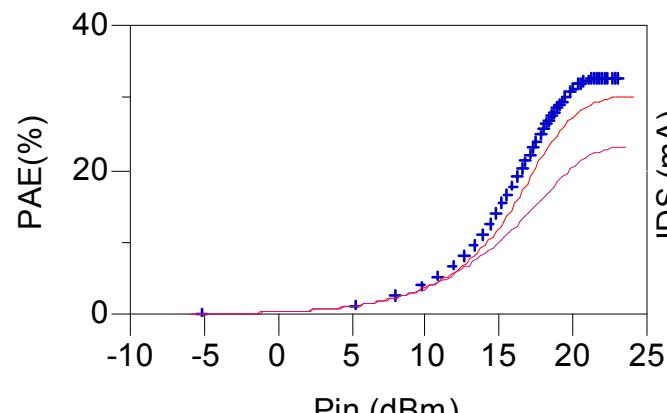
- Traps ON
- Traps OFF
- + Measurements



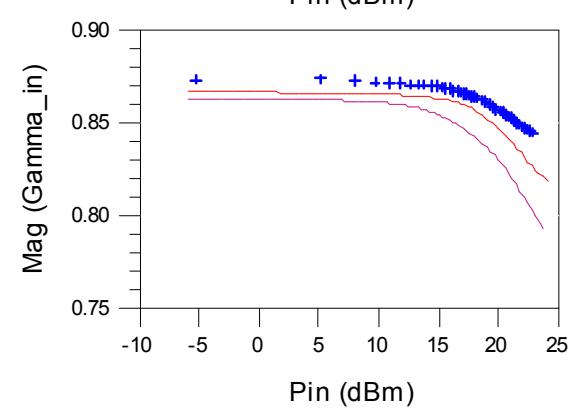
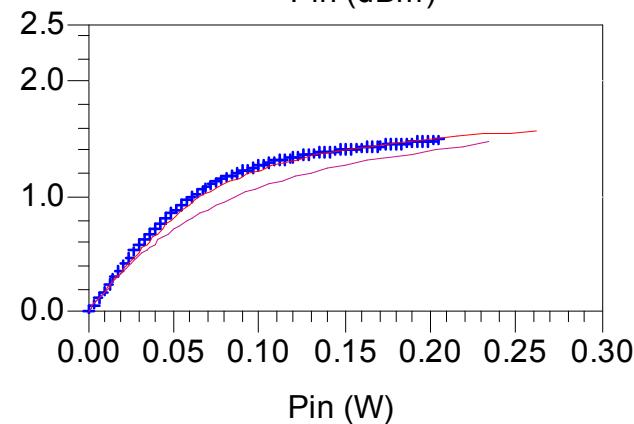
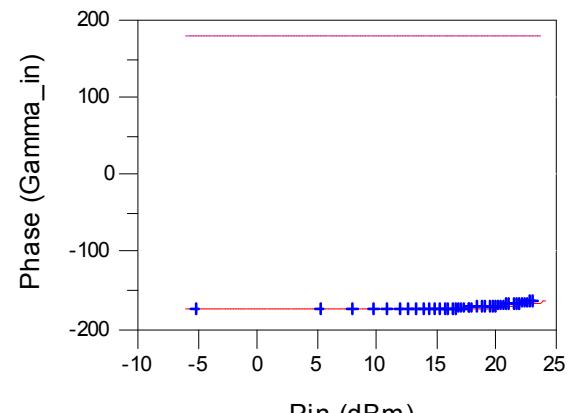
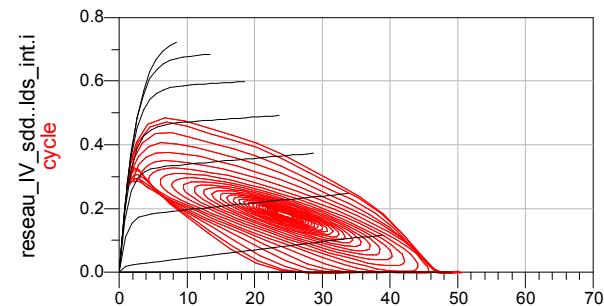
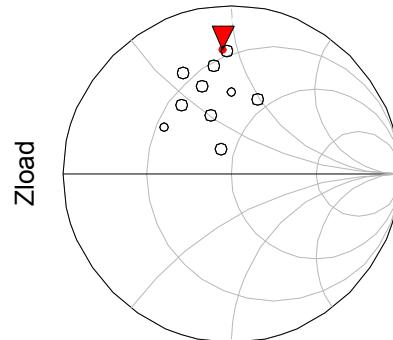
Measurements @ VSWR = 2.5



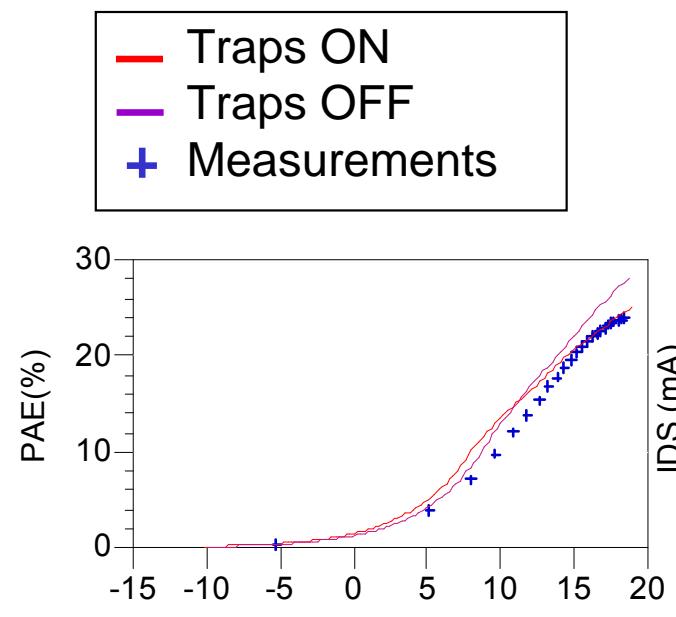
Model Validity : Large Signal



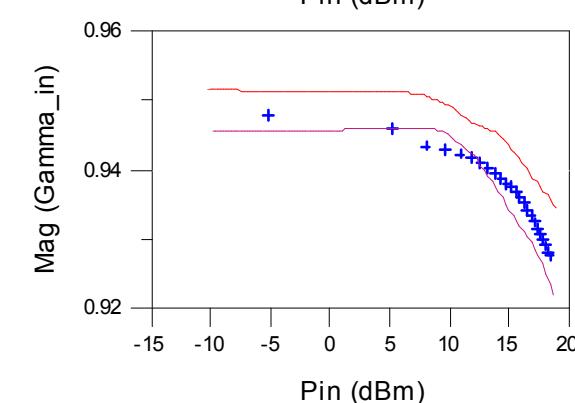
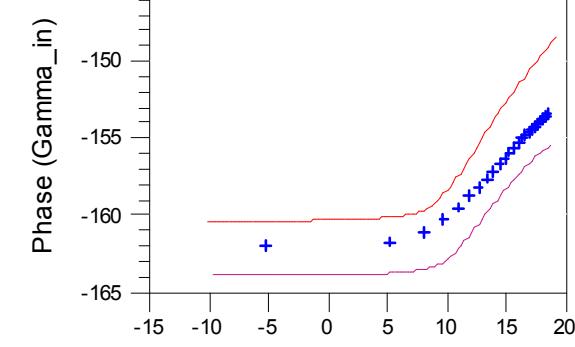
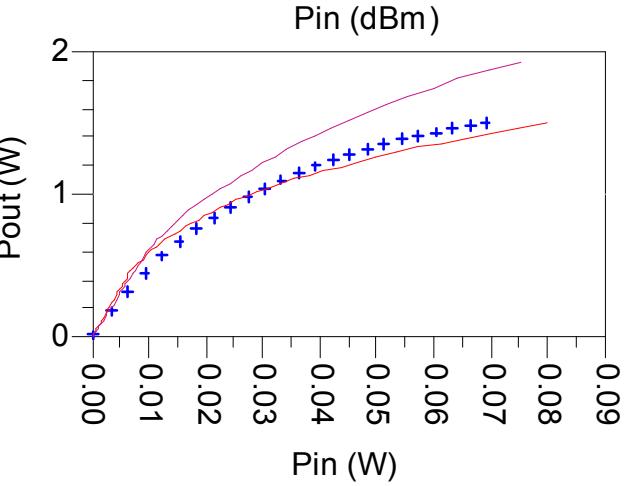
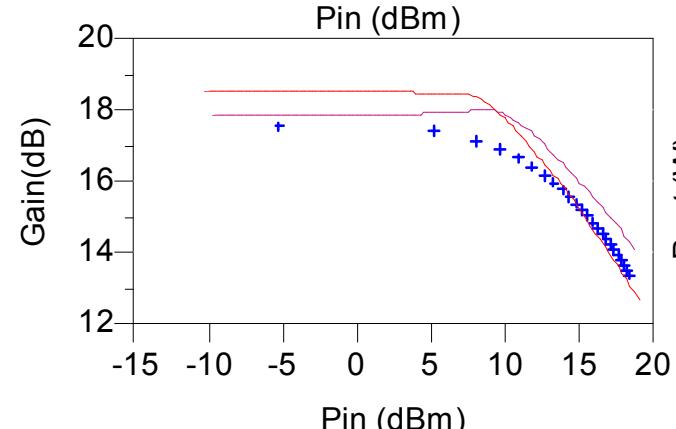
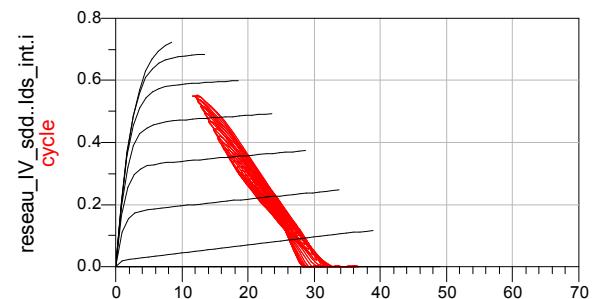
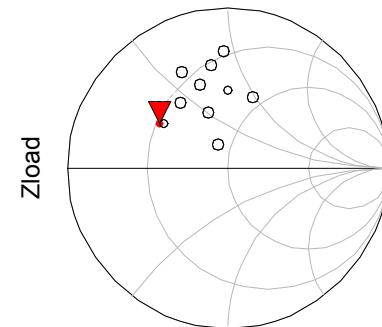
Measurements @ VSWR = 2.5



Model Validity : Large Signal

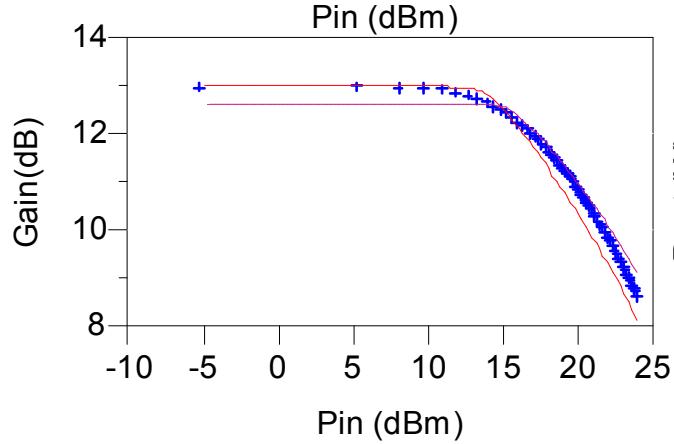
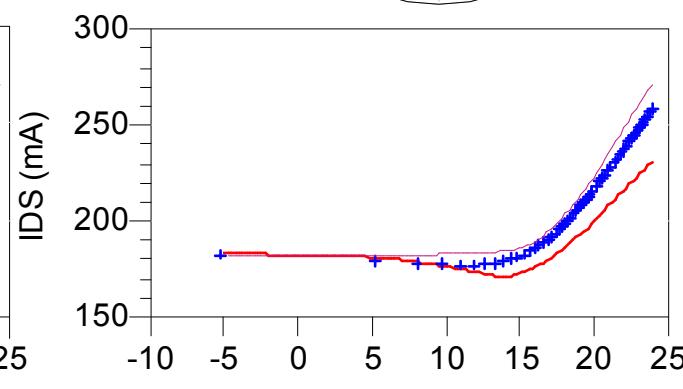
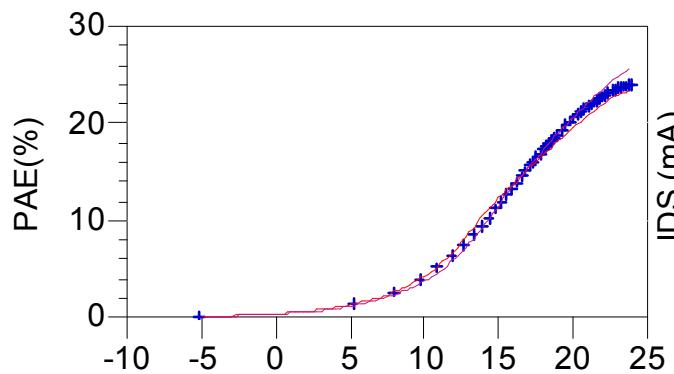


Measurements @ VSWR = 2.5

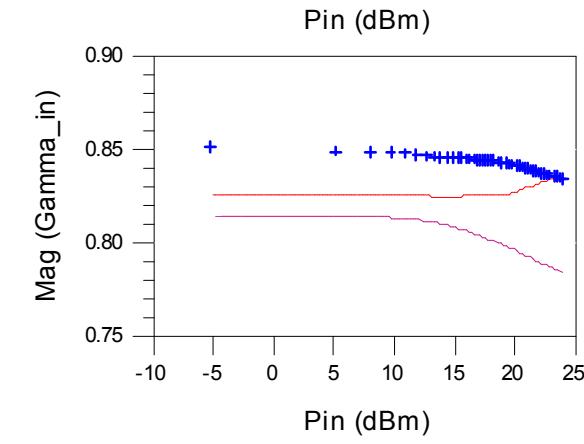
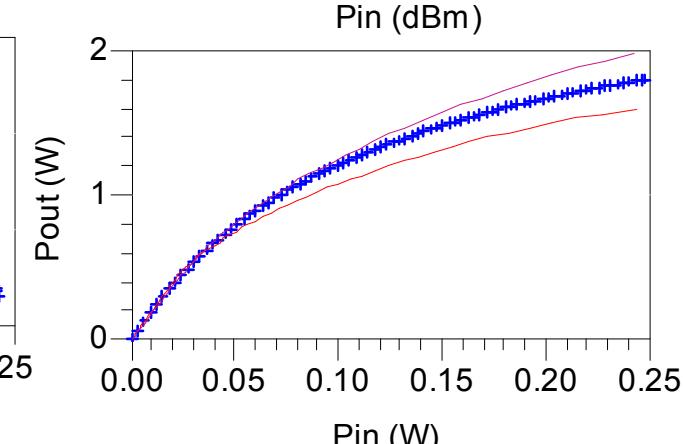
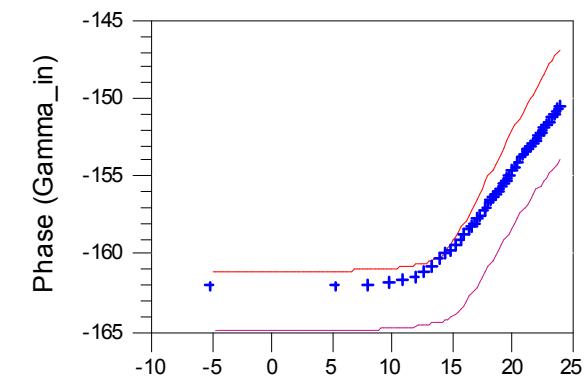
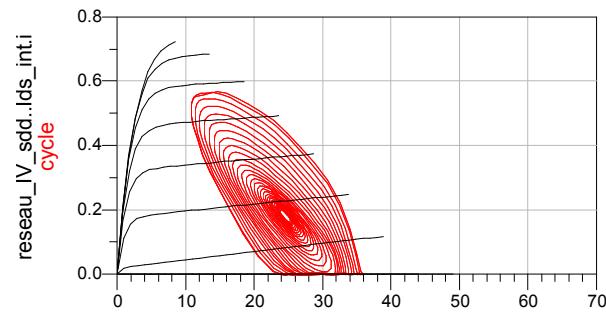
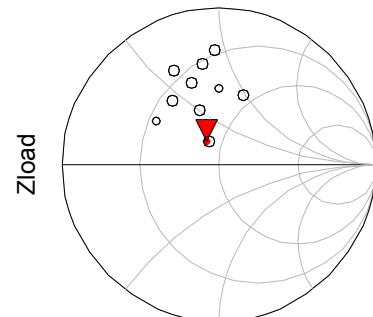


Model Validity : Large Signal

- Traps ON
- Traps OFF
- + Measurements

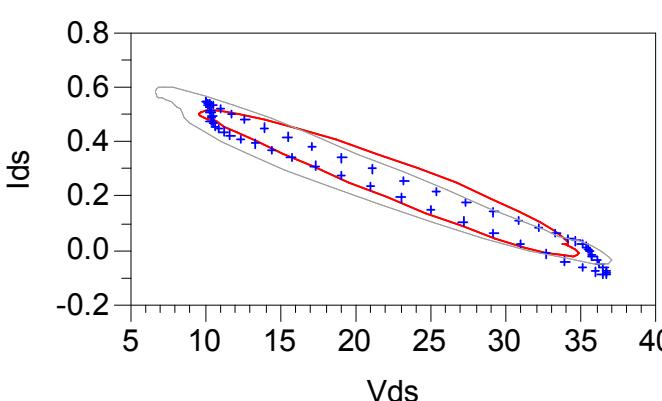
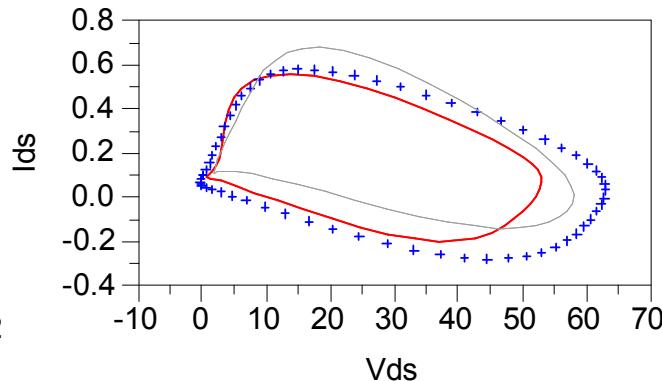
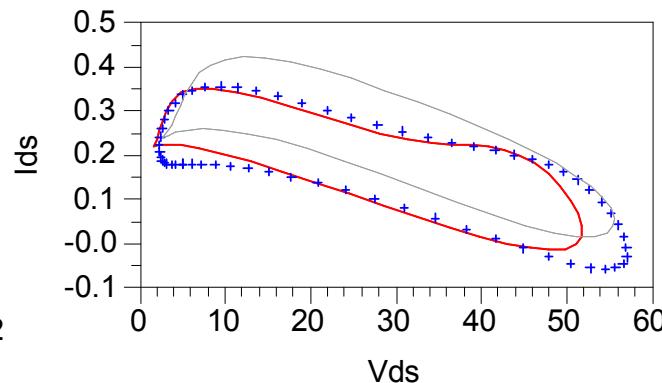
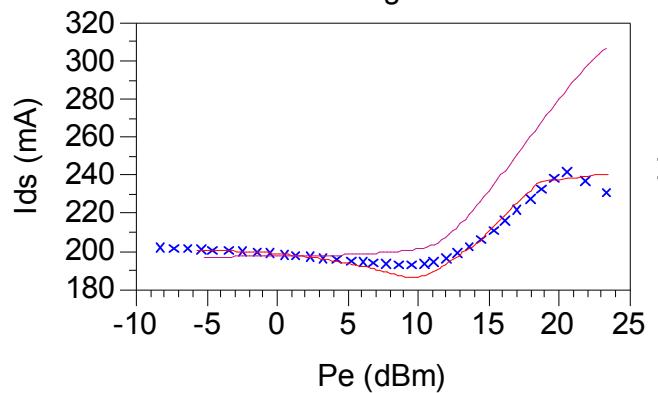
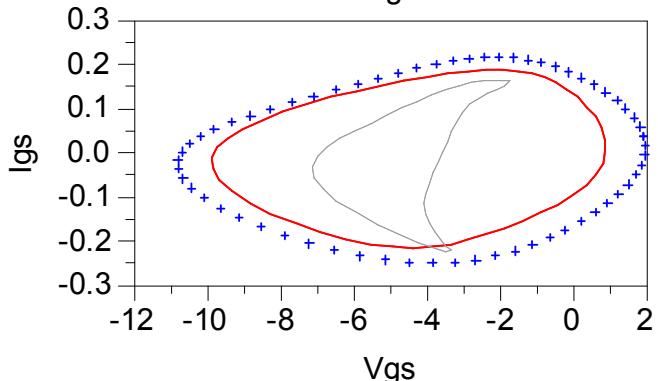
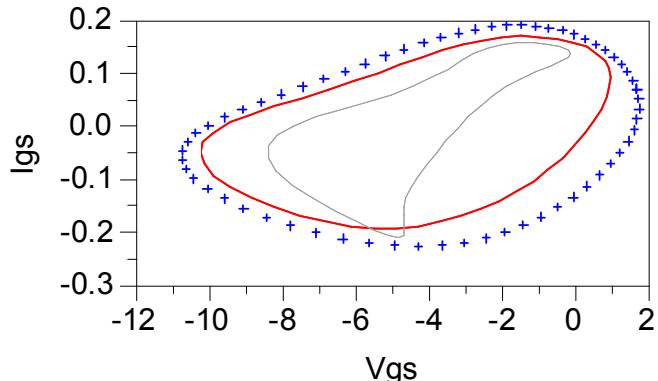


Measurements @ VSWR = 2.5



Model Validity : Large Signal

Time Domain Load-Pull @ 5 GHz, 25V, DC Bias / CW RF



— Traps ON
— Traps OFF
+ Measurements

VSWR = 4

5dB Gain comp.

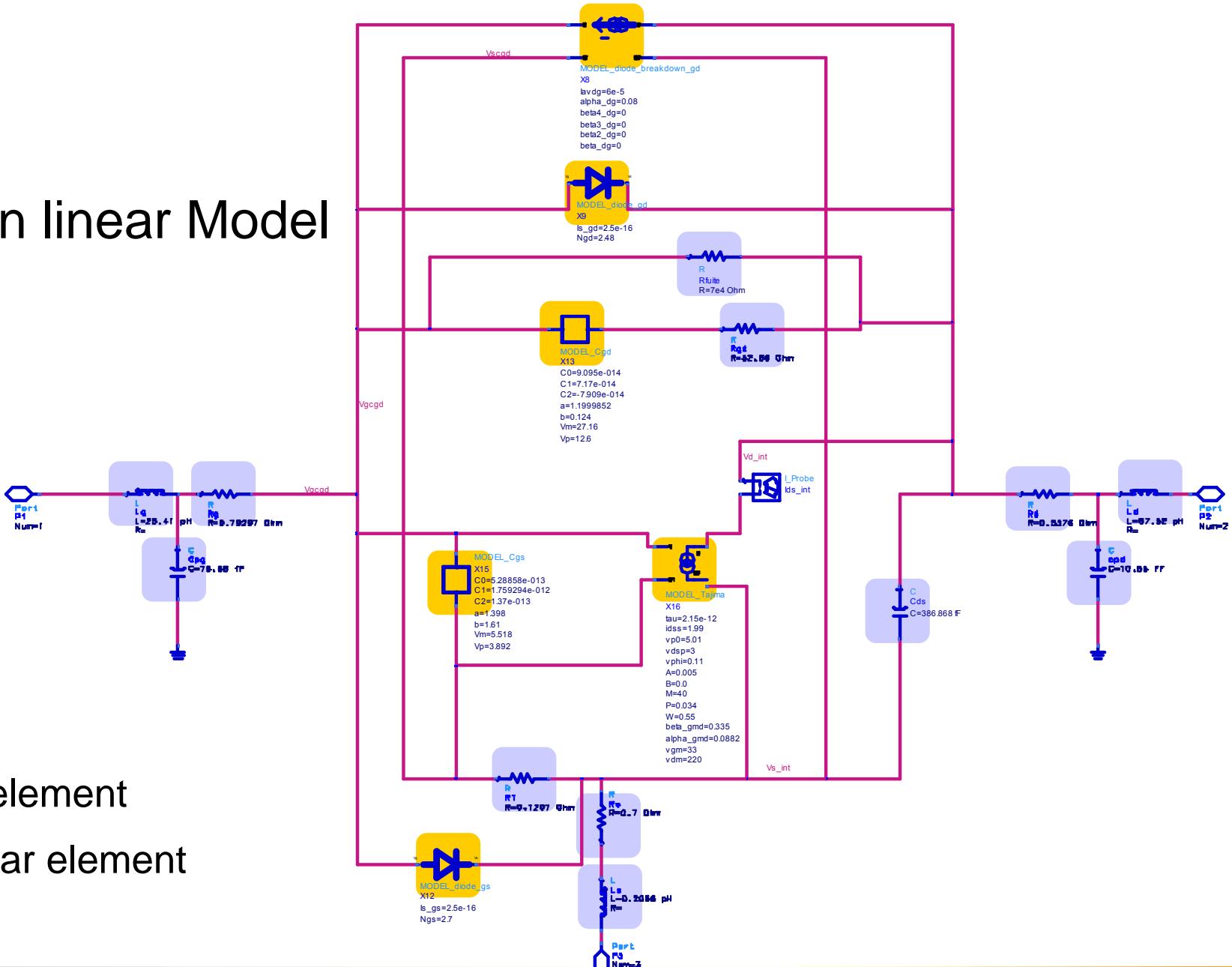
VSWR = 3.3

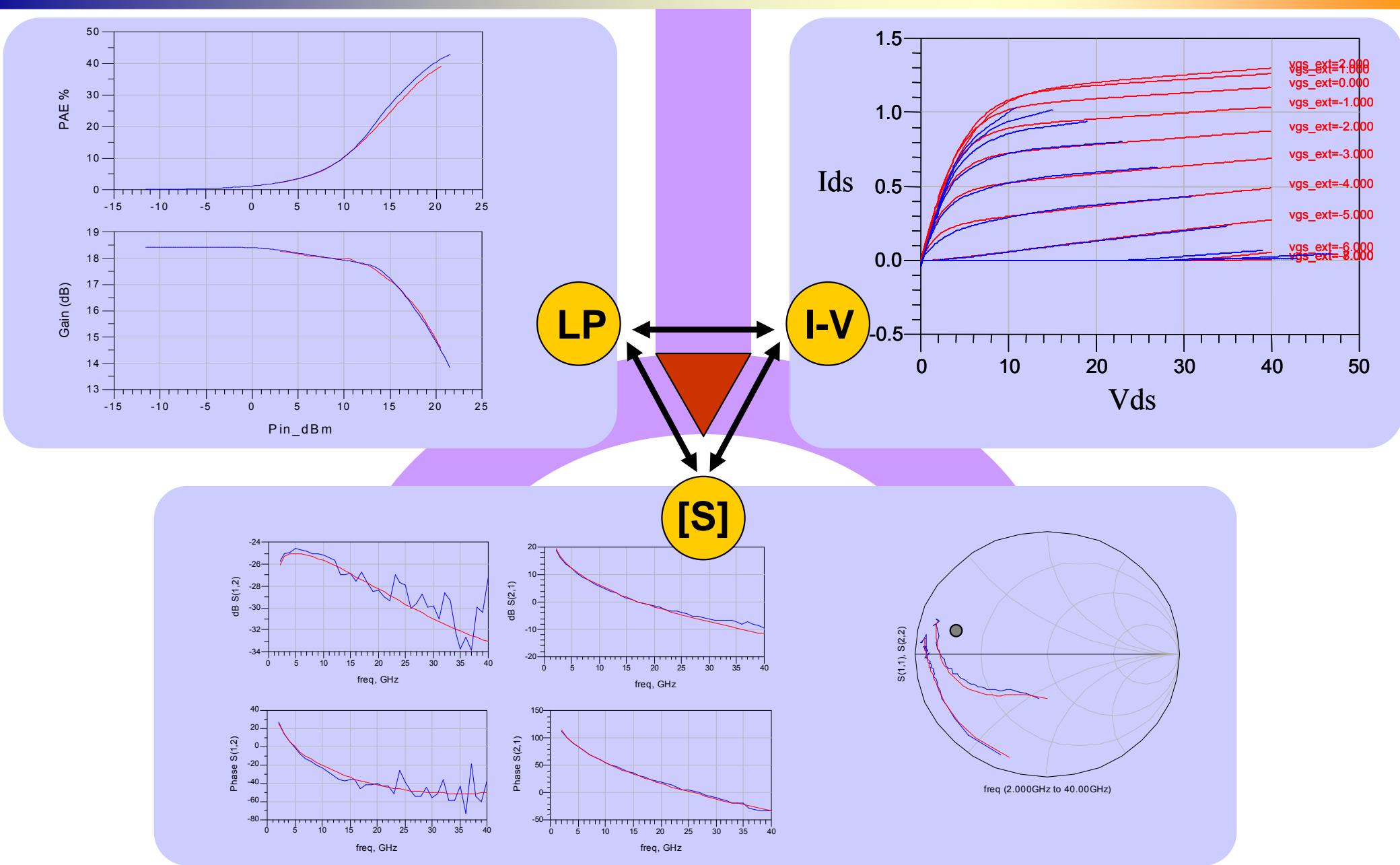
7dB Gain comp.

VSWR = 2

8dB Gain comp.

Classical Non linear Model

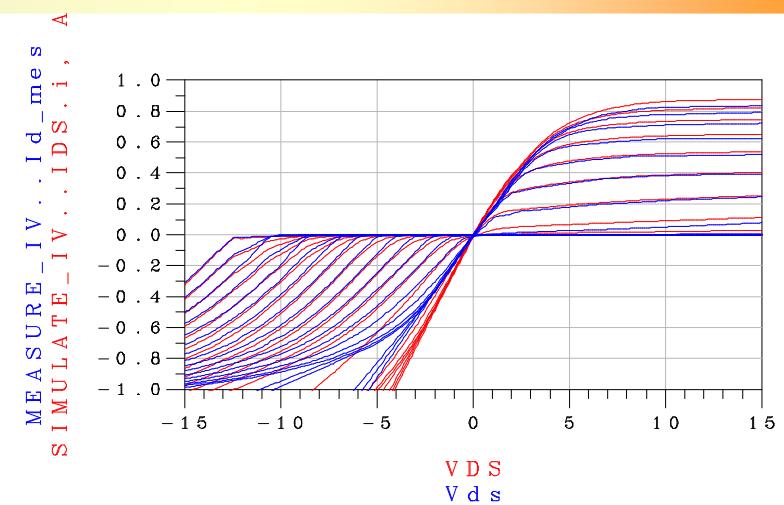
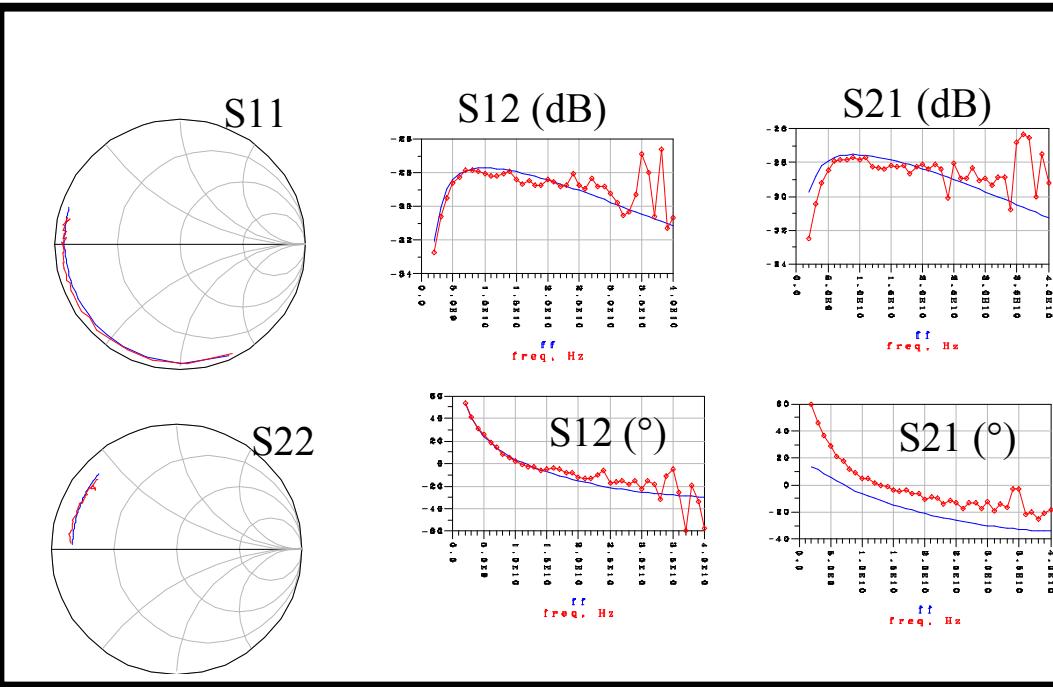




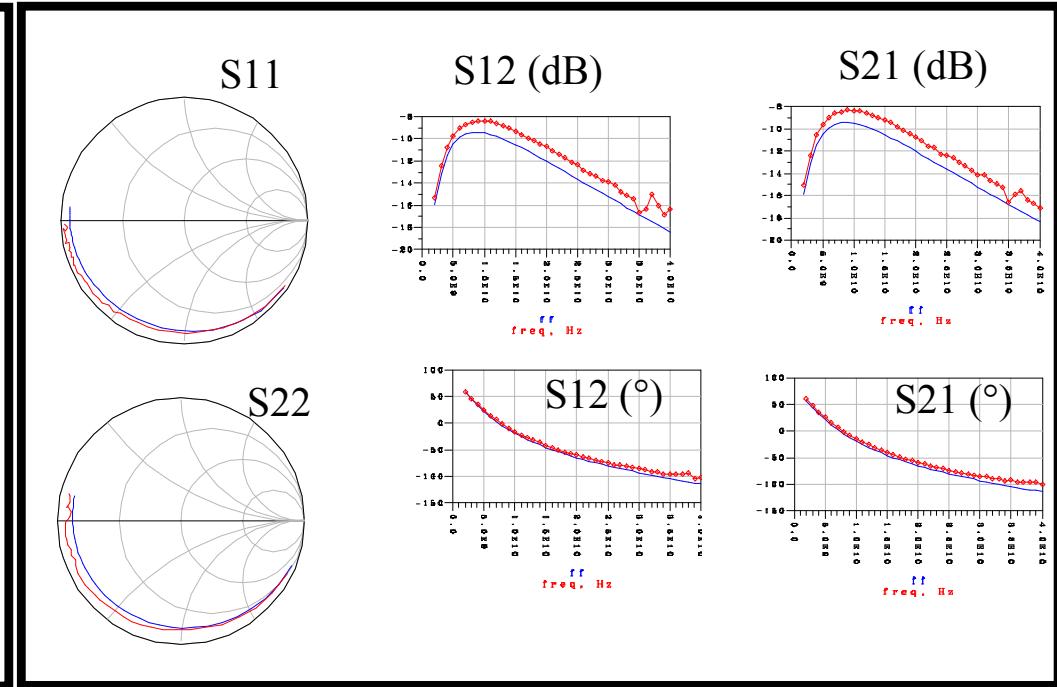
Cold FET Model for Switches Application

The source current is a table model

$$V_{gs} = +1V / V_{ds} = 0V$$



$$V_{gs} = -12V / V_{ds} = 0V$$



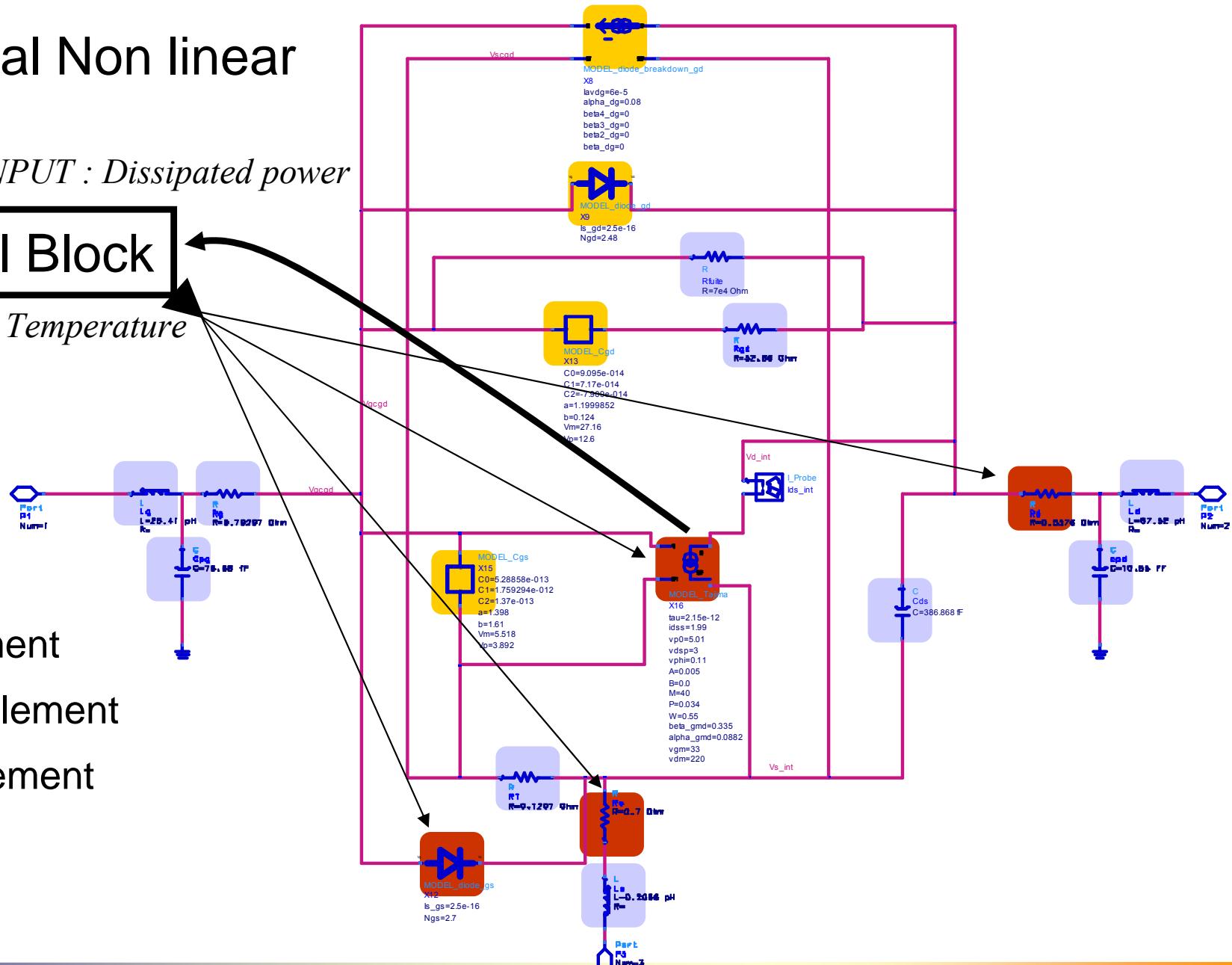
Electro-thermal Non linear Model

INPUT : Dissipated power

Thermal Block

OUTPUT : Temperature

-  Linear element
-  Nonlinear element
-  Thermal element



Conclusion



UNIVERSITÀ DEGLI STUDI DI ROMA
UTorVergata
Università

Measured by	Model	Note	Foundry	Techno	Transistor	Application	Design Team	EDA
XLIM	Nonlinear		Tiger	CPW	AEC1148 - 12x100	HPA (X-band)	TIGER	 ADS
XLIM	Nonlinear (+thermal)		Tiger	CPW	AEC1148 - 8x75	HPA (X-band)	TIGER	 ADS
XLIM	Nonlinear	for 4x250 interpolation	QinetiQ	CPW	Gibson - 2x250	HPA (Wideband 2-6 GHz)	INDRA	 ADS
XLIM	Cold FET	Release #2	Tiger	CPW	AEC1148 - 8x75	SPDT (X-band)	TIGER	 ADS
XLIM	Nonlinear		QinetiQ	CPW	Gibson - 8x250	HPA (S-band)	BAE	 ADS
XLIM	Nonlinear		QinetiQ	CPW	Iona - 8x125 (type Z)	HPA (Wideband 6-18 GHz)	INDRA	 ADS
XLIM	Nonlinear		Tiger	CPW	KQ031 - 12x100	HPA (X-band)	TIGER	 ADS
XLIM	Nonlinear		QinetiQ	CPW	Iona - 8x75	HPA (Wideband 6-18 GHz)	SLX_UK	 ADS
XLIM	Cold FET		QinetiQ	CPW	Iona - 8x75	SPDT (X-band)	TNO	 ADS
XLIM	Nonlinear (+trapping)		Tiger	CPW	KQ031 - 16x100	HPA (X-band)	UMS	 ADS
XLIM	Cold FET	Release #2	Tiger	CPW	KQ031 - 12x100	SPDT (X-band)	TNO / ELT	 ADS
XLIM	Nonlinear		Tiger	CPW	KQ031 - 16x140	HPA (X-band)	UMS	 ADS
XLIM	Nonlinear (+trapping)	40V Class B	Tiger	CPW	LO892 - 8x250	HPA (S-band)	SAAB	 ADS
XLIM	Nonlinear (+trapping)	25V Class B	Tiger	CPW	LO892 - 8x250	HPA (S-band)	SAAB	 ADS
XLIM	Nonlinear (+thermal +trapping)	Class B @ 25V	Tiger	CPW	LO892 - 8x250	HPA (S-band)	SAAB	 ADS
XLIM	Nonlinear	compiled model @ 15V	QinetiQ	CPW	Endeavour - 4x50	LNA (Wideband)	SLX_UK / TNO	 ADS
XLIM	Nonlinear		QinetiQ	CPW	Endeavour - 8x75	LNA (Wideband)	SLX_UK / TNO	 ADS
TVR	Noise		Selex-SI CPW	SLX19_2212 - 4x75	LNA (X-band)	SLX-SI	 ADS	- 8x125 (SPDT Configuration) SPDT (Wideband)
TVR	Noise		Selex-SI CPW	SLX19_2212 - 2x50	LNA (X-band)	SLX-SI	 ADS	- 2x125 LNA (Wideband)
TVR	Noise		QinetiQ CPW	Iona - 8x75	LNA (Wideband)	SLX-UK / TDL	 ADS	- 2x125 HPA (Wideband 6-18 GHz) TDL
TVR	Noise		QinetiQ CPW	Iona - 2x50	LNA (X-band)	TNO	 ADS	- 2x125 HPA (Wideband 6-18 GHz) TDL
TVR	Nonlinear	Nonlinear measurements from PTO have been used [Release #2]	Selex-SI CPW	SLX19_2212 - 10x100	HPA (X-band)	SLX-SI	 AWR	- 8x125 (SPDT Configuration) SPDT (Wideband)
TVR	Nonlinear	Nonlinear measurements from PTO have been used	Selex-SI CPW	AMS04_1111 - 12x100	HPA (Wideband 2-6 GHz)	INDRA	 AWR & ADS	- 2x75 LNA (Wideband)
TVR	Nonlinear	Nonlinear measurements from PTO have been used	Selex-SI CPW	AMS04_1111 - 10x100	HPA (Wideband 2-6 GHz)	INDRA	 AWR & ADS	- 2x75 LNA (Wideband)
TVR	Nonlinear	Nonlinear measurements from PTO have been used	Selex-SI CPW	AMS04_1111 - 12x200	HPA (S-band)	EMW	 AWR & ADS	- 4x125 LNA (Wideband)
TVR	Linear		Selex-SI CPW	SLX25_1112 - 2x100 (Switch Device)	SPDT (Wideband)	ELT	 AWR & ADS	- 4x125 LNA (Wideband)
TVR	Linear		Selex-SI CPW	SLX25_1112 - 2x200 (Switch Device)	SPDT (Wideband)	ELT	 AWR & ADS	- 2x125 LNA (Wideband)
TVR	Nonlinear	Nonlinear measurements from PTO have been used	Selex-SI MS	SLX18_2311 - 10x100	HPA (Wideband 2-6 GHz)	INDRA	 AWR	- 4x125 HPA (Wideband 6-18 GHz) SLX_UK
TVR	Linear	S-Par data from TVR, Pout vs Pin data from PTO	Selex-SI MS	SLX38_1112 - 3x50 (Parallel Switch Device)	SPDT (Wideband)	ELT	 AWR & ADS	- 10x200 HPA (S-band)
TVR	Linear	S-Par data from TVR, Pout vs Pin data from PTO	Selex-SI MS	SLX38_1112 - 3x100 (Parallel Switch Device)	SPDT (Wideband)	ELT	 AWR & ADS	- 8x75 (30 um Lgg) HPA (Wideband 6-18 GHz) SLX_UK
TVR	Linear		Selex-SI MS	SLX38_1112 - 5x100 (Parallel Switch Device)	SPDT (Wideband)	ELT	 AWR & ADS	- 8x75 (60 um Lgg) HPA (Wideband 6-18 GHz) SLX_UK
TVR	Linear		Selex-SI MS	SLX38_1112 - 4x50 (Serie Switch Device)	SPDT (Wideband)	ELT	 AWR & ADS	- 8x75 (SPDT Configuration) SPDT (X-band)
TVR	Linear	S-Par data from TVR, Pout vs Pin data from PTO	Selex-SI MS	SLX38_1112 - 4x100 (Serie Switch Device)	SPDT (Wideband)	ELT	 AWR & ADS	
TVR	Linear	S-Par data from TVR, Pout vs Pin data from PTO	Selex-SI MS	SLX38_1112 - 6x100 (Serie Switch Device)	SPDT (Wideband)	ELT	 AWR & ADS	
TVR	Noise	Linear data from TVR, non linear data from PTO	Selex-SI MS	SLX38_1112 - 4x75	LNA (Wideband)	ELT	 AWR & ADS	
TVR	Noise	Linear data from TVR, non linear data from PTO	Selex-SI MS	SLX38_1112 - 8x75	LNA (Wideband)	ELT	 AWR & ADS	
TVR	Noise		QinetiQ CPW	Endeavour - 2x75	LNA (X-band)	TNO	 ADS	
TVR	Noise		QinetiQ CPW	Endeavour - 2x125	LNA (Wideband)	SLX_UK	 ADS	
TVR	Noise		QinetiQ CPW	Endeavour - 4x125	LNA (Wideband)	SLX_UK	 ADS	