40 ns Pulsed I/V Set-up and Measurement Method applied to InP HBT characterization and Electro-thermal modeling

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***Abstract* — This paper presents a novel pulsed I/V measurement methodology applied to HBTs characterization using very narrow 40 ns pulse widths. The measurement procedure consists in applying pulsed collector emitter voltages while driving the transistor base with constant DC currents. The proposed measurement technique is applied here to the characterization and electro-thermal modeling of InGaAs/InP DHBTs from Alcatel Thales III-V Lab. By monitoring pulse widths from 400 ns down to 40 ns, non isothermal, quasi isothermal and isothermal behaviors of transistors are observed respectively. Measurements and simulations are then done to study electro-thermal effects in bipolar current mirrors.**

I. Introduction

InP DHBT technology is suitable to address very high-speed integrated circuits such as wide band samplers as well as clock recovery and decision circuits in optoelectronic applications [1]. One of the key building blocks of very fast bipolar circuits like Track and Hold or Sample and Hold circuits, is the differential pair in which base currents are switched between two transistors. Differential pair blocks have attractive feature to avoid the need for inter-stage coupling capacitors and to reject signal and spurious common to the inputs. In such circuits detrimental imbalance due to electro-thermal aspects have to be carefully examined. Mirror current source is another basic circuit which can also be affected by electro-thermal effects that can result in MMIC performance deviations. As a consequence, accurate HBT electro-thermal characterization and modeling is an important issue for successful high-speed integrated circuit simulation and design and for device reliability investigation [2], [3]. Another key feature justifying the important need for electro-thermal characterization and modeling is that a dense integration of transistors having high current densities is required to design high-speed circuits. Pulsed I/V measurements with minimum pulse widths in the order of a few hundred ns suitable for power transistors characterization and modeling, have been already reported in [4],[5]. This paper focuses on very narrow 40 ns pulsed I/V measurements. Transistors that have been characterized and modeled in this work are 40 μm^2 InGaAs /InP DHBTs from Alcatel Thales III-V Lab. An Electro-thermal model has been extracted from measurements and validated by comparing simulations and measurements of a pair of transistors mounted in a current mirror configuration. In part II of the paper, the set-up and measurement procedure are described. In part III, the electro-thermal HBT model is given. In part IV, measurements and simulations of a pair of transistors mounted in a current mirror configuration are shown for wide and narrow pulse operation. In part V, 1 – 65 Ghz S parameter measurements and simulations of a single transistor are reported for two different operating conditions corresponding respectively to cutoff region and saturated region. To conclude the application of this work to the study of a track and hold circuit for microwave signal sampling is mentioned.

II. Set-up and characterization method description

The pulsed I/V set-up presented in this paper is based on the use of a 4200 KEITHLEY semi-conductor characterization system. The proposed pulsed I/V measurement methodology consists in biasing the transistor base using a DC current source through a bias tee while pulsing the collector voltage with a 40 ns pulse generator. No bias tee is used at the collector port to reach a minimum 40 ns pulse width. The used pulse duty cycle is 10%. Pulsed voltage measurements are made alternately at the collector and the base port to achieve the best pulse shapes. For collector emitter voltage measurements, a 50 Ω scope channel is used. For base emitter voltage measurements, a 1 MΩ scope channel is used. Pulse operating conditions and measurement principle are sketched in figures 1 and 2. On wafer measurements of 40 μm^2 InP DHBTs from Alcatel Thales III-V Lab have been performed and are reported in his paper. The InP Double Heterojunction Bipolar Transistors (DHBT) structure used in this process includes a highly C-doped graded InGaAs base and a step-graded quaternary base-collector interface. Thickness optimization for base (<65nm) and collector (<250nm) enables to achieve a current gain of about 50 for 40 μm^2 transistors, while the Transition Frequency (F_T) and the Maximum Oscillation Frequency (F_{MAX}) are in the 170-250 GHz range for a current density of 2.2mA/μm^2 (220kA/cm^2). The fully self-aligned triple-mesa technology includes 50Ω/sq NiCr resistors, Metal Insulator Metal (MIM) capacitors and three Ti/Au metal levels for circuit interconnections. With such functional characteristics, such components are suitable for high-speed digital circuit operation.

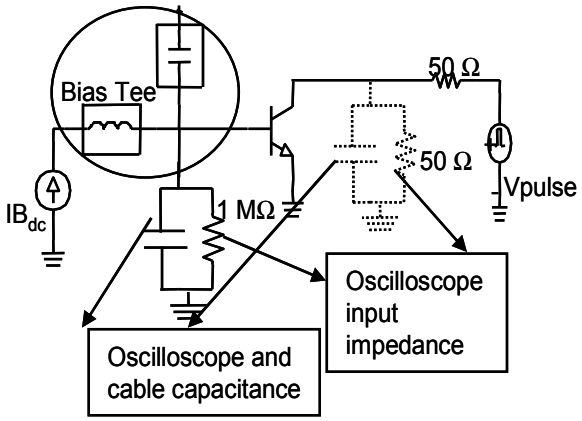


Figure 1: Pulse operating conditions

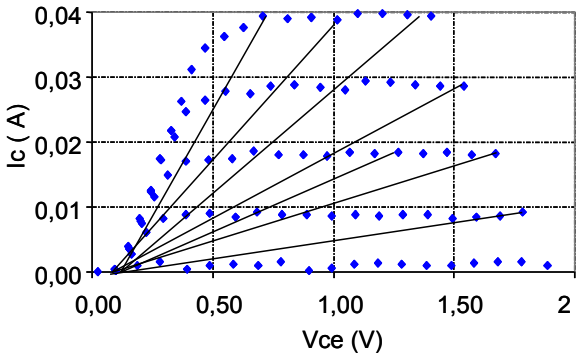
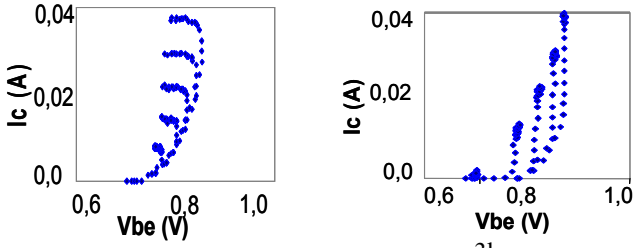


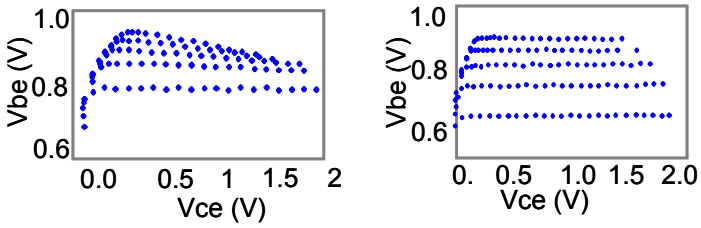
Figure 2: Illustration of the pulse measurement sequence

IV pulsed measurement results are given in figures 3 and 4 in the case of 400ns and 40 ns pulse widths. Collector current versus base emitter voltage measurements shown in figure 3 indicate that the proposed measurement method is very safe on devices. Base emitter voltage versus collector emitter voltage measurements shown in figure 4 highlight the presence of self-heating effects.



3a 3b

Figure 3: Collector current versus base emitter voltage at constant base current (3a: 400ns pulse width; 3b: 40 ns pulse width)



4a 4b

Figure 4: Base emitter voltage versus collector emitter voltage at constant base current (4a: 400ns pulse width; 4b: 40 ns pulse width)

III. Model Topology

The electro-thermal HBT model extracted in this work is based on a Π topology. Intrinsic equivalent model is shown in figure 5. Equations of the model have been reported in [6].

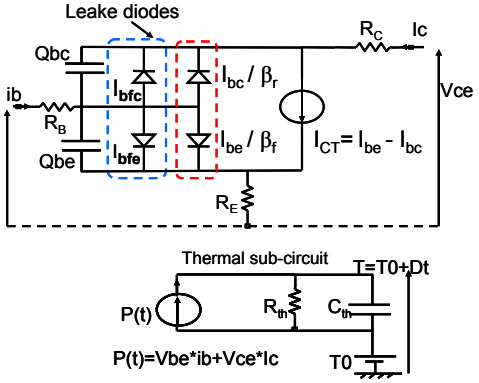


Figure 5: Model topology

In figures 6 and 7, simulation results are compared to measurements for 400ns and 40 ns pulse widths.

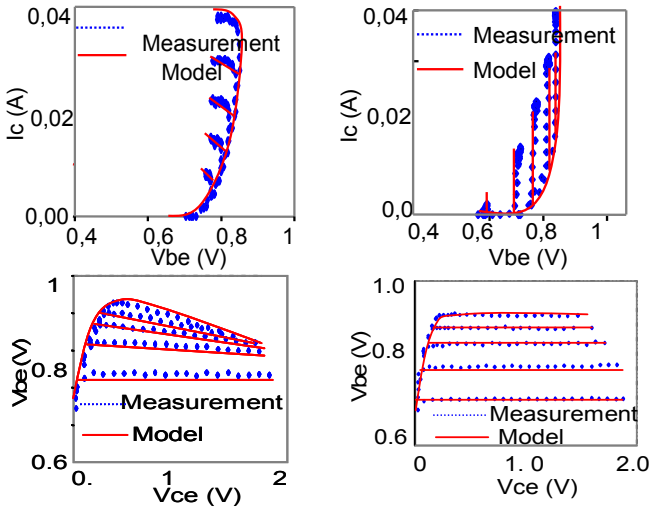


Figure 6: Ic and Vbe versus Vce characteristics:left column (400 ns pulse width),right column (40 ns pulse width)

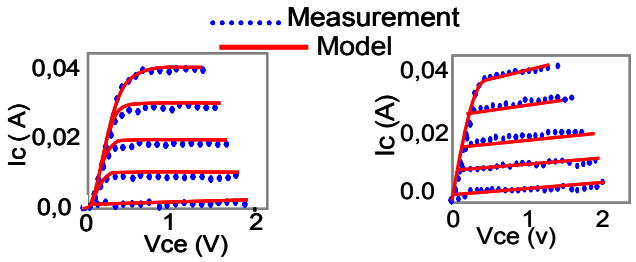


Figure 7: Ic versus Vce characteristics: left column(400 ns pulse width), right column (40 ns pulse width)

IV. Application to Current Mirror Source Measurement and Simulation

A pair of two identical 40 µm^2 InGaAs/InP DHBTs mounted in a current mirror configuration as illustrated in figure 8 has been measured. The input current Iin is applied with a DC source while the output voltage Vout is applied with a pulse generator. Measurement results for 400ns pulse widths are shown in figure 9. Measurement results for 40 ns pulse widths are shown in figure 10. In figure 9, we can observe that the output current Iout follows an exponential law versus Iin when Vout is higher than 1 volt. In figure 10 we can see that the current mirror does not exhibit current bifurcation when 40 ns pulses are applied. So we can conclude that the origin of such a phenomenon is due to transistors self-heating, notably because the two transistors do not operate at the same biasing conditions. In order to have an HBT electro-thermal model that enables predictions of such current bifurcation (thermal run-away of the output transistor), we found that emitter and collector extrinsic resistors have to be temperature dependant

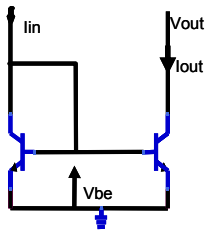


Figure 8 : current mirror configuration

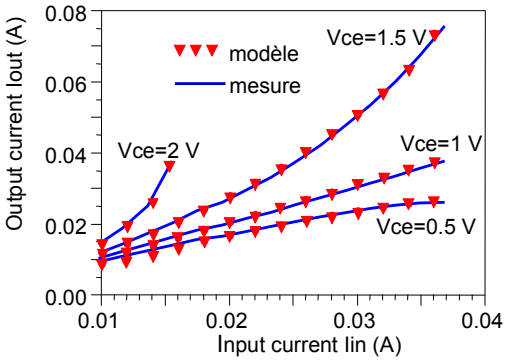


Figure 9 : current mirror characteristics: (400ns pulsed Vout)

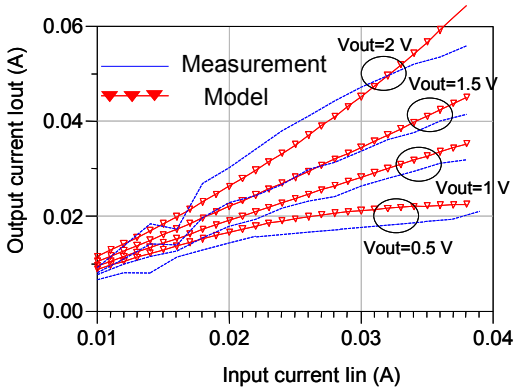


Figure 10 : current mirror characteristics: (40ns pulsed Vout)

The law adopted to provide a very good fit between simulations and measurements has the following form.

$$R = R_{T0} * \exp -(\frac{(T_j - T_0)}{\alpha}) \qquad (1)$$

T_0 is the ambient temperature. R_{T0} is the resistance at junction temperature T_j equal to T_0. α is a parameter which defines the sensitivity of the resistance with respect to the temperature. Different values of parameters R_{T0} and α are tuned for emitter resistance and for collector resistance modeling. It has to be noted here that under DC operation, the current mirror exhibits the same characteristics than it does in the case of 400 ns pulsed Vout. Figure 11 shows the temperature dependence of R_c and R_E (respectively collector and emitter resistances).

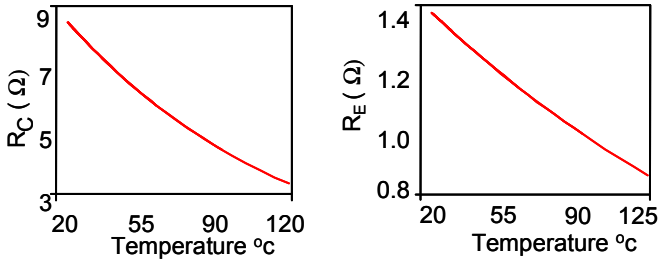


Figure11: Collector resistance and emitter resistance modeling.

V. S- PARAMETERS RESULTS

S parameters measurements of a single 40 µm² InGaAs/InP HBT have been performed over the 1 – 65 GHz frequency bandwidth. Comparisons between measurements and simulations are shown in figure 12a and 12b for two different bias points (Ic = 0 mA , Vce = 2V) and (Ic = 30 mA , Vce = 1V) , corresponding respectively to transistor cutoff region and saturated region . Here again , good agreements between measurements and simulations are obtained .

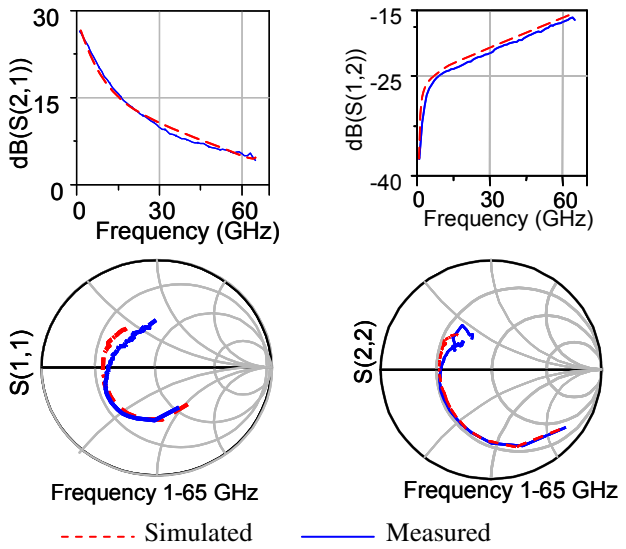


Figure 12a : simulated and measured S-parameters(Ic = 30 mA Vce = 1V)

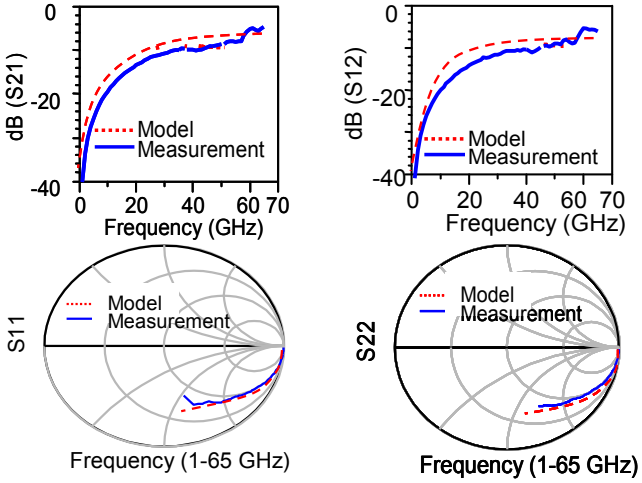


Figure 12b : Simulated and measured S-parameters (Ic = 0 mA Vce = 2V)

V. CONCLUSION

We have reported on a new and narrow pulsed IV measurement procedure that is here applied to InP HBTs electro-thermal modeling. A validation of this work has been demonstrated by characterizing a current mirror source configuration. Such a circuit is particularly well suited for transistor electro-thermal modeling validation. The characterization tool and measurement procedure presented in this paper reveal to be well suited to aid in designing high-speed integrated circuits. Work under progress now concerns investigations of the behavior of a track and hold circuits for high speed sampling of microwave signals. A building block that consists in a differential pair , a current mirror source , and a switched emitter follower transistor is being studied .Simulation results based on the use of HBT electro-thermal modeling work reported here will be given in the final version of this paper .

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