Study and Design of High Efficiency Switch Mode GaN Power Amplifiers at L-band Frequency

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***Abstract*— Activities have been carried out to determine the best electrical operating conditions of GaN HEMT that enable maximum power added efficiency at L-Band for Switch Mode Power Amplifiers (class F, inverse class F and class E). Satellite Radio navigation applications (Galileo) are targeted. Maximization of power added efficiency is of prime importance to save DC power consumption, reduce self heating effects and improve reliability of power amplifiers. At 50V drain bias, a maximum power added efficiency (PAE) of 72% and 40.3 dBm output power (Pout) are obtained using class-F operating conditions at 2dB gain compression while a 75% PAE and 41.0 dBm Pout are obtained using class E at 3dB gain compression.**

I. INTRODUCTION

THIS paper includes both theoretical analysis and large signal measurements of a 10 Watt GaN transistor from Eudyna Devices Inc. RF power efficiency is a key feature for high power amplifiers in satellite communications. Basically, the transistor used exhibits maximum power added efficiency performances, if the overlap between intrinsic voltage and current waveforms at the output is minimized [1]. At microwave (L-Band) the first three harmonics of the microwave useful signal can be reasonably controlled. Optimal combinations of sine wave, quasi square wave or rectified half wave current and voltage waveforms at the output of the transistor while the input voltage remains a sine wave lead to class-AB, class-F, inverse class-F and class E operating conditions.

For ideal Class-E operation, the transistor operates as an on/off switch and the load network shapes the voltage and current waveforms to prevent simultaneous high voltage/zero current and high current / zero voltage in the transistor. Such conditions minimize power dissipation, especially during switching transitions [2] [3].

Recent published works related to the design of Class-E power amplifiers, where Si-LDMOS transistors are used, reported a power added efficiency (PAE) of about 65% at 1.1 GHz [4].Due to higher current densities, carrier mobility and breakdown voltage GaN HEMT devices appears to be great candidates for high efficiency power amplifier designs and to target switching mode operation at microwaves frequencies.

Theoretical study and circuit simulation presented in this work are validated by calibrated time domain load pull measurements. The paper is organized as following.

Part II is dedicated to the description of theoretical optimum voltage and current waveforms for maximum PAE and switch mode operation.

In part III, Harmonic Balance Simulation results at 2 GHz using ADS package and a non linear model of a 10W GaN HEMT from Eudyna are given and discussed.

In part IV, time domain measurements are shown to validate the study.

Part V focuses on the circuit design of a L-Band Class-E amplifier using distributed matching components.

As a conclusion, future investigations are mentioned.

II. SWITCH MODE OPERATION

The single-ended Class E switched-mode power amplifier was introduced by Sokals in 1975 and has found widespread applications due to its design simplicity and high efficiency operation. In the simplest case, the load network can be represented by the shunt capacitance C_S and inductance L_S connected in series with the load R_{load}. The drain of the transistor is connected to the supply voltage by the choke inductance RFC with high reactance at the fundamental frequency as depicted in figure 1.

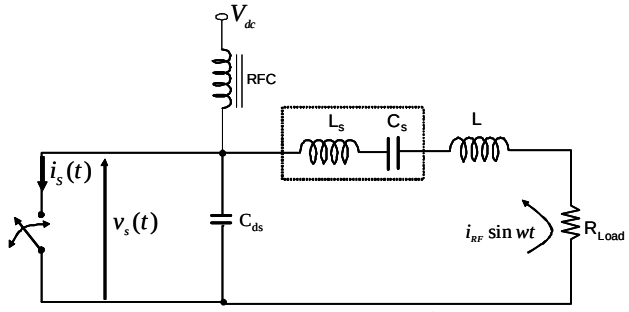

Fig. 1. Ideal switch mode power amplifier class E.

The load network of class-E amplifiers is a serie resonant network. The transistor is considered to be an ideal switch that is driven in such a way to provide the device switching

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between its on-state and off-state operation conditions [5]. For lossless operation mode, it is necessary to provide the following optimum conditions for voltage across the switch just prior to the start of switch on at the moment t = T_S, when transistor is saturated:

$$v_s(t)_{t=Ts} = 0 \text{ and } \left.\frac{dv_s(t)}{dt}\right|_{t=Ts} = 0$$

Where Ts is the period of input driving signal. In this case, the output power is equal to the power delivered by the power supply, the drain efficiency reached 100% and the ideal time domain waveforms are presented in figure 2.

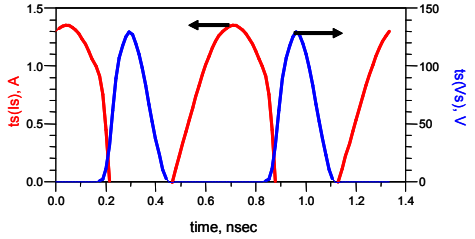


Fig. 2. Ideal class E drain current and voltage waveforms

The load network of class F and F^{-1} amplifiers is a parallel resonant circuit as illustrated in figure 3.

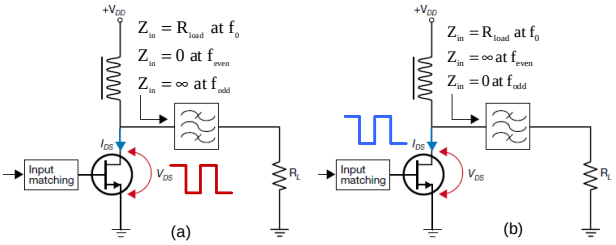


Fig. 3. Ideal class-F (a) and inverse class-F (b) circuit topology.

Figure 4 shows the ideal time-domain current and voltage waveforms of the class-F and inverse class-F amplifiers, when they have the same fundamental output power under the same drain biases. The class-F amplifiers have half-sinusoidal current and square-wave voltage signals.

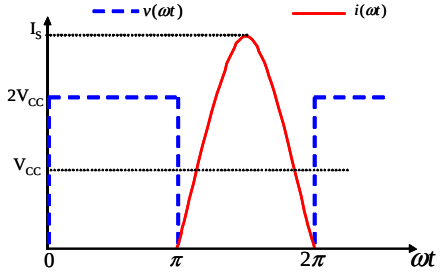


Fig. 4. Ideal class F drain current and voltage waveforms

The class-F amplifier, which has short load termination at even-order harmonics and open load termination at odd-order harmonics, has become a representative of the high-efficiency amplifier approach. Ideally 100% PAE can be reached [6].

The inverse class-F is dual of the class-F where the Id and Vd waveforms are interchanged figure 5.

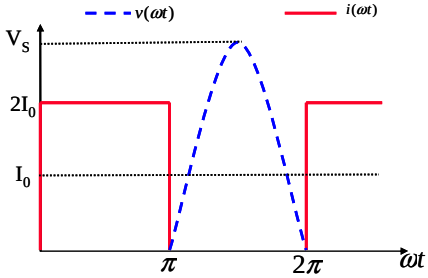


Fig. 5. Ideal inverse class F drain current and voltage waveforms.

III. NON LINEAR CIRCUIT SIMULATIONS.

The component used in this study is a transistor EGN010MK GaN HEMT (10W) from the foundry *Eudyna inc*. A non linear model has been extracted using pulsed I/V and pulsed S parameter measurements. Model topology is shown in figure 6.

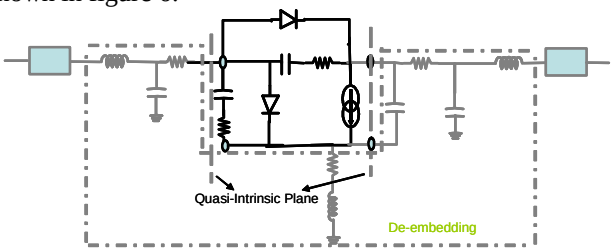


Fig. 6. Non linear model topology.

The unique combination of high-current and high f_T of a HEMT and also high breakdown afforded by the wide band-gap, enables the AlGaN/GaN HEMT on SiC in high-power switch-mode operation [6][7]. This ensures efficient and broadband operation in switching-mode. Moreover, high frequency switching mode operation requires transistors to handle the high current arising when discharging the capacitance over the low resistive drain-to-source channel. Wide band-gap HEMTs seem to be ideal components for this type of applications.

The following study was performed at the bias point Vgs0= Vp =- 1.15V and Vds0=50V. (Vp: knee voltage).

HB simulations using ADS package have been performed with harmonic control at the first three harmonics. The following simulation results focus on switch mode operating conditions (F, F^{-1} and E).

Simulated de-embedded time-domain waveforms of the intrinsic drain-source voltage Vds and intrinsic drain current Ids are represented in Figure 7.

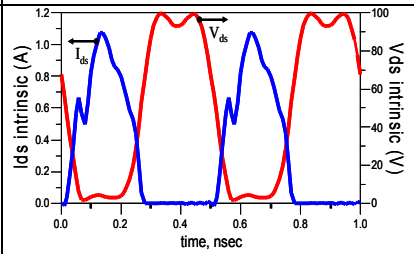
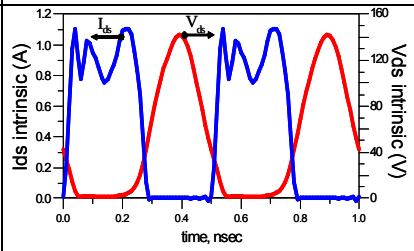
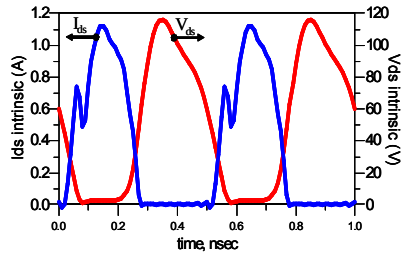
	Time domain waveforms	PAE	Comp. Gain
F		72%	2dB
F^{-1}		74%	5dB
E		75%	3dB

Fig. 7. Simulated intrinsic drain to source voltage (red) and intrinsic drain current (bleu) waveform.

Class-F operation provides a maximum efficiency of 72% at an output power of 40.3 dBm and a gain compression of 2 dB. In the configuration of inverse class F, we obtain a maximum PAE of 74.5% at an output power of 42.6 dBm and a gain compression of 5 dB. In class E configuration, we can obtain a maximum PAE of 75% at an output power of 41.1 dBm and a gain compression of 3 dB.

We can observe in figure 7, that class E offers a good compromise between output power, efficiency and gain compression ratio.

IV. TIME DOMAIN WAVEFORM MEASUREMENTS.

The study has been validated by time domain waveform measurements [10] using a multi-harmonic tuner (MPT from Focus Microwave) and a calibrated large signal network analyzer (LSNA). The block diagram of the set-up is given in figure 8.

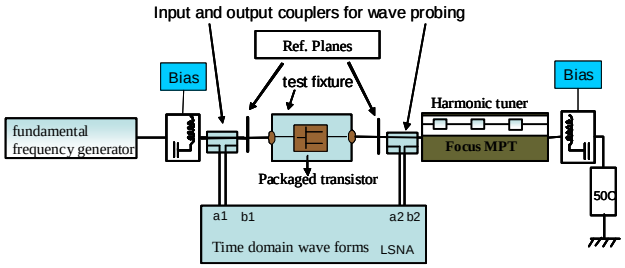


Fig. 8. Block diagram of calibrated time domain load pull bench.

The test bench is calibrated on a frequency grid from 2GHz to 10 GHz. Therefore 5 harmonics are taken into account for time domain waveform extractions. A relative SOLT calibration is performed. An absolute power calibration is achieved using a power meter and a phase calibration is done using an harmonic phase reference generator (HPR). [8]

Taking into account extrinsic elements of the non linear model extracted and shown in figure 6, measurements are de-embedded to get “quasi intrinsic” voltage and current waveforms at both gate and drain ports.

Output harmonic tuner is set to reach class E operating conditions. (Zload@F0 = 5.2 + j 17 Ω; Zload@2F0 = 15 + j72 Ω; Zload@3F0 = 140 + j 167Ω; at drain port of packaged transistor). Optimized load impedances and power performances have not been exactly reached because of coupler losses used for power wave probing and LSNA measurements.

Figures 9 and 10 show measurement results obtained.

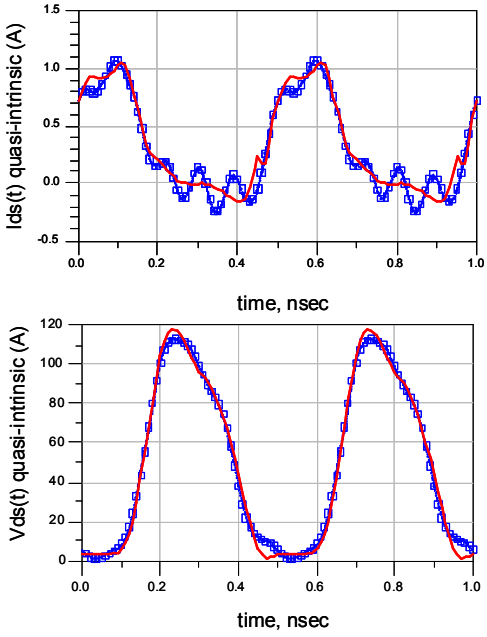


Fig. 9. Time domain waveform class-E operation measurements (blue square) and simulation (red line).

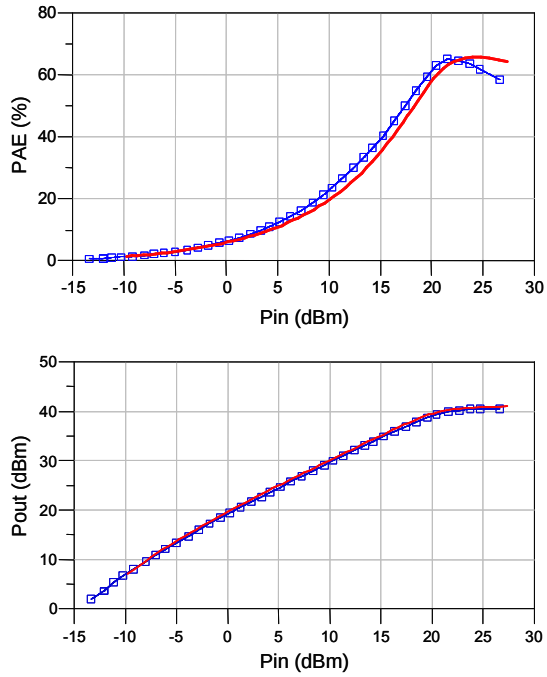


Fig. 10. Simulated (red line) and Measured (blue square) performances.

These measurement results validate the study. It demonstrates a perfect fit on time domain measurement for quasi-intrinsic voltage and current drain source waveform.

V. Design of Class E Amplifier

The schematic of the class-E power amplifier using distributed elements for harmonic impedance matching is given in figure 11.

Input circuit realizes 50Ω matching at the fundamental frequency. Output circuit topologies are now synthesized to achieve impedance transformation from 50 ohm load to the suitable optimum impedance ZL at the fundamental, second and third harmonic loads. The output matching network consists of three parts. First, an open circuited stub TL4 connected to the drain port by a tuned stripline TL5 provides a suitable third harmonic impedance (a high impedance required). Second, a short circuited stub TL2 connected to the drain port by a tuned strip line TL3 while the combination with TL5 provides a suitable second harmonic impedance (a high impedance is required too). This stub TL2 is near one quarter wavelength long at the fundamental frequency. Third, a tuned line TL1 provides a suitable load impedance tuning at the fundamental frequency.

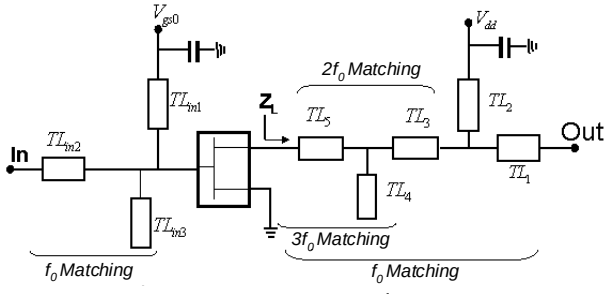


Fig. 11. Schematic diagram of the class-E power amplifier designed at 2 GHz.

The power-added efficiency of the transistor reaches 74%. The corresponding performances are the following: 41.0 dBm output power, 77% drain efficiency and 18.2 dB power gain. We obtain maximum simulated power added efficiency for class E amplifier at 3dB gain compression.

VI. Conclusion

An optimized GaN HEMT switch mode power amplifier has been studied in the 2 GHz frequency range. At 50V drain bias voltage, the Class E power amplifier demonstrates a best compromise between power-added efficiency and output power.

A further investigation concerns the optimisation of harmonic terminations at the input of the transistor.

References

[1] Andrei Grebennikov, Nathan O. Sokal *"Switchmode RF Power Amplifiers", Newnes, 2007.*

[2] N. O. Sokal and A. D. Sokal, "Class-E – A new class of high efficiency tuned single-ended switching power amplifiers", *IEEE Journal of Solid States Circuits, Vol. 10, No. 3, pp 168 –176, June 1975.*

[3] F. H. Raab, "Idealized Operation of the Class E Tuned Power Amplifier," *IEEE Trans. on Circuits and Systems, Vol. CAS-24, No. 12, pp. 725-735, Dec. 1977.*

[4] F. Wang and D.B. Rutledge, "A 60-W L-Band ClassE/Fodd,2 LDMOS Power Amplifier Using Compact Multilayered Baluns", *2004 IEEE Topical Workshop on Power Amplifiers for Wireless Communications.*

[5] Scott Sheppard and al., "High-Efficiency Amplifiers Using AlGaN/GaN HEMTs on SiC", *Cree Inc., 4600 Silicon Dr., Durham, NC 27703.*

[6] Young Yun Woo and al, "Analysis and Experiments for High-Efficiency Class-F and Inverse Class-F Power Amplifiers", *IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, VOL. 54, NO. 5, MAY 2006.*

[7] J. Benedikt, R. Gaddi, P. Tasker, and M. Goss, "High-power timedomain measurement system with active harmonic load-pull for highefficiency base-station amplifier design", *IEEE Transactions on Microwave Theory and Techniques, vol. 48, pp. 2617–2624, Dec. 2000.*

[8] J. Verspecht, "Calibration of a Measurement System for High Frequency Nonlinear Devices", *Doctoral Dissertation, Vrije Universiteit Brussel, November 1995.*

[9] J. Flucke and al, "Improved Design Methodology for a 2 GHz Class-E Hybrid Power Amplifier Using Packaged GaN-HEMTs", *Microwave integrated circuit conference 2007.*

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Outline

1. Introduction: Switch Mode Power Amplifier (SMPA).

2. Study and Simulation of high efficiency operating conditions.

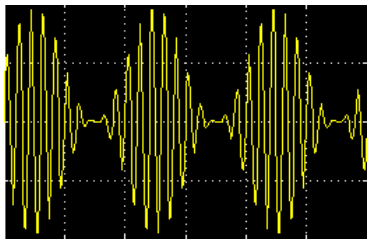
   - ✓ Output termination for high efficiency classes (F, F^{-1} et E).
   - ✓ Input termination and voltage shaping (Efficiency enhancement by conduction angle reduction).

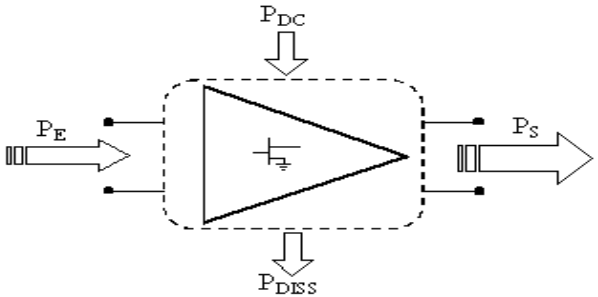
3. Time domain Load-pull measurement to validate the study.

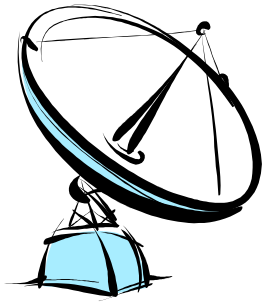
4. Conclusion.

1 Switch Mode Power Amplifier

Switch Mode Power Amplifier (SMPA)

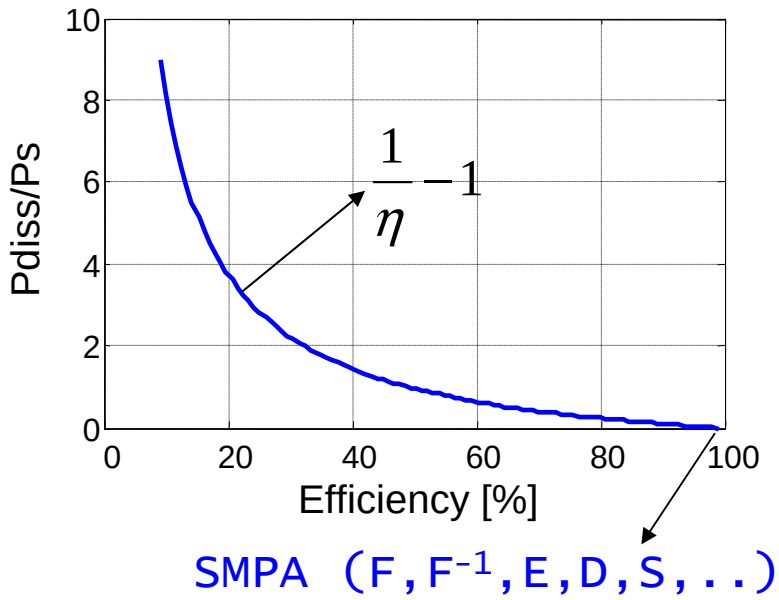






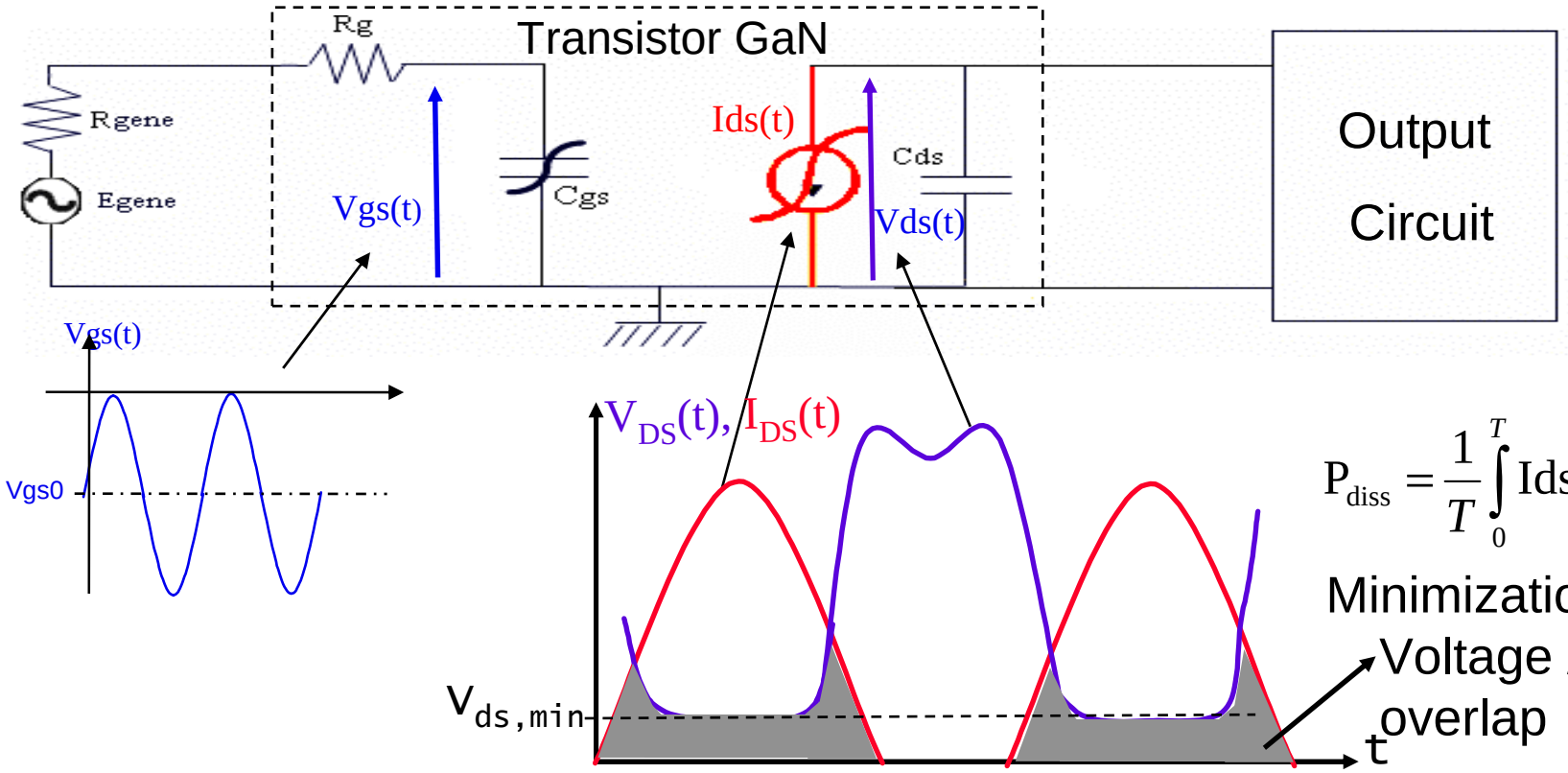
$$P_{in} + P_{DC} = P_{out} + P_{diss} \qquad P_{diss} = P_{DC}\left(1 - \frac{(P_{out} - P_{in})}{P_{DC}}\right) = P_{DC}(1 - PAE)$$

- **Why high efficiency amplifier is important?**
  - **Increased power consumption**
    - ✓ **Heavier power supplies**
    - ✓ **Battery cost**
    - ✓ **Electrical power expenses**
  - **Further multiplied by need for extra cooling**
  - **Deterioration of semiconductor reliability**



- **Solution : Switch Mode Power Amplifier**

Switch Mode Power Amplifier (SMPA)



$$P_{diss} = \frac{1}{T}\int_0^T Ids(t).Vds(t)\,dt$$

Minimization of the Voltage / Current overlap

➢ **Minimization of RF losses across the switch requires:**

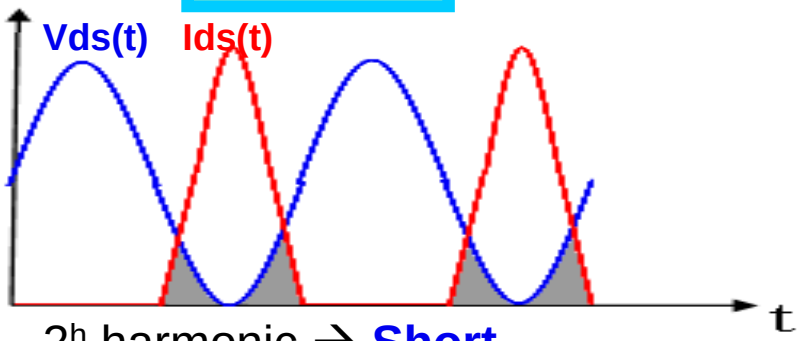
- ✓ In ON state **$V_{ds,min} = 0$** (Zero voltage switching condition (ZVS)) => **Low $R_{ds,on}$**
- ✓ In transition state: maximum slopes **dV_{ds}/dt and dI_{ds}/dt**
  => **Low value of Capacitances (Cgs et Cds).**

Advantage of GaN HEMT

Switch Mode Power Amplifier (SMPA)

Ideal harmonic load configurations for high efficiency operation → Control of the first 3 harmonics

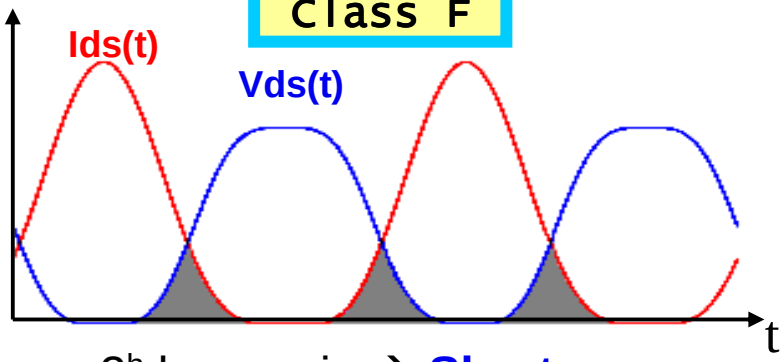
Class AB



2^h harmonic → **Short**

3^h harmonic → **Open**

Class F

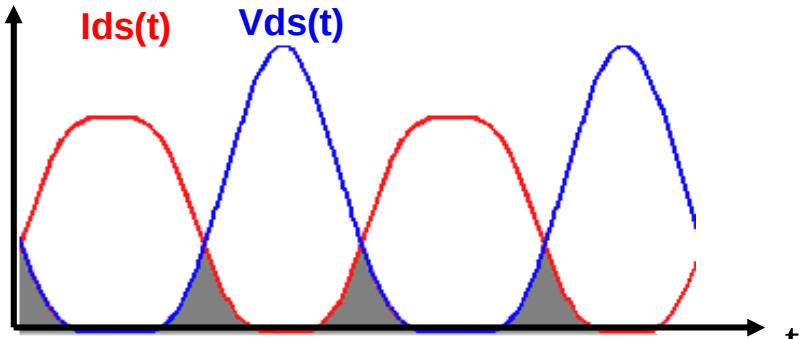


2^h harmonic → **Short**

3^h harmonic → **Open**

Load

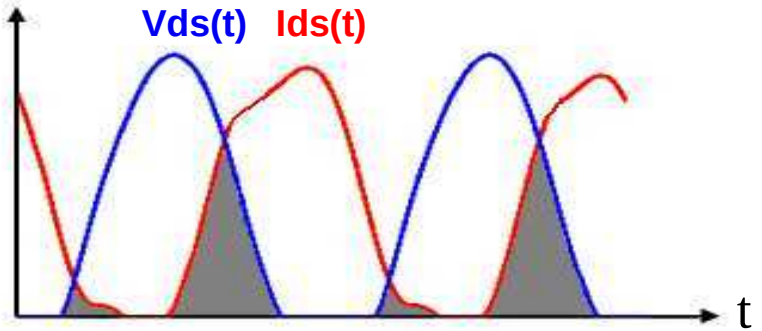
inverse Class F



2^h harmonic → **Open**

3^h harmonic → **Short**

Class E



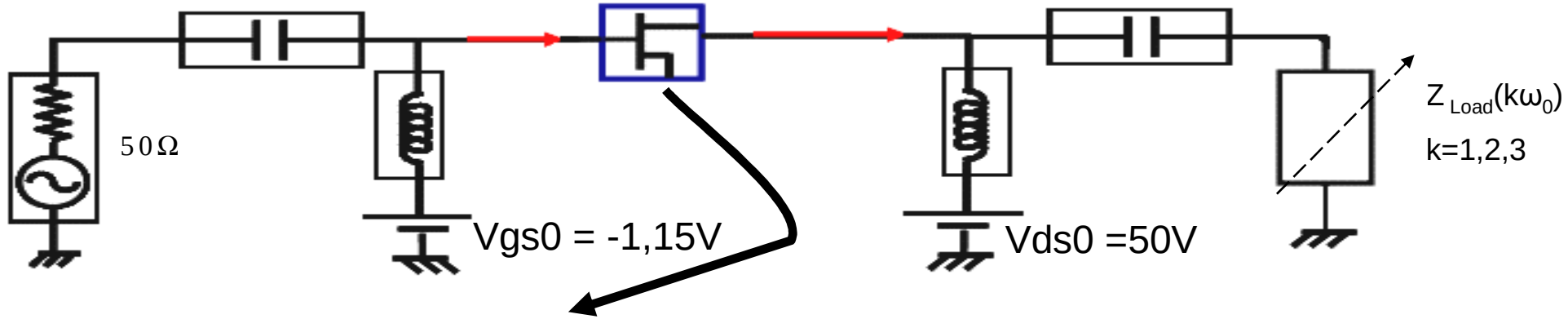
2^h harmonic → **Open**

3^h harmonic → **Open**

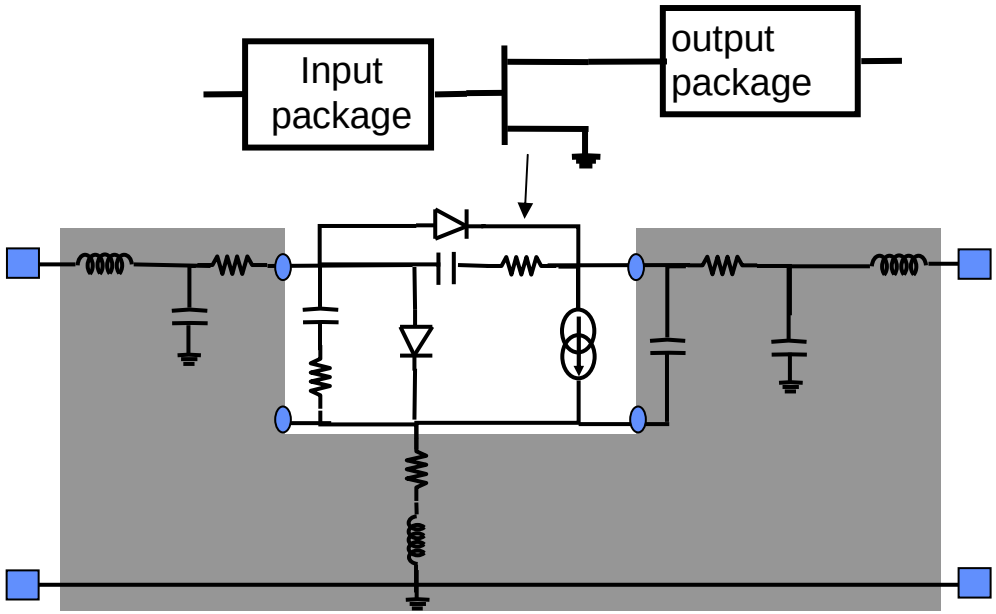
2 Study and Simulation of high efficiency operating classes

2.1- Simulation methodology

⇨ **Source and Load impedance tuning at the first 3 harmonics.**



Non linear model of transistor



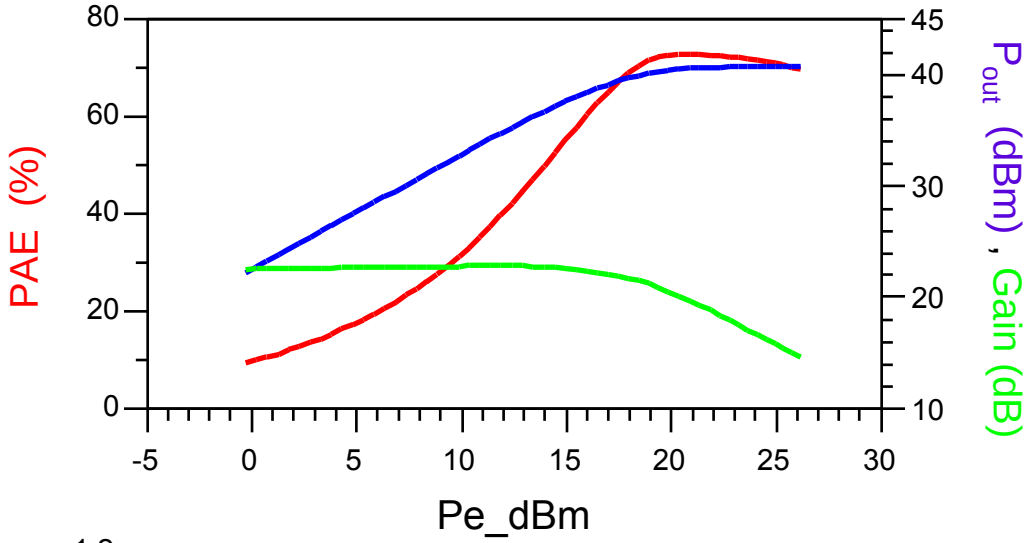
Optimisation Criteria :

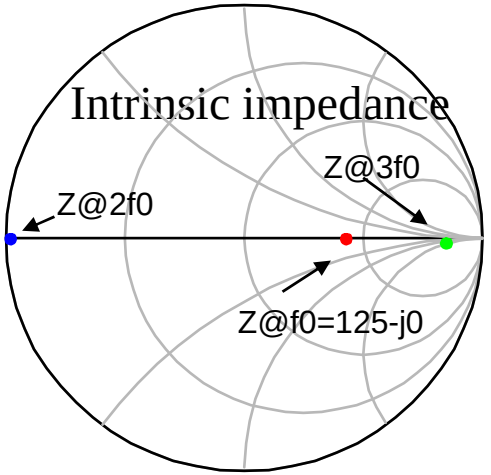
- ✓ Intrinsic drain source voltage and current waveforms
- ✓ Gate source voltage shape
- ✓ Dynamic Load Line

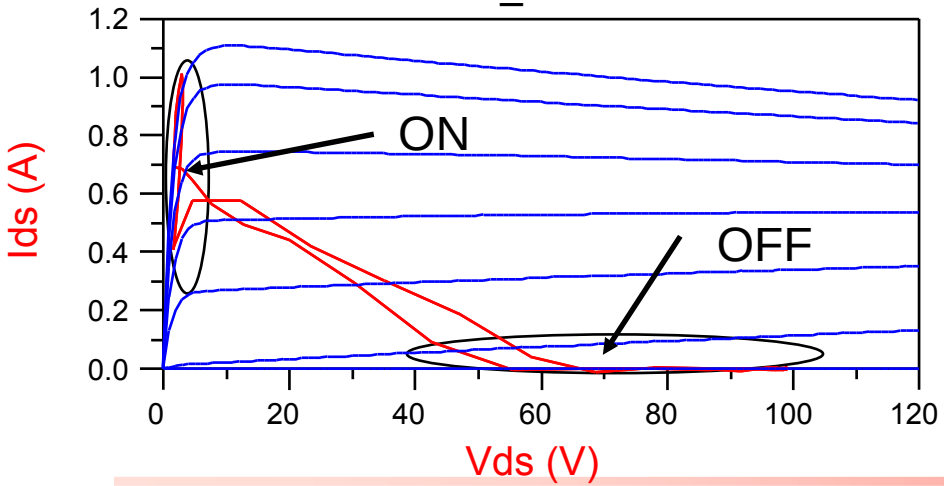
2.2- Simulation result – GAN HEMT Eudyna 10W @2GHz.

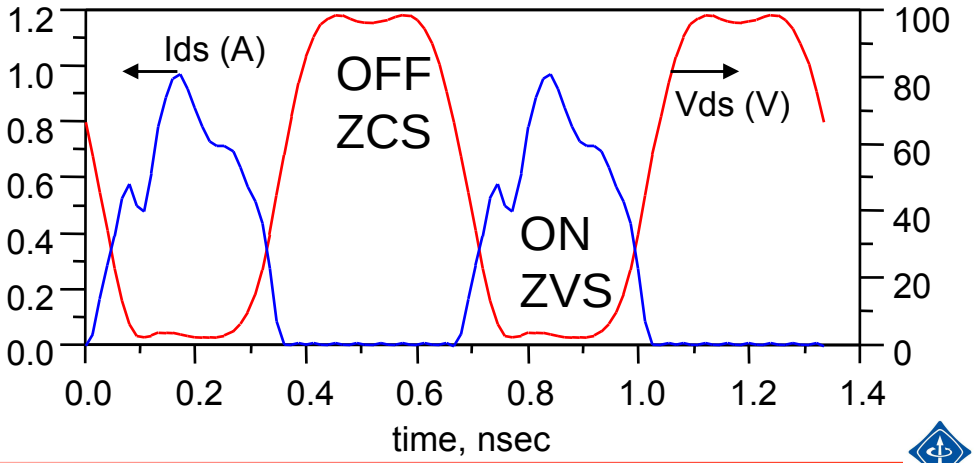
Class F @ Vds0=50V

PAE	Ps	Compression Gain
70%	40.0 dBm	@1dB
72%	40.3 dBm	@2dB





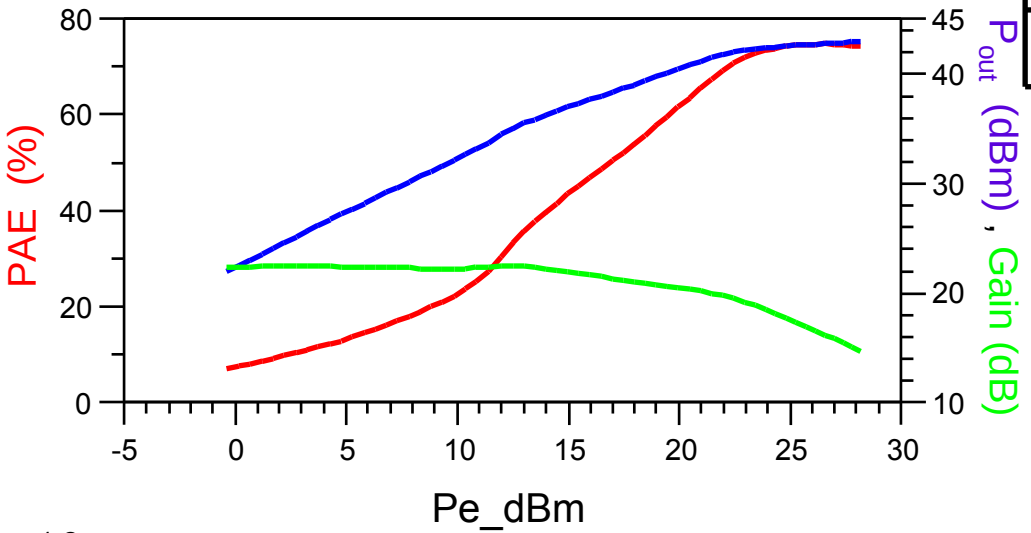


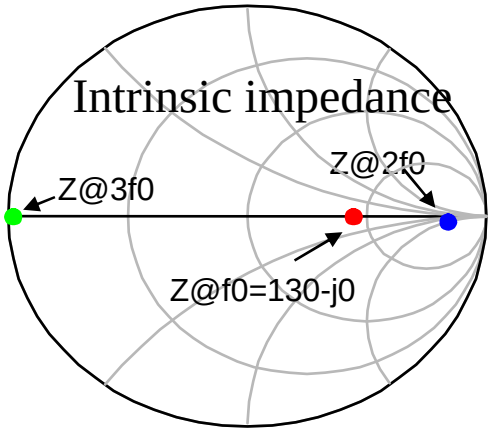


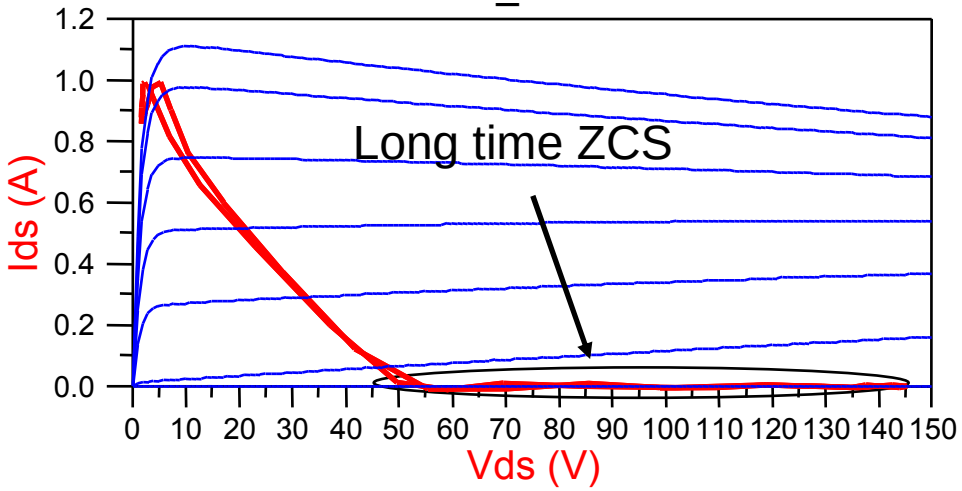
2.2- Simulation result – GAN HEMT Eudyna 10W @2GHz.

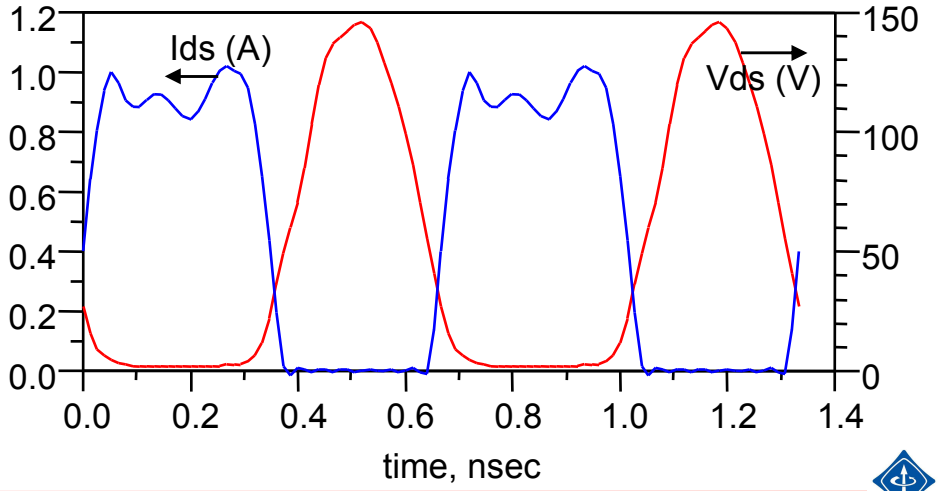
Inverse class F @ Vds0=50V

PAE	Pout	Compression Gain
54%	38.9 dBm	@1dB
74.5%	42.6 dBm	@5dB





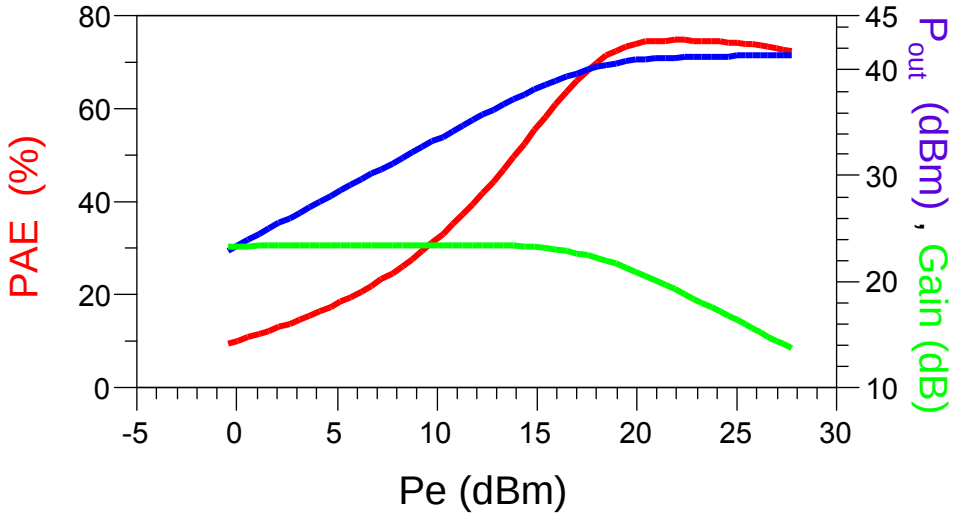


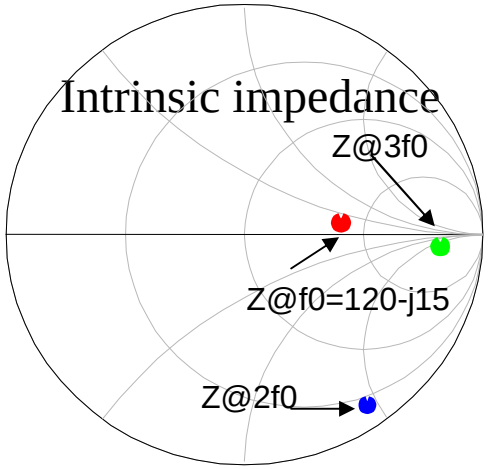


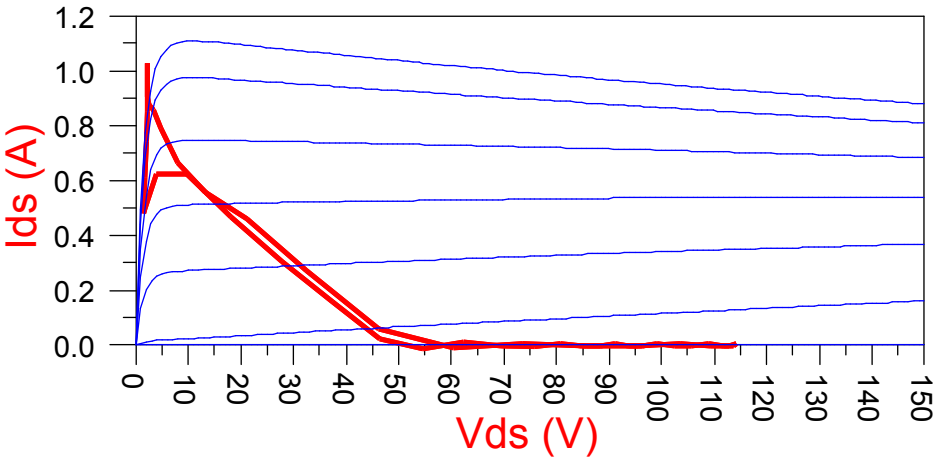
2.2- Simulation result – GAN HEMT Eudyna 10W @2GHz.

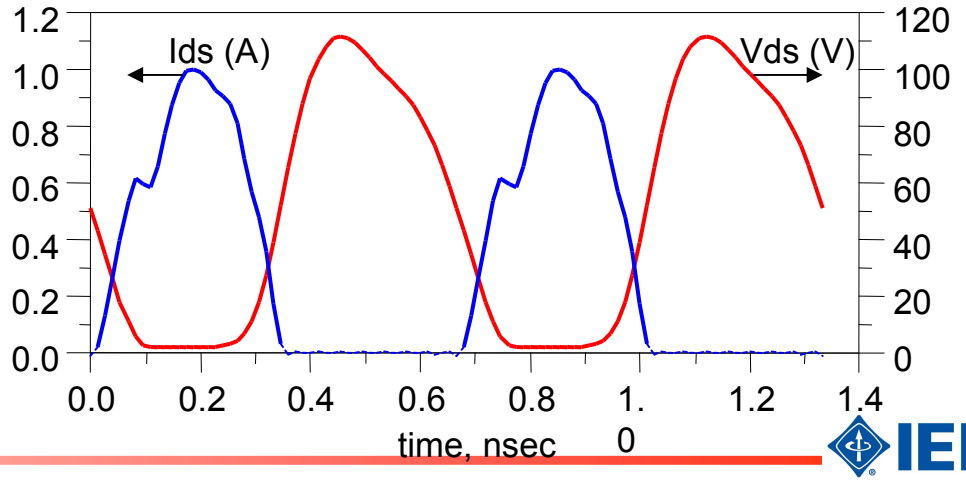
Class E @ Vds0=50V

PAE	Pout	Compression Gain
69.0%	40.0dBm	@1dB
75%	41.0 dBm	@3dB









2.2- Simulation result – GAN HEMT Eudyna 10W @2GHz.

Advantages and disadvantages of high efficiency Classes

Class F:

- **High efficiency is obtained at low gain compression**
- **maximum drain source voltage swing: 2Vds0 (Low power output compared of F^{-1} and E)**

Inverse Class F:

- **Maximum drain source voltage swing: 3Vds0 (high output power)**
- **High efficiency are obtained at 5dB of compression gain**

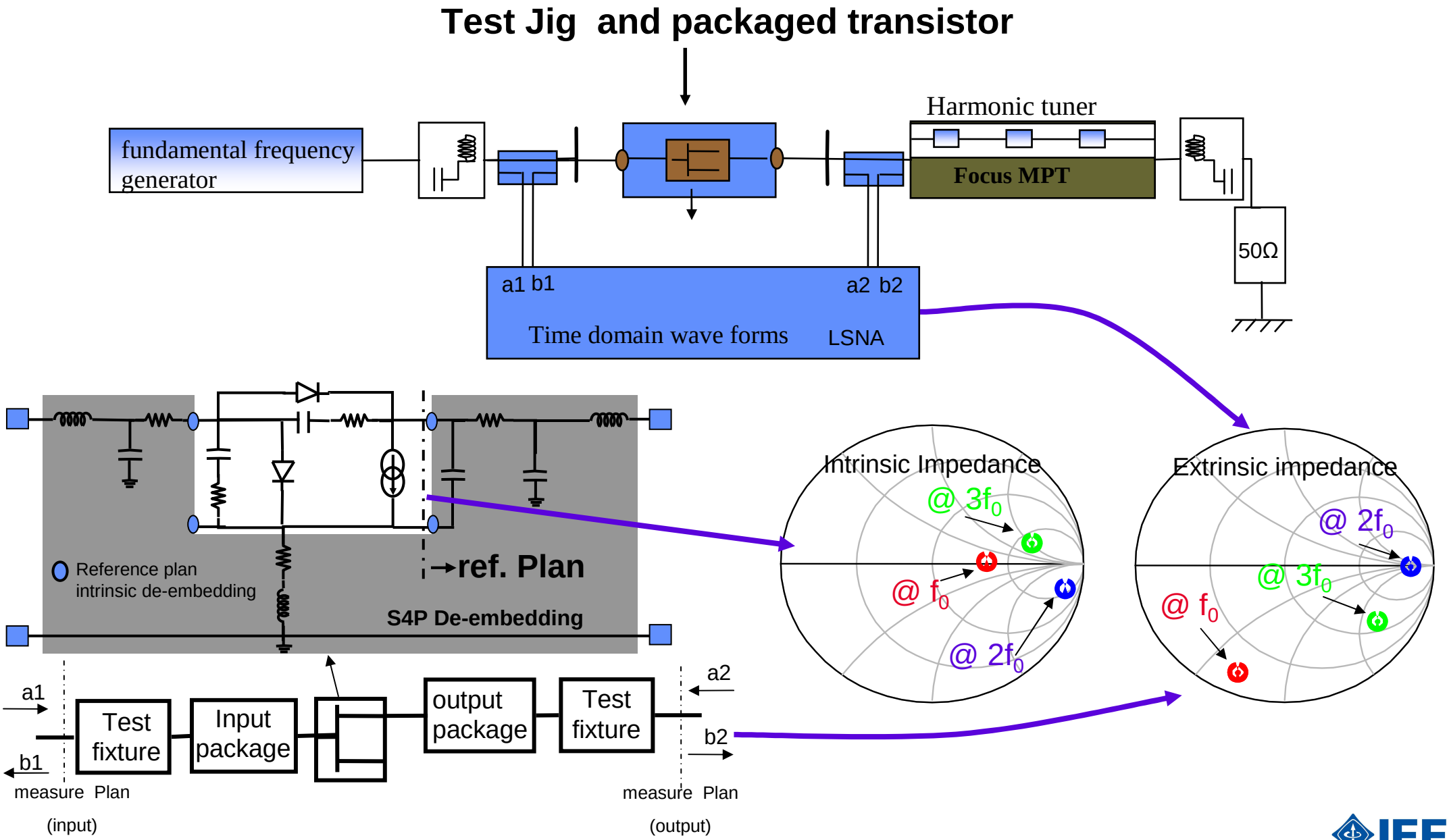
Class E:

- **The class E offers a good compromise trade of output power, efficiency and gain compression.**

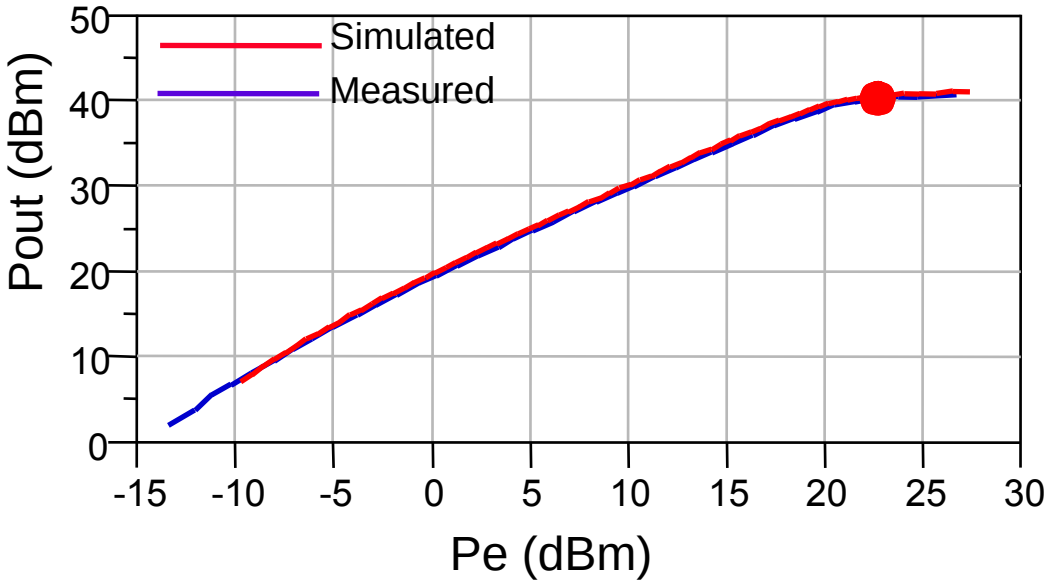
In any case the main critical point stands in the low pass behavior of the gate access

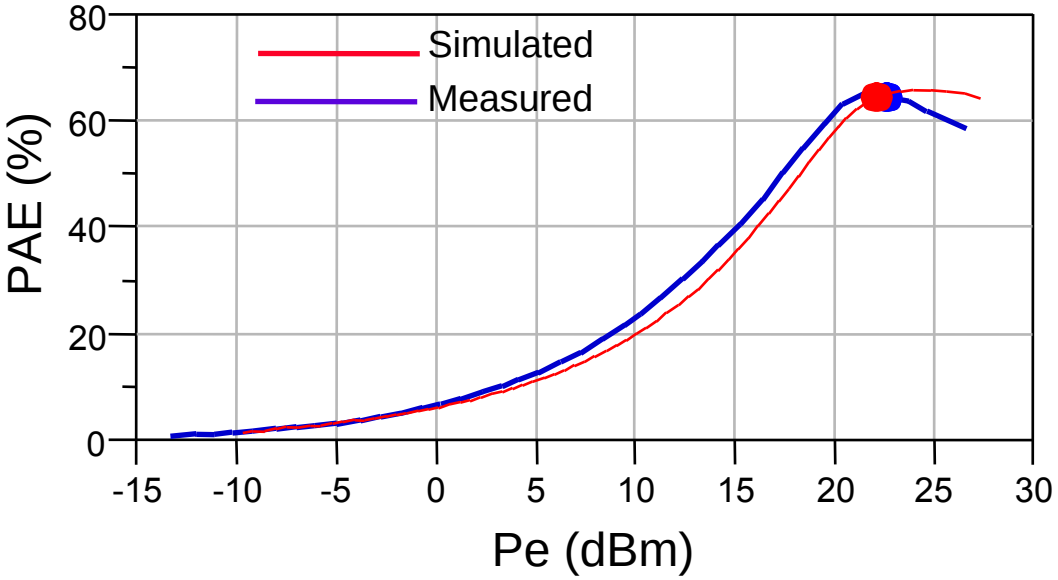
3 Time domain Load-pull measurement and Circuit design

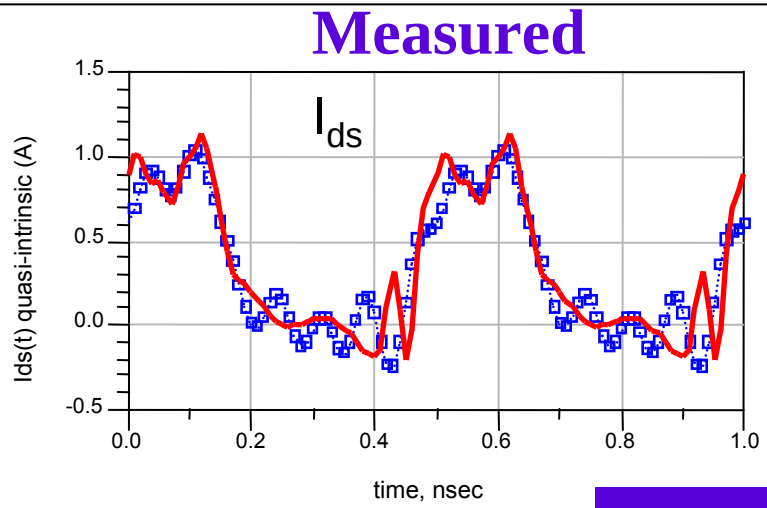
4.1- Time domain Load-pull measurement of GaN HEMT Eudyna 10W

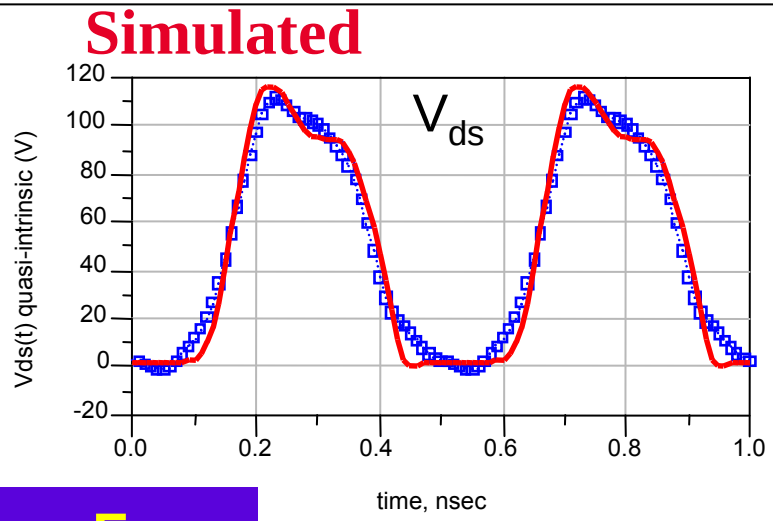


4.1- Time domain Load-pull measurement of GaN HEMT Eudyna 10W



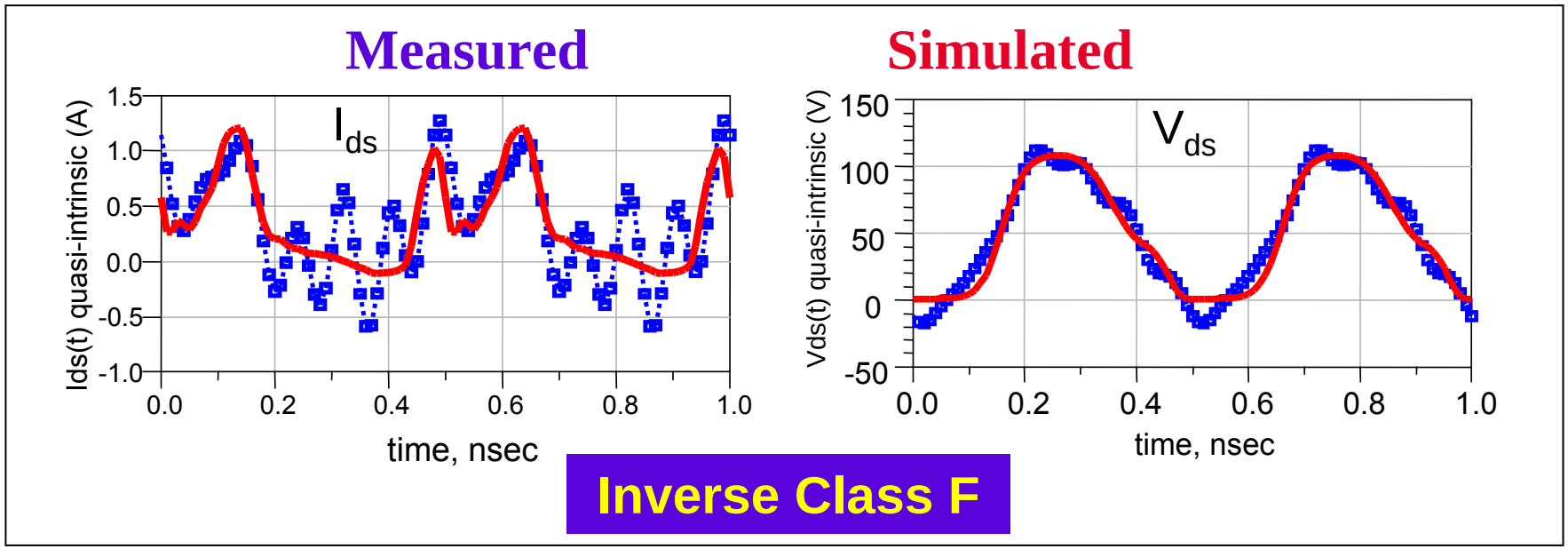


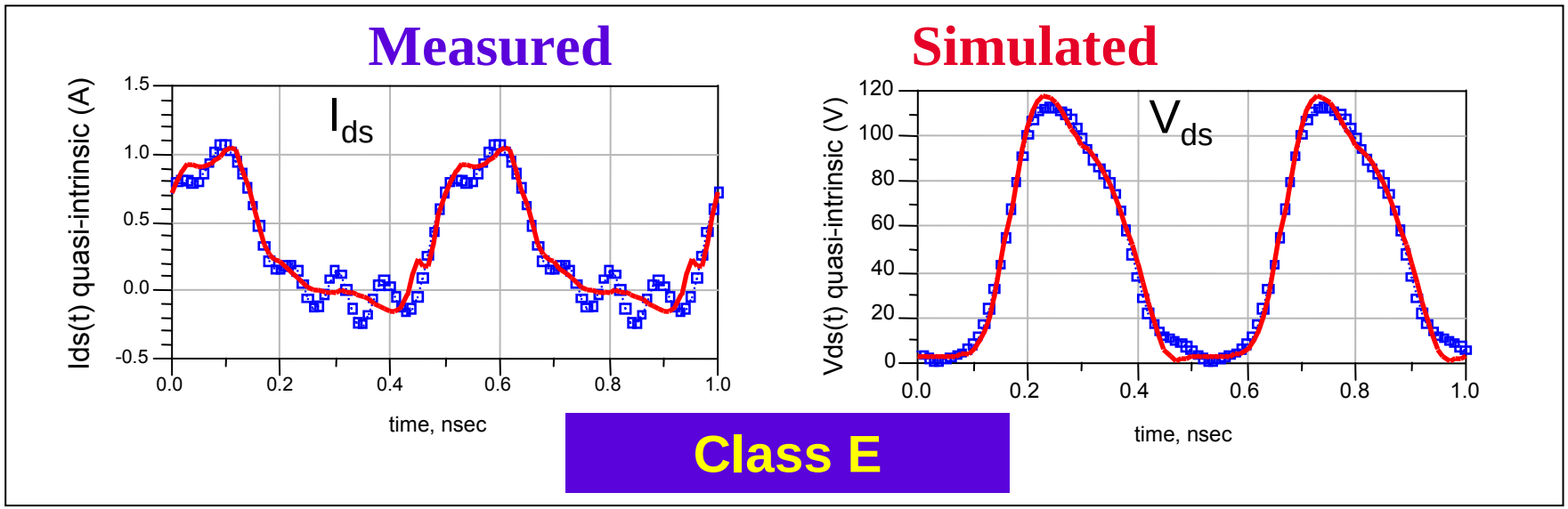




Classe F

4.1- Time domain Load-pull measurement of GaN HEMT Eudyna 10W





4 Conclusion

Conclusion

- The results of this study promotes class E operation for high power GaN amplifiers at L Band
- The class E offers a trade-off between output power, efficiency and gain compression.

A main and original aspect of this work lies in measured time domain waveforms that validate transistor modeling and simulations results

Future work concerns now gate source voltage shaping to improved Zero current switching conditions and PAE performances .

For that purpose the design of a driver amplifier is necessary

Thank you for your attention

Question ?

4.2 – Circuit design under development