Efficiency enhancement of GaN power HEMTs by controlling gate-source voltage waveform shape

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***Abstract*— This paper presents a technique to improve the power added efficiency (PAE) of GaN power amplifiers by an appropriate shaping of the gate source voltage waveform. The proposed technique is based on second harmonic injection at the transistor input. It is applied here to a 15W GaN HEMT die from Cree that has been characterized using an harmonic load pull test bench at L-band.**

The work reported here focuses on experimental gate-source voltage waveform shaping and its impact on PAE performances.

An original aspect concerns calibrated time domain waveform measurements and shaping that are performed and investigated simultaneously at both input and output ports of the transistor under test close to intrinsic accesses.

Measurement results performed at 2GHz validate optimized operating conditions derived from theoretical analysis and circuit simulations. For a fixed input bias voltage (close to pinch off voltage in our case), significant efficiency improvements are obtained when the positive half wave of the gate-source voltage is sharpened. Best and worst cases are examined respectively and show 25 point PAE difference at saturated power.

I. INTRODUCTION

AlGaN/GaN HEMT technology has a strong potential for high efficiency, high power microwave amplification because of high current densities, high breakdown voltage and capability to handle high temperature.

Furthermore, possible high output voltage operation presents a great advantage for low loss output impedance matching that is crucial to reach large output saturated power and consequently high power added efficiency. High power added efficiency is one of the prime specifications to meet in power amplifier designs.

High efficiency class F, F^{-1}, single ended GaN amplifiers have been reported during the past few years [1], [2], [3], [4].

CMCD GaN push-pull based topologies have been also demonstrated [5]. In these referenced works, suitable harmonic terminations at transistor's drain have been intensively studied and designed in order to minimize voltage and current overlap resulting in minimized dissipated power and maximum PAE.

This paper focuses specifically on gate source voltage waveform shaping which is an additional key point to reach the highest possible efficiency performances. This particular aspect has already been pointed out in [6] and [7] for GaAs PHEMT technology. In this work, the effect of gate-source voltage shaping on PAE performances is studied for a GaN HEMT device.

Theoretical study and circuit simulations are validated by calibrated time domain load pull measurements. The paper is organized as following.

Part II is dedicated to the description of theoretical optimum voltage and current waveforms for maximum PAE.

In part III, Harmonic Balance Simulations results at 2 GHz using ADS package and a non linear model of a 15W GaN HEMT from CREE are given and discussed.

In part IV, on wafer time domain measurements are shown to validate the study. Active second harmonic injection at the gate port represents here an original aspect of the presented test bench and experimental results.

As a conclusion, future investigations are mentioned.

II. THEORETICAL ANALYSIS OF INPUT/OUTPUT IDEAL WAVEFORM SHAPING.

To reach high efficiency performances of microwave power transistors, it is necessary to control load impedances at several harmonics, in order to minimize output intrinsic voltage and current waveform overlap.

At microwave frequencies, the first three harmonic terminations can be reasonably controlled.

Ideal drain-source voltage and drain current time domain waveforms for class F and inverse class F power amplifier are shown in figure 1. The grey area that highlights waveform overlapping must be reduced as much as possible to maximize efficiency.

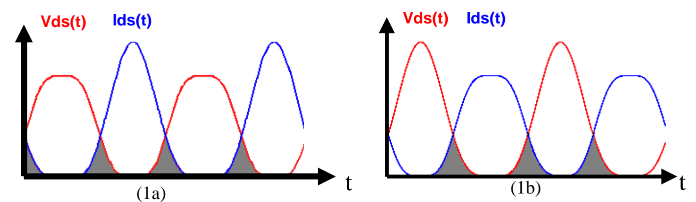

Fig. 1 Ideal output voltage and current waveforms: class F (a) and F^{-1} (b).

These representative voltage and current waveforms are given here for an input biasing voltage near pinch off voltage.

For high efficiency conditions, the device is driven at significant gain compression. Gate source and gate drain

capacitances are non linear and generate harmonic currents flowing into the source network. Harmonic 2 plays a major role and must be properly controlled by the source network. Otherwise the intrinsic gate source voltage can be distorted, the worst case being an “inverse” half sine wave shape that results in a significant increase of the DC drain current and a decrease of PAE performances. This worst case condition leads to an increase of the ON time “t_{ON}” and consequently a wider “aperture angle” of the transistor.

On the contrary, if an appropriate control of the input gate source voltage shape is achieved to reach an half sine wave shape, the on time t_{ON} and the aperture angle are reduced. It results in a reduction of the DC drain current along with a minimization of the drain voltage and drain current overlapping. Best and worst case conditions are sketched in figure 2 for class F operation mode.

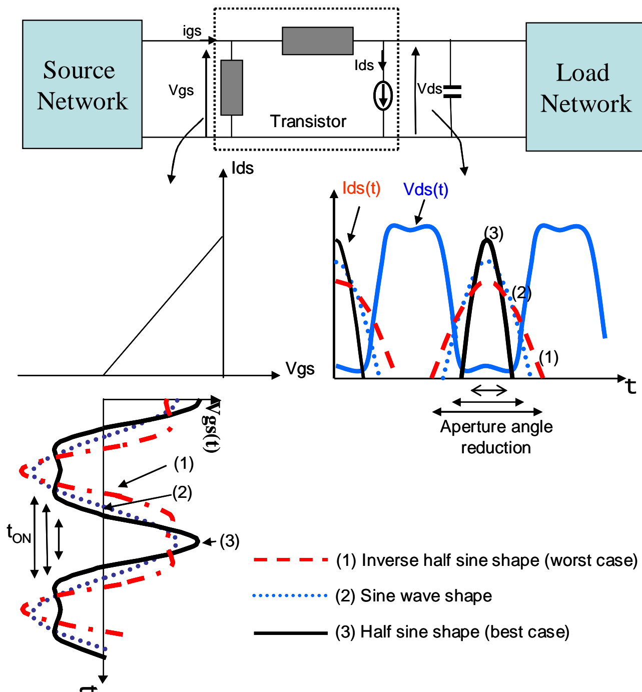

Fig. 2 Illustration of the effect of the input voltage shape on the aperture angle.

The theoretical half sine wave gate source voltage derived from analytical Fourier series expansion limited to two harmonics is:

$$Vgs(t) = V_{gs0} + V_{gs1} * \cos(wt) + V_{gs2} * \cos(2 * wt + \phi)$$

Optimum waveform shaping is obtained for $Vgs_2 = Vgs_1/7$ and $\varphi=0$ as illustrated in figure 3.

The following of the paper focuses on this optimal operating conditions that can be experimentally achieved by second harmonic injection at the gate port.

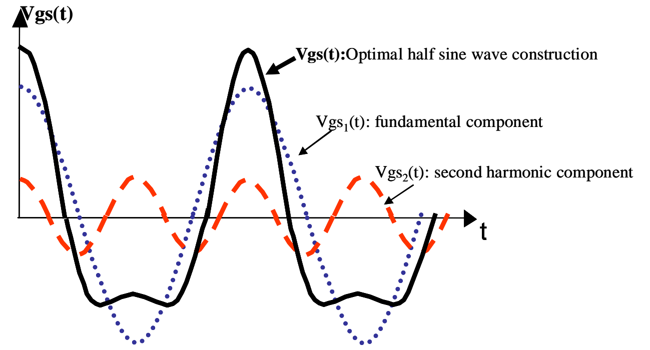

Fig. 3 Optimal half sine wave construction with H1 and H2.

III. Simulation Results.

A non linear model of a 15 W GAN HEMT die from CREE has been extracted using pulsed I/V and pulsed S parameter measurements. Model topology is shown in figure 4. HB balance simulations using ADS package have been performed with harmonic control at the first three harmonics. The following simulation results focus on class F operating conditions.

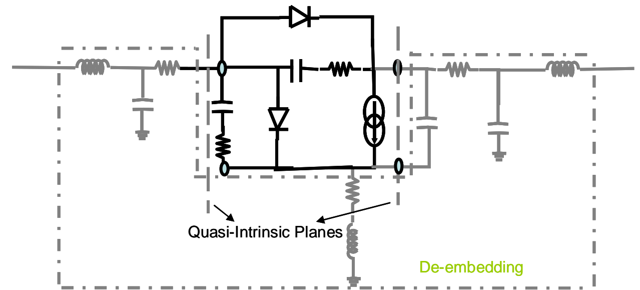

Fig. 4 Non linear model topology.

Simulated input-output intrinsic time domain waveforms are plotted in figure 5. Three different cases are represented:

1: Optimal second harmonic injection at the input
2: Input second harmonic terminated into 50Ω.
3: Input second harmonic terminated into a short.

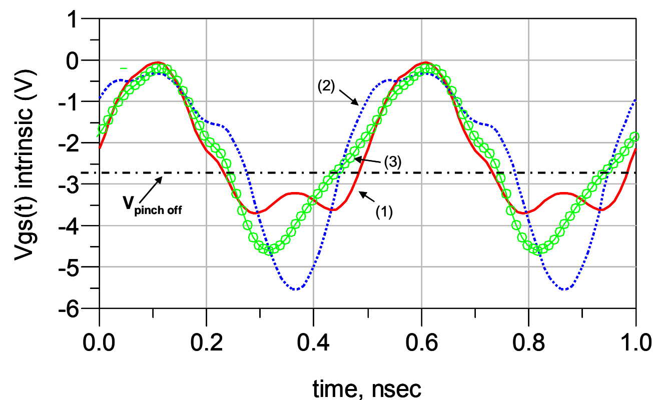

Fig. 5a Simulated intrinsic gate-source waveforms @ 38.5 dBm output power.
1. Optimal second harmonic injection at the input.
2. Input second harmonic terminated into 50Ω.
3. Input second harmonic terminated into a short.

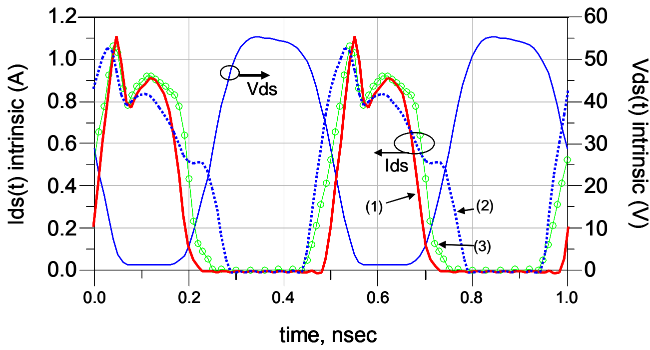

Fig. 5b Simulated output intrinsic voltage/current waveforms @ 38.5 dBm output power.

1. Optimal second harmonic injection at the input.
2. Input second harmonic terminated into 50Ω.
3. Input second harmonic terminated into a short.

We can observe in figure 6 that we obtain maximum simulated power added efficiency for an optimized half sine gate-source voltage waveform obtained by active injection of the second harmonic at the gate port. PAE of 75% is obtained @38.5dBm output power. Simulations were performed to obtain a maximum efficiency (Class F PAE optimization).Input power drive has been limited so that no significant direct gate source diode conduction takes place. This constraint is an important feature for reliability aspects to target satellite applications.

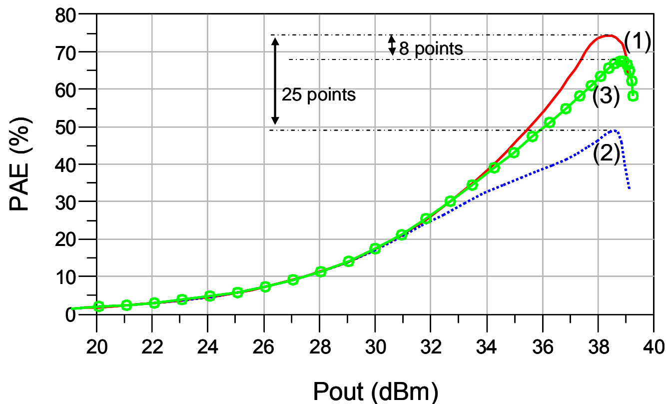

Fig. 6 Simulated power added efficiency vs. output power @2GHz.

1. Optimal second harmonic injection at the input.
2. Input second harmonic terminated into 50Ω.
3. Input second harmonic terminated into a short.

IV. TIME DOMAIN WAVEFORM MEASUREMENTS.

The study has been validated by on wafer time domain load-pull waveform measurements [8] using a multi-harmonic tuner (MPT from Focus Microwave) and a calibrated large signal network analyzer (LSNA). The block diagram of the set-up is given in figure 7.

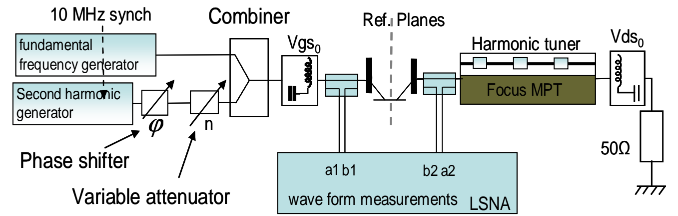

Fig. 7 Block diagram of calibrated time domain load pull bench.

The test bench is calibrated on a frequency grid from 2GHz to 10 GHz. Therefore 5 harmonics are taken into account for time domain waveform extractions. A relative SOLT calibration is performed. An absolute power calibration is achieved using a power meter and a phase calibration is done using an harmonic phase reference generator (HPR). [9]

Error corrected absolute power waves are measured at the tips of the bonding (reference planes indicated in figure 8) thanks to an associated calibration kit [10].

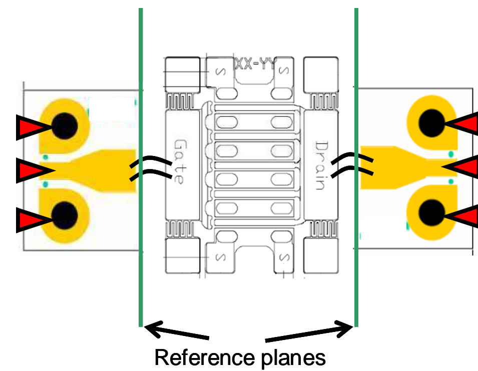

Fig. 8 Photograph of the GaN die with bonding and coplanar accesses.

Taking into account extrinsic element of the non linear model extracted and shown in figure 4, measurements are de-embedded to get “quasi intrinsic” voltage and current waveforms at both gate and drain ports.

Output harmonic tuner is set to reach class F operating conditions. (Zload@F0 = 29 + j32 Ω; Zload@2F0 = 5 - j2 Ω; Zload@3F0 = 8 + j23 Ω; at probe tips). Optimized load impedances and power performances have not been exactly reached because output coupler losses used for power wave probing and LSNA measurements.

Nevertheless the focus here is to validate significant effects on PAE performances due to gate source voltage shaping. When the input source at 2F0 is turned off, source impedance conditions correspond approximately to 50Ω at all harmonics.

When the input source at 2F0 is turned on, second harmonic signal injection is tuned by using a phase shifter and an attenuator. Optimal half wave “quasi-intrinsic” gate source voltage waveform can be experimented.

Figures 9, 10 and 11 show measurement results obtained.

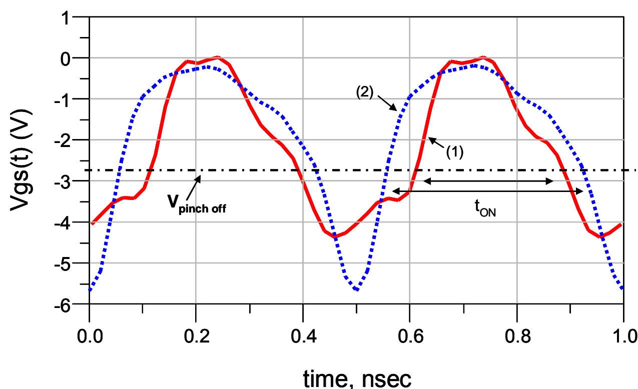

Fig. 9 Measured gate source voltage deem bedded at quasi intrinsic access and obtained at 37.5 output power.

1. Optimal second harmonic injection at the input.
2. Input second harmonic terminated into 50Ω.

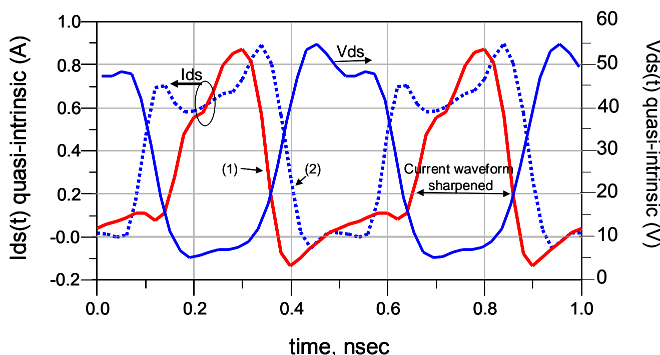

Fig. 10 Measured output waveforms embedded at quasi intrinsic access and obtained at 37.5 dBm output power.

1. Optimal second harmonic injection at the input.
2. Input second harmonic terminated into 50Ω.

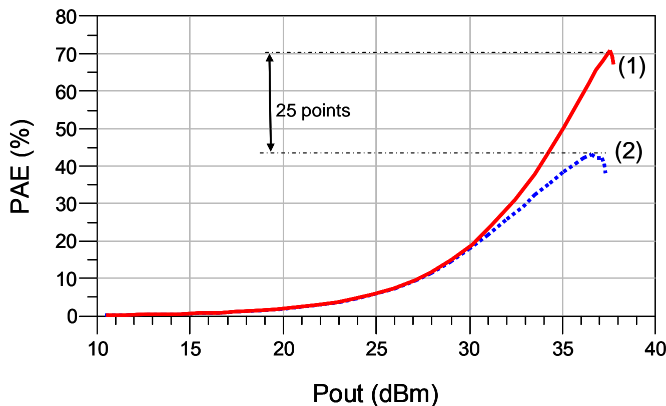

Fig. 11 Power added efficiency measurements versus output power :

1. Optimal second harmonic injection at the input.
2. Input second harmonic terminated into 50Ω.

These measurement results validate the study. It can be clearly observed that an appropriate gate source voltage shaping leads to a decrease of the ON time "t_{ON}" (as indicated in figure 9) ; a decrease of aperture angle (as indicated in figure 10) and a corresponding significant 25 point PAE enhancement shown in figure 11) .

V. Conclusions

This paper has demonstrated the prime importance of an appropriate gate-source voltage waveform control for the design of high efficiency GAN amplifier driven in saturation regime. A particular and original emphasis has been put on calibrated and "quasi intrinsic" time domain waveform measurements. Gate voltage waveform shaping with on/off transient times as quick as possible is the major challenge today to reach very high efficiency power amplifiers and target "Switching mode power amplifier design".

This work points out this feature and indicates potential interest in controlling a quasi half sine gate source voltage waveform. Other high efficiency operating conditions like inverse class F and class E have been also studied and can be discussed in the final paper. Work under investigation concerns now the design of a driver circuit capable to feed the input of GaN power transistor with optimal waveform shape for L-band applications.

Acknowledgment

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Efficiency enhancement of GaN power HEMTs by controlling gate-source voltage waveform shape.

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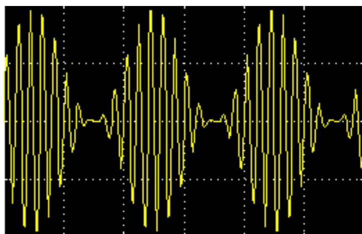
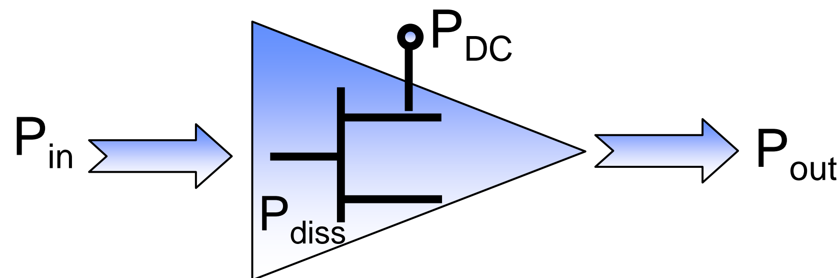
Outline

1. Introduction.
2. High Efficiency operation.
3. Gate source voltage waveform shaping.
4. Validation by time domain waveform measurements.
5. Conclusion.

1
Introduction

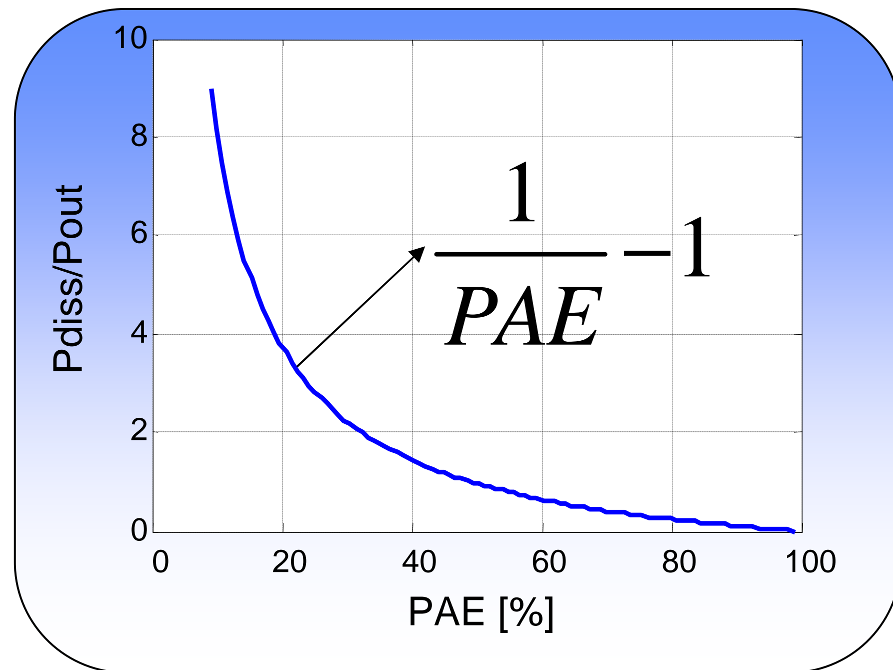
High Efficiency Power Amplifiers





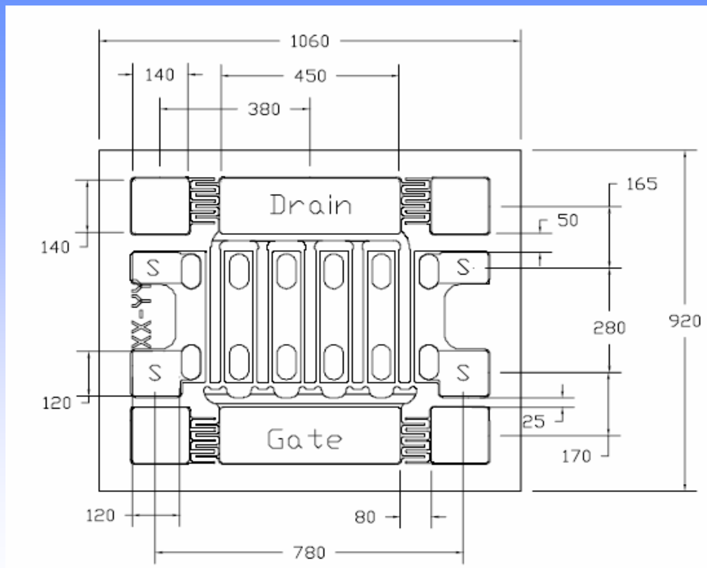
$$P_{in} + P_{DC} = P_{out} + P_{diss}$$

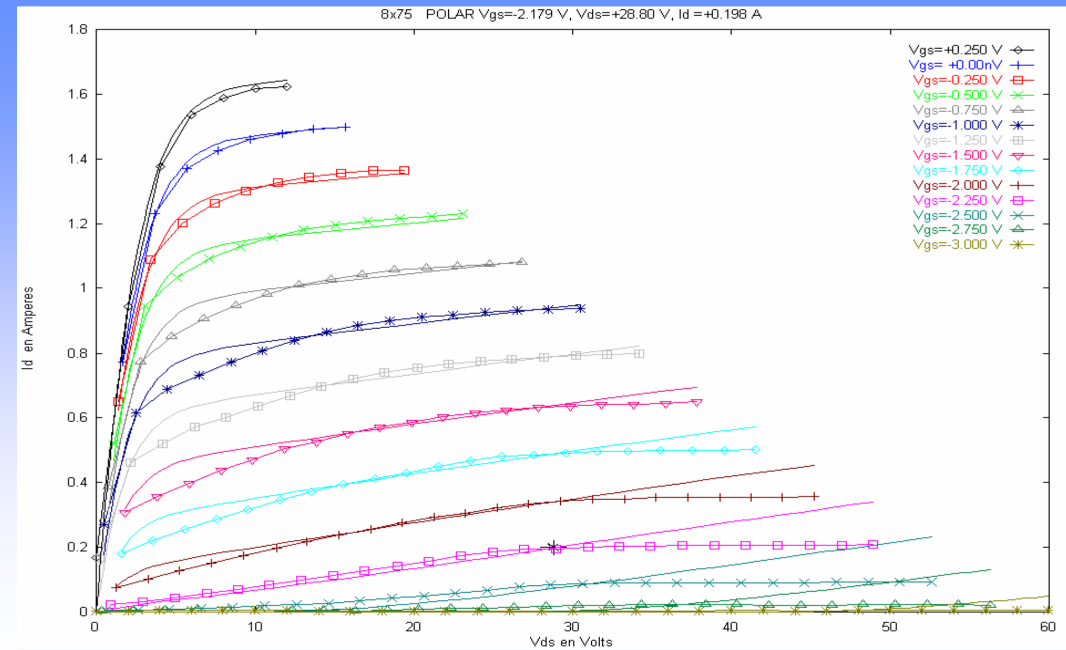
$$P_{diss} = P_{DC}\left(1 - \frac{(P_{out} - P_{in})}{P_{DC}}\right) = P_{DC}(1 - PAE)$$



- **High efficiency is Important to:**
  - **reduce power consumption**
  - **Decrease junction temperature (Tj) (better reliability)**
  - **Simplify thermal management (lower cost)**

Device used : 15 W GaN HEMT from CREE CGH60015D





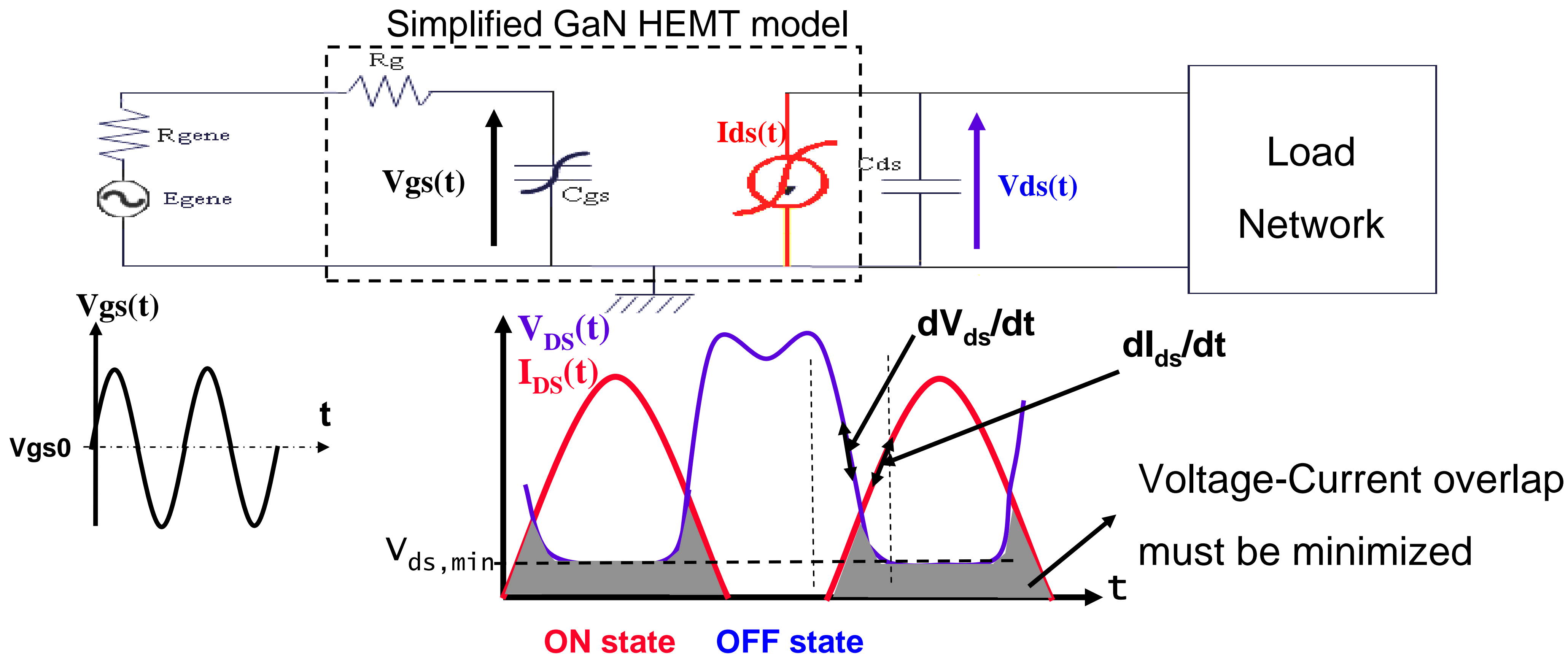
Characteristics of transistor used:

- ✓ V_{BK}>100V
- ✓ Rdson~ 2 ohm
- ✓ Cds=0.9 pF
- ✓ Cgs= 8 pF
- ✓ Rg=0.5 ohm

Device size 2mm

2 High efficiency operation.

High efficiency operation



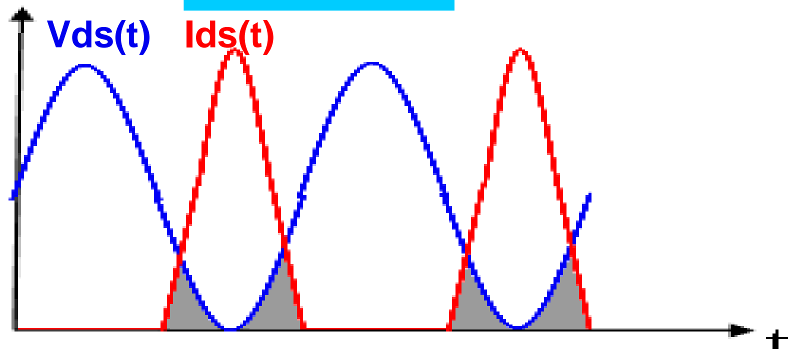
➢ **Minimization of dissipated power:**

During ON state Vds, must be minimum => Low $R_{ds,on}$

During transitions dV_{ds}/dt and dI_{ds}/dt must be maximum => Low capacitances (Cgs,Cds)

Load impedance controlled at the first three harmonics

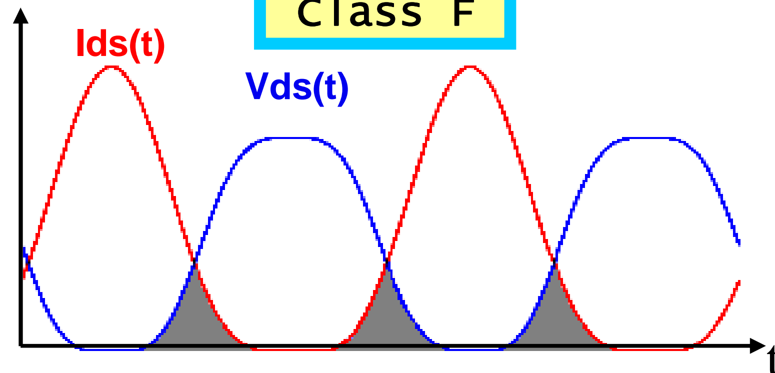
Class AB



2nd harmonic → **low impedance**

3rd harmonic → **low impedance**

Class F

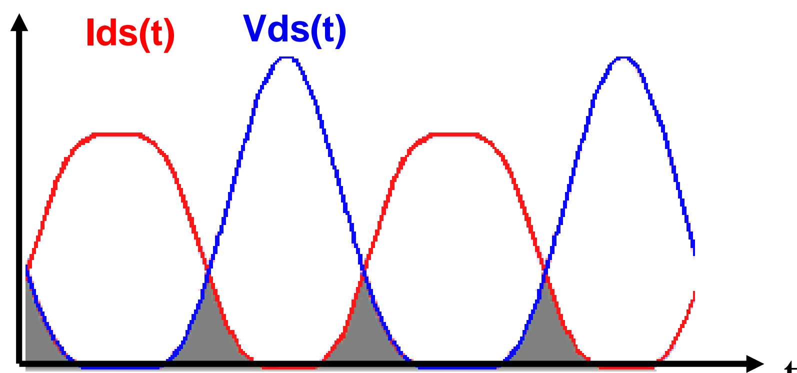


2nd harmonic → **low impedance**

3rd harmonic → **high impedance**

Load

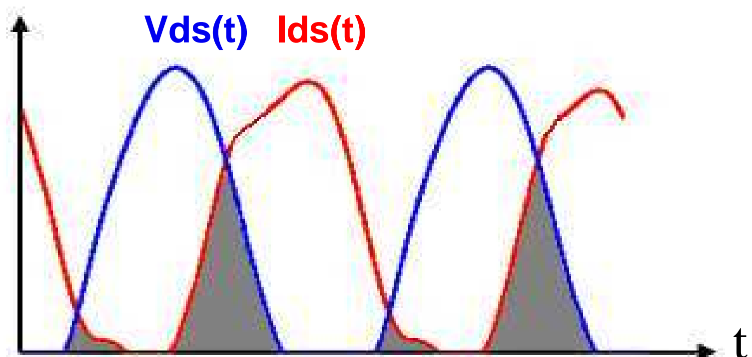
inverse Class F



2nd harmonic → **high impedance**

3rd harmonic → **low impedance**

Class E

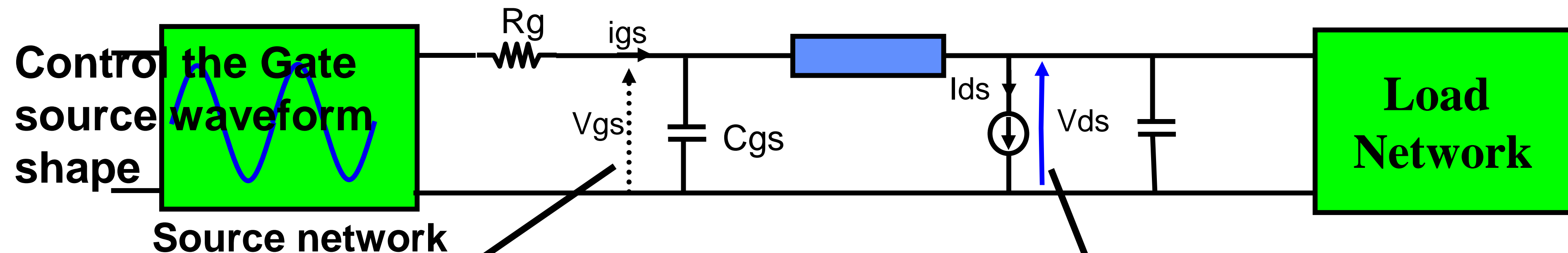


2nd harmonic → **high impedance**

3rd harmonic → **high impedance**

3 Gate source voltage waveform shaping.

PAE enhancement by gate source voltage shaping



Ids

Vgs

Vgs(t)

t

Second Harmonic injection

Ids(t) Vds(t)

t

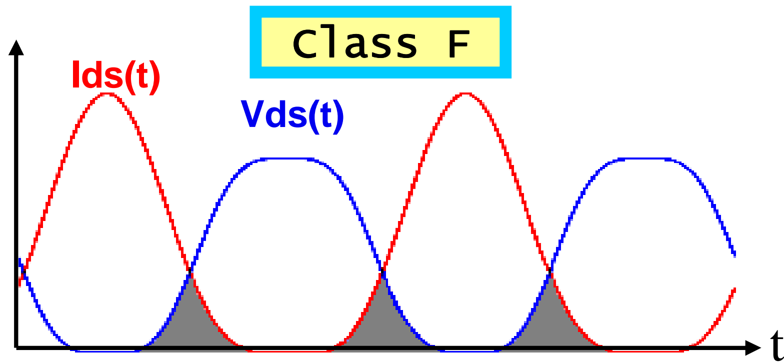
Aperture time

$$Vgs(t) = V_{gs0} + V_{gs1} * \cos(wt) + V_{gs2} * \cos(2 * wt + \phi)$$

$$Vgs_2 = \frac{Vgs_1}{7}, \phi = 0$$

Combination of gate source waveform shaping and load terminations

Class F



2nd harmonic → low impedance

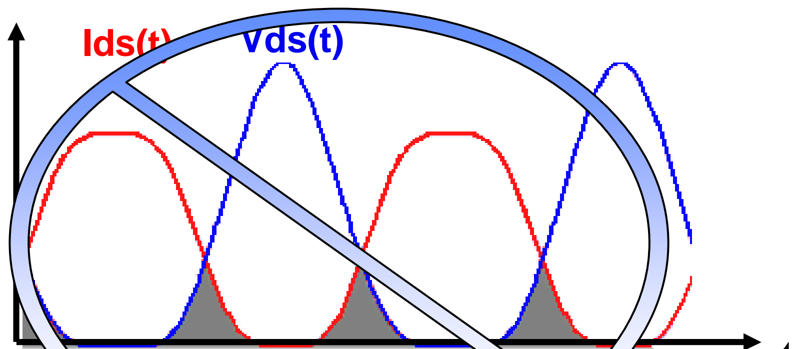
3rd harmonic → high impedance

2nd harmonic means Short circuit at output
(output drain current exists at 2nd harmonic)
We can inject H2 at gate port of transistor

Class F and input voltage shaping

Load

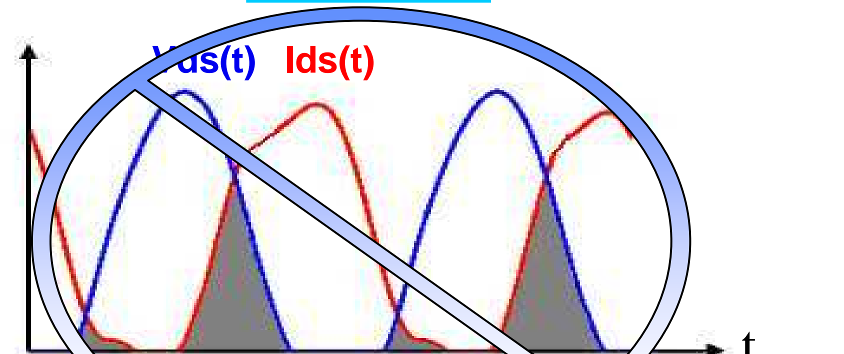
inverse Class F



2nd harmonic → high impedance

3rd harmonic → low impedance

Class E

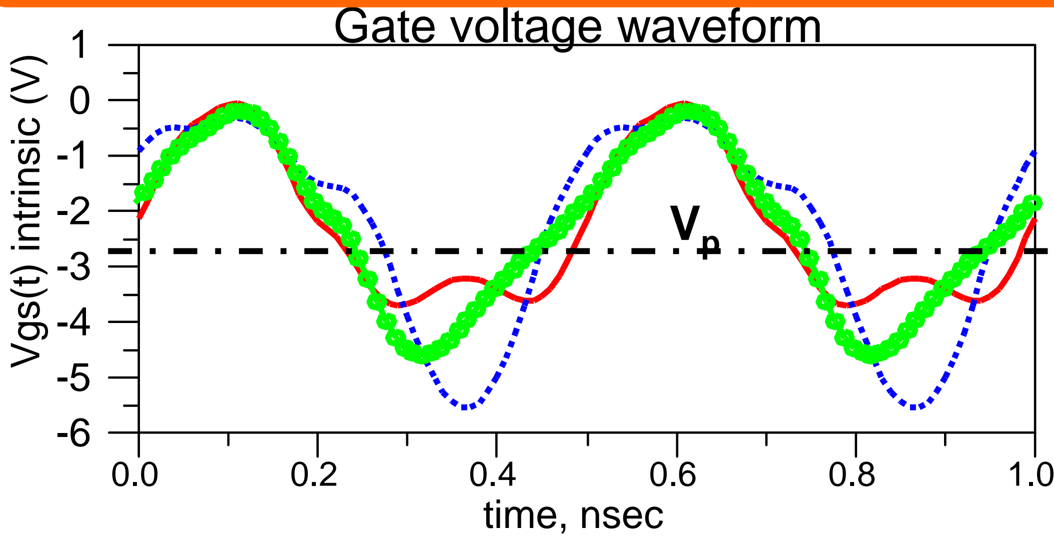


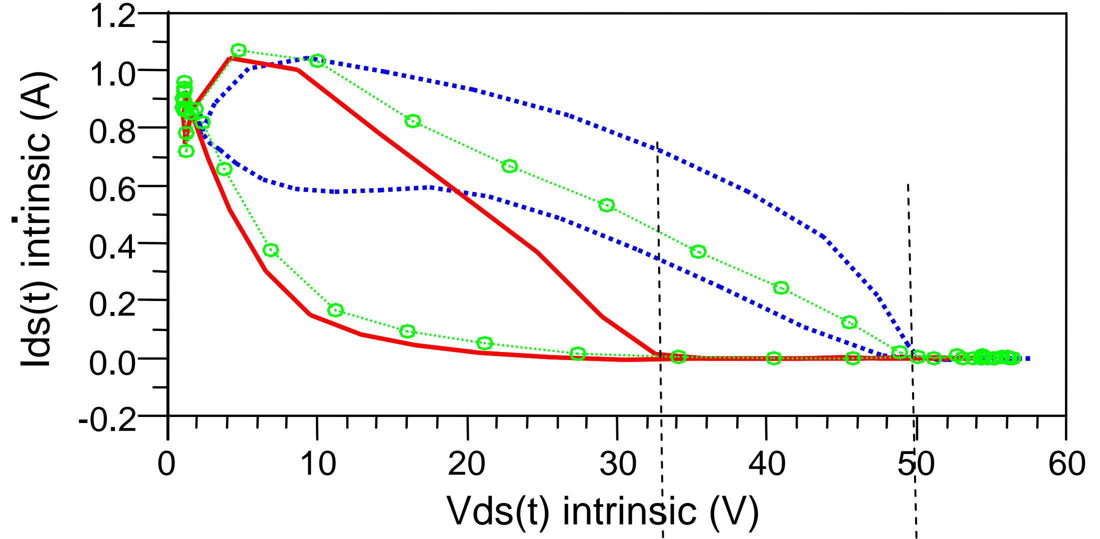
2nd harmonic → high impedance

3rd harmonic → high impedance

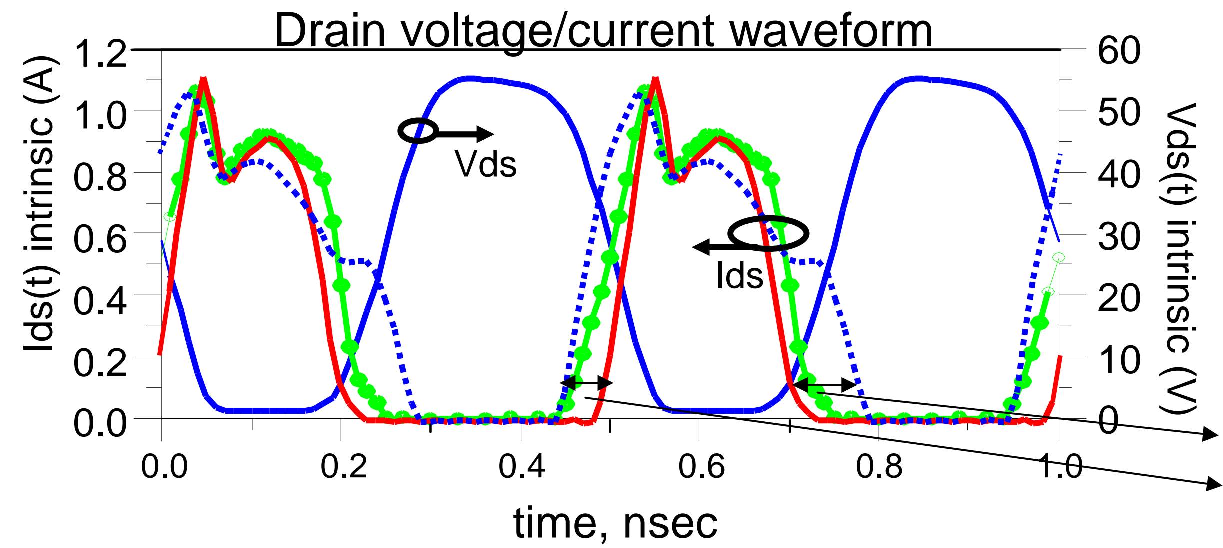
Simulation results : *Frequency = 2 GHz*

Source impedance at H2 =50Ω. Source impedance at H2 : short circuit.
second harmonic injection at the input





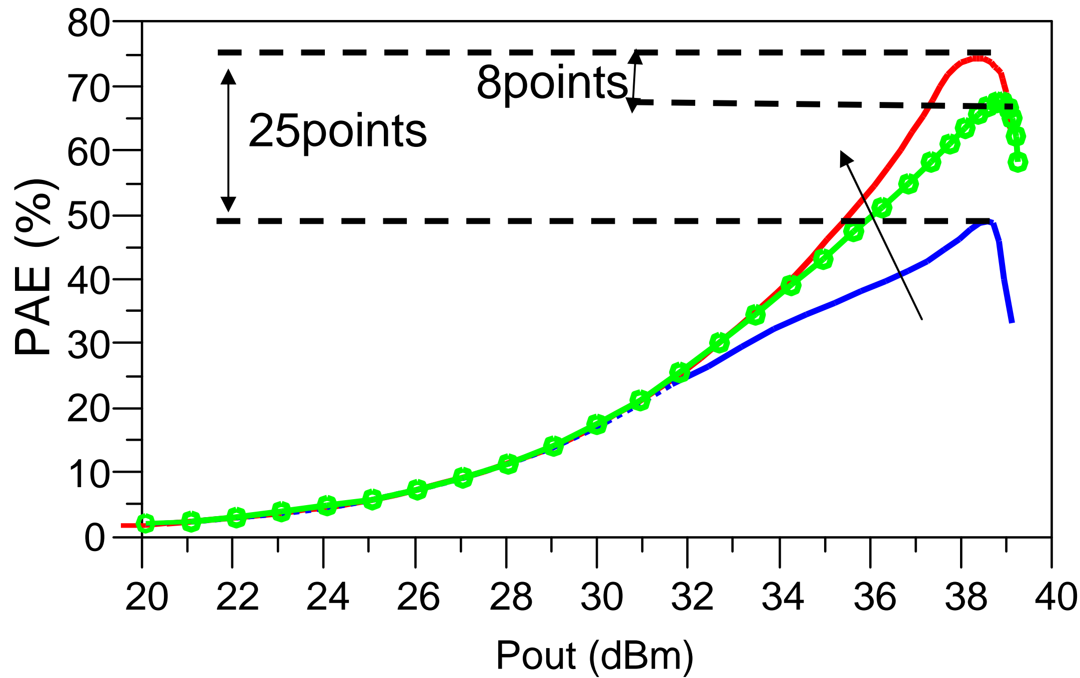
Increase of zero current duration

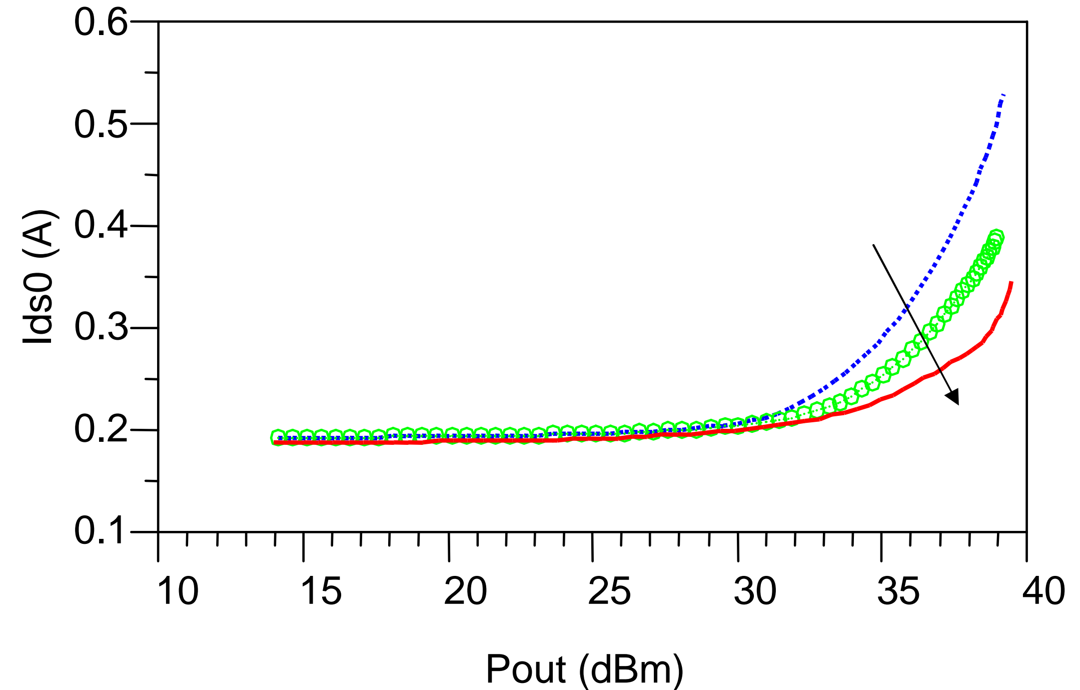


Aperture angle reduction
➔Efficiency enhancement

Simulation results : Frequency = 2 GHz

.... Source impedance at H2 =50Ω.
Source impedance at H2 : short circuit.
Second harmonic injection at the input

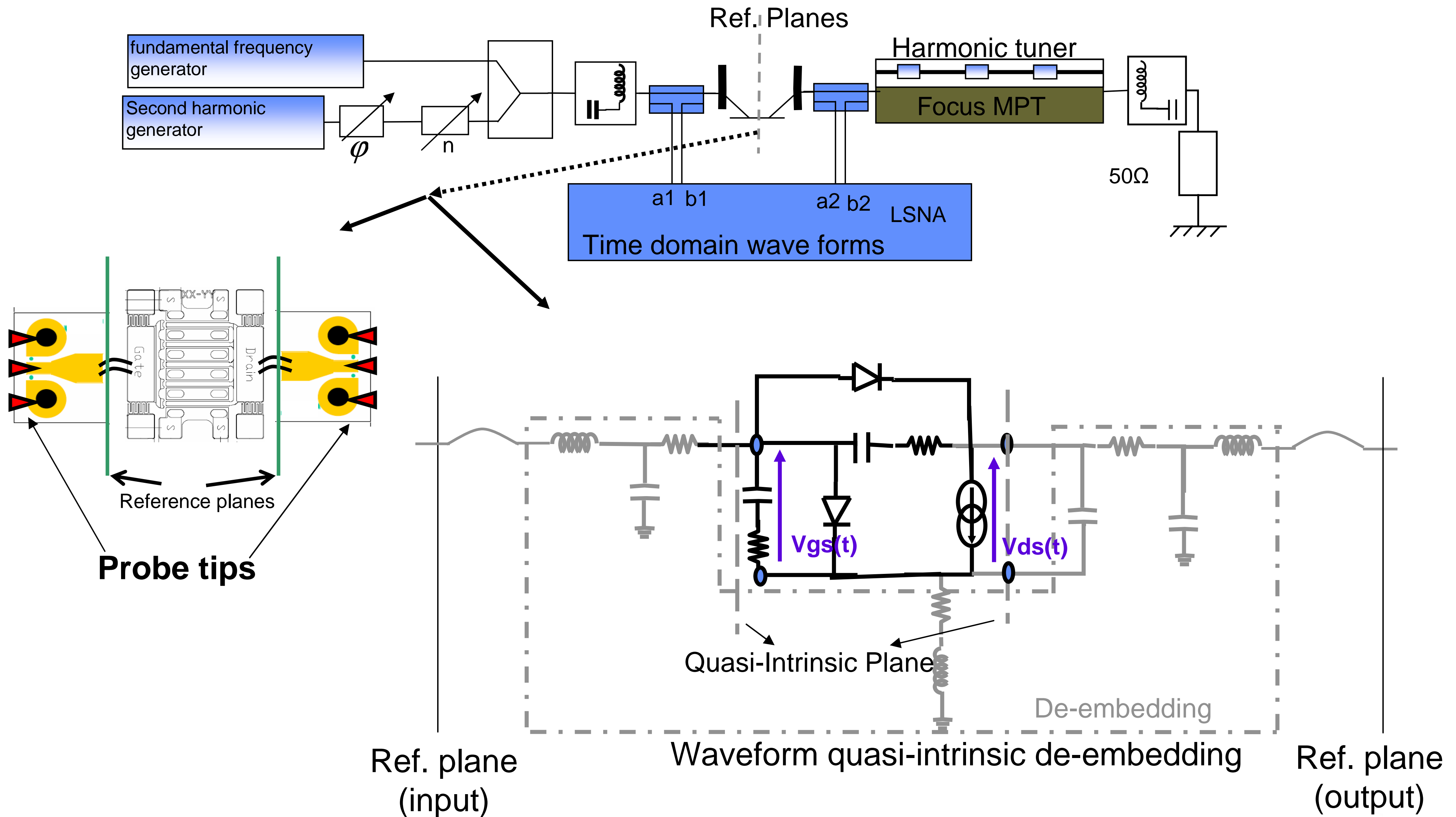




PAE improvements obtained by this technique due to a significant decrease of the DC drain current

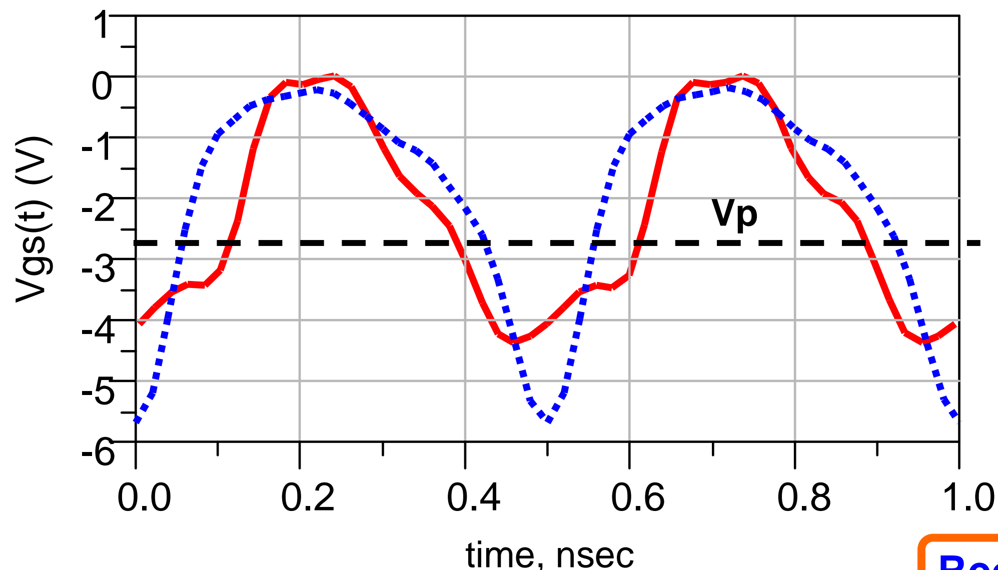
4 Validation by time domain waveform measurement.

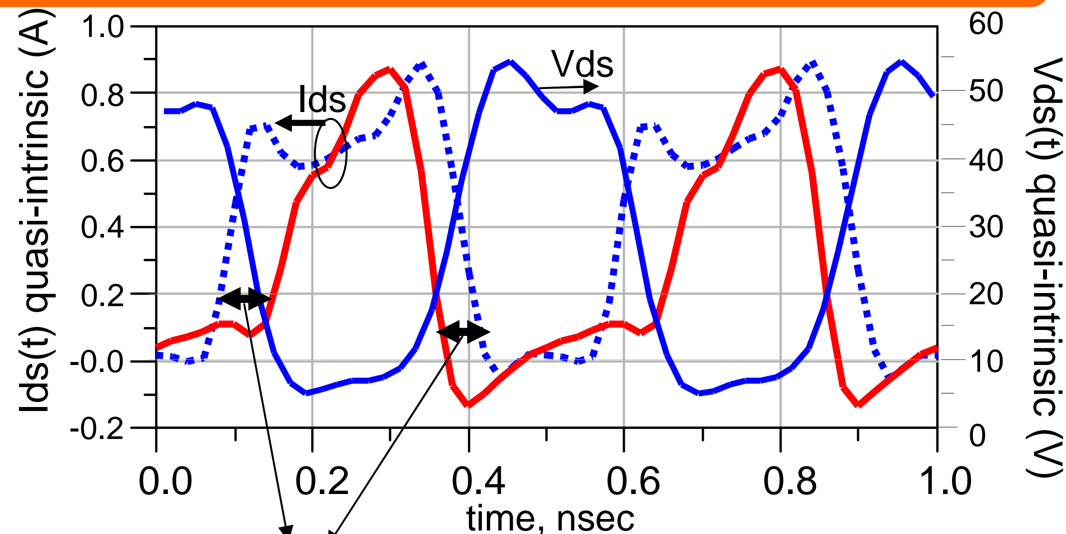
Time domain Load-pull measurements



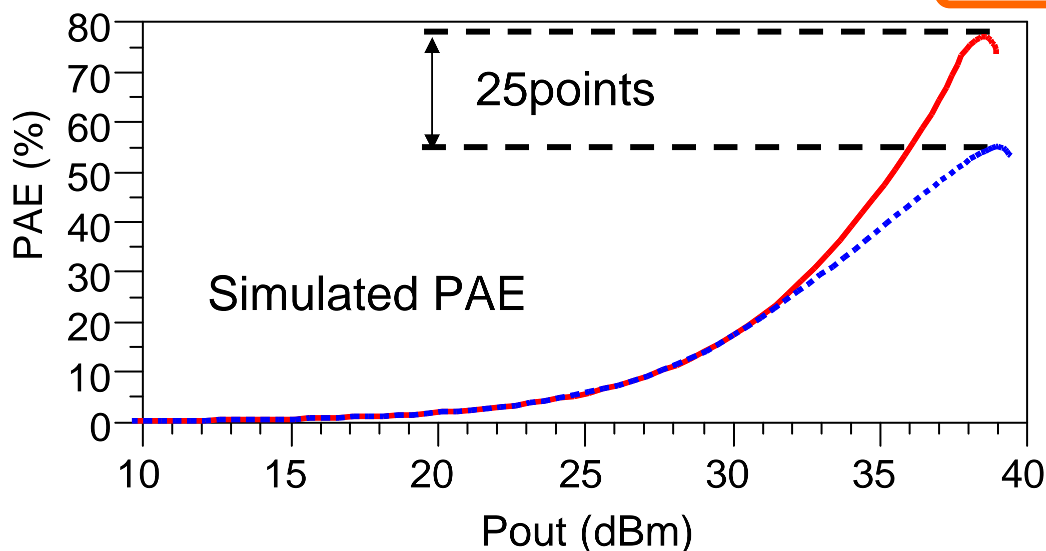
Time domain Load-pull measurements

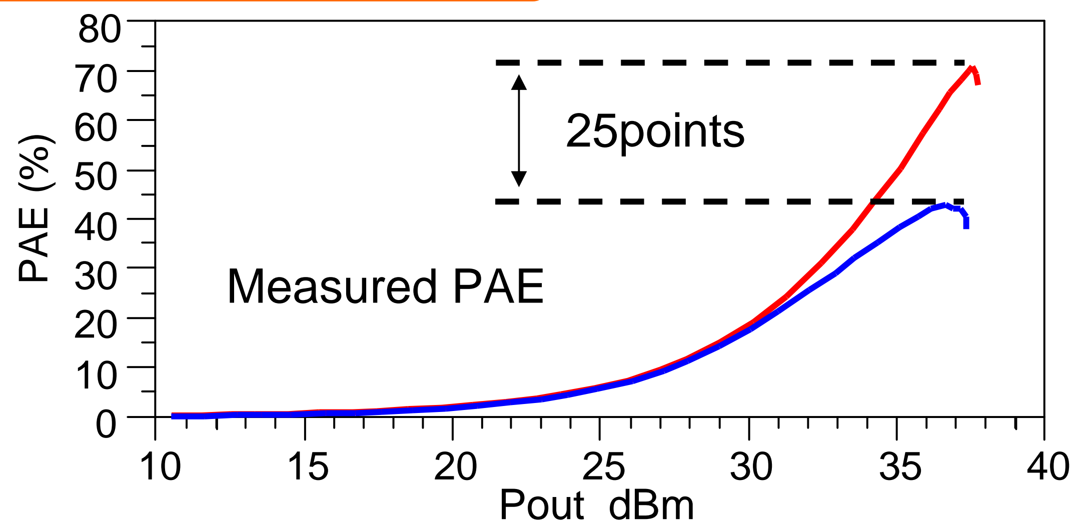
Source impedance at H2 =50Ω. Second harmonic injection at the input





Reduction of the aperture angle

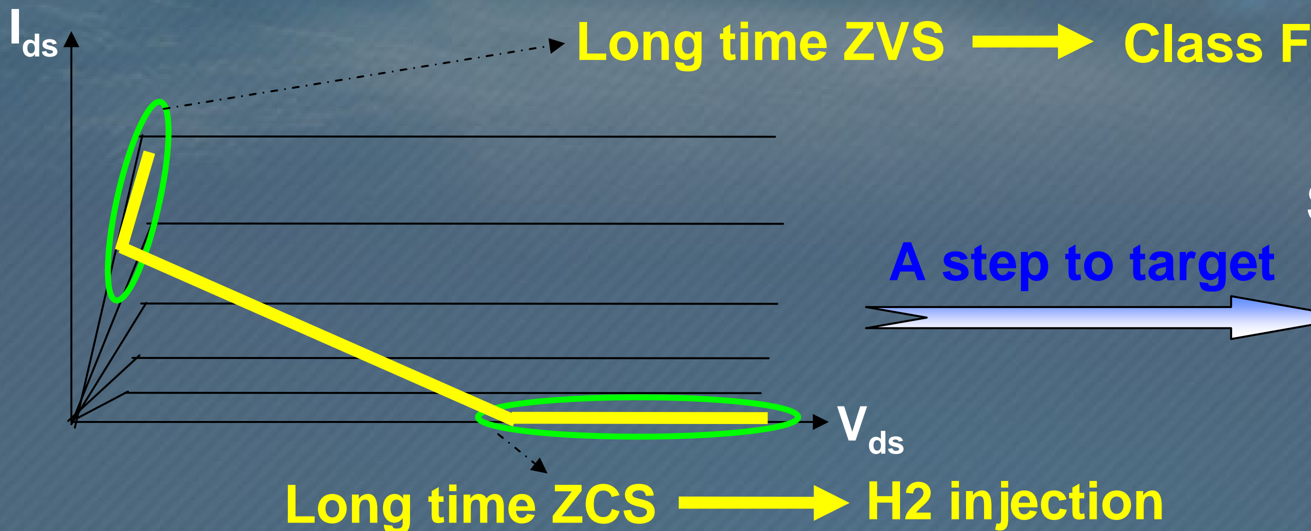




5
Conclusion

Conclusion

- This work has focused on gate source voltage waveform shaping for PAE optimization
- A main and original aspect of this work lies in measured time domain waveforms that validate transistor modeling and simulation results



A step to target

Switch mode power amplifier :

- ON: high I_{ds} / low V_{ds}
- OFF: high V_{ds} / low I_{ds}
- Fast transitions

Future work concerns design of two stage power amplifier

A driver has to be designed to achieve the appropriate gate source voltage waveform of the power stage.

Thank you for your attention

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