43W, 52% PAE X-Band AlGaN/GaN HEMTs MMIC Amplifiers

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***Abstract* — This paper presents the results obtained on X-Band GaN MMICs developed in the frame of the Korrigan project launched by the European Defense Agency. GaN has already demonstrated excellent output power levels, nevertheless demonstration of excellent PAE associated to very high power in MMIC technology is still challenging. In this work, we present State-of-the-Art results on AlGaN/GaN MMIC amplifiers. An output power of 43W with 52% of PAE was achieved at 10.5 GHz showing that high power associated with high PAE can be obtained at X-band using MMIC GaN technology.**

***Index Terms* — GaN, HEMT, MMIC, power amplifier, X-band.**

I. Introduction

The presence of piezoelectric effects in the GaN material leads to the presence of piezoelectric charges at interfaces, giving a 2-dimensional electron gas with an electron density larger than that created in GaAs HEMTs using intentional doping. The large bandgap of 3.4eV results in a high breakdown field of 3MV/cm, the thermal conductivity of GaN at 300K is $190 Wm^{-1}K^{-1}$ and that of SiC is $400 Wm^{-1}K^{-1}$ allowing a good dissipation of the heat generated in the channel. On the other hand the high breakdown field allows an increase in bias voltage by a factor of at least 5. These combined characteristics lead to power densities up to a factor of 10 times larger than in GaAs HEMTs [1],[2],[3],[4]. The higher power available in GaN devices means that there is an opportunity to trade power for PAE. In this work, we report on the performances obtained with MMIC power amplifiers at X-band on AlGaN/GaN HEMT technology on SiC substrate.

II. Device Fabrication

The AlGaN/GaN HEMT epitaxial layer was grown on a silicon carbide substrate by low-pressure metal organic chemical vapor deposition (MOCVD). Electrical isolation of devices was performed by helium implantation. Ti/Al/Ni/Au ohmic contacts were formed using rapid thermal annealing at temperature of 900°C. Mean contact resistance extracted from TLM measurement is 0.2 Ω.mm. Mo-based T-gates with 0.25µm length were defined by electron beam lithography. The devices were then passivated using plasma enhanced chemical vapor deposition (PECVD) of SiO_2/Si_3N_4. After front side processing, the SiC wafer was thinned down to 100 µm. Plasma etching via-holes technology was used to ground the devices. Fig.1 shows the gain current cut-off frequency (Ft) and maximum available gain cut-off frequency (Fmag) for various total gate width devices.

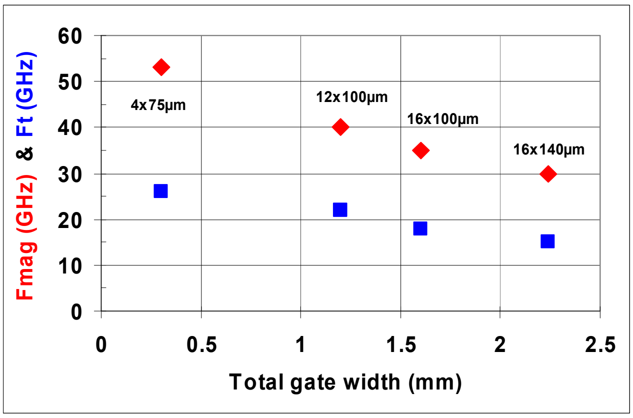

Fig. 1. Fmag and Ft evolution versus total gate width (Vds=5V, Ids=100mA/mm)

A typical power device of 1.6mm total gate width presents a Ft value of 18 GHz and a Fmag value of 35 GHz. A ratio of 2 between Ft and Fmag values is well conserved from elementary to power devices.

III. Device Topology

Elementary devices are based on 16x100µm topology. This power device, presented on Fig. 2, is used both in the first and second stage. It has a maximum available gain of 11.8dB at 10 GHz and a maximum available gain cut-off frequency of 35 GHz at a Vds voltage of 20V and 320mA of drain current in continuous mode.

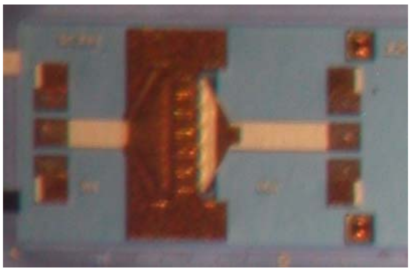

Fig. 2. Photograph of the microstrip 16x100µm power device.

Fig. 3 shows load-pull power measurements of this 1.6mm device at 10 GHz. Measurements are performed in pulse mode with a pulse length of 10µs with 10% of duty cycle and without any harmonic frequencies optimization. The device is biased at a voltage of 25V and a quiescent drain current of 430 mA. At the optimum load at the fundamental frequency for maximum PAE (5+j.5 Ω), the device shows a PAE of 55% with a typical output power of 38dBm (6.4W) corresponding to a power density of 4W/mm and 9.5dB of associated gain. The linear gain is 11dB. At the optimum load at the fundamental frequency for maximum output power (10-j.2 Ω), the output power reached 40.6dBm (11.4W – 7.1W/mm) with 51% of associated PAE and 10dB gain. Appropriate harmonic tuning and re-tuned of the fundamental frequency bring the optimal impedances for maximum power and PAE together and thus contribute to increase the output power and PAE of devices in MMIC circuits.

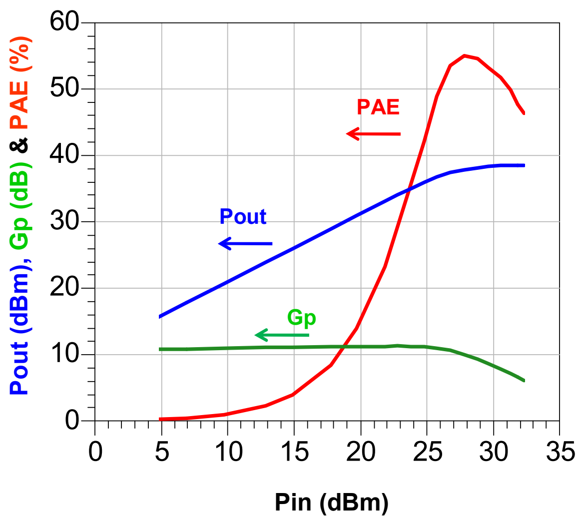

Fig. 3. Load-Pull measurement of 16x100µm device at optimum load for PAE. (Vds_0=25V, Ids_0=430mA, F_0=10 GHz, pulsed 10µs/10%).

IV. Amplifier Design

Amplifier is based on two stages architecture (Fig. 4). Two devices are used in the first stage which drives four transistors in the output stage. The chip size is 4500 x4000 µm² (18 mm²). Due to the high level of output power reached and in order to reduce both DC and RF losses in the transmission lines of matching and biasing networks, electroplated gold layer of 6µm thickness was deposited on the output combiner as well as on the first and on the inter-stage combiners. A parallel RC network in series at the input of each transistor enhances the stability of HPAs and prevents the occurrence of parametric oscillation phenomena [5]. The simulation of the stability of these amplifiers was first performed in linear operation mode at the quiescent biasing point. Then, the non linear stability was analyzed at high input power level [6].

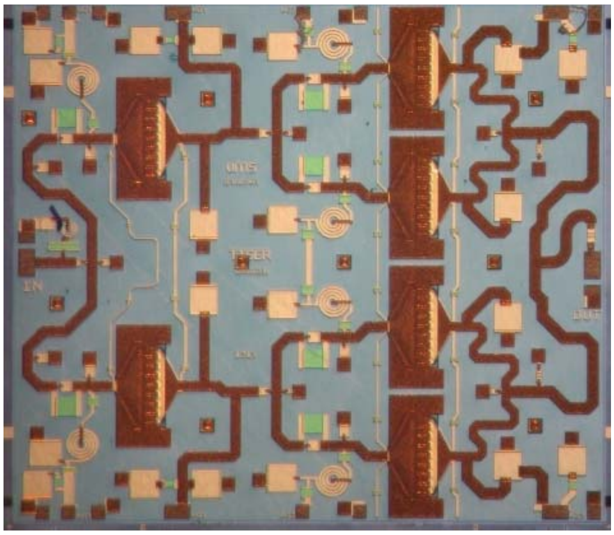

Fig. 4. Photograph of amplifier.

V. Amplifier Results – Batch 1

Different batches of amplifiers were realized. This part presents results obtained in the frame of the first one. Amplifiers were first measured on wafer with a pulsed S-Parameter bench. Fig. 5 shows S-Parameter measurements of amplifier at reduced drain voltage of 20V and drain current of 2A.

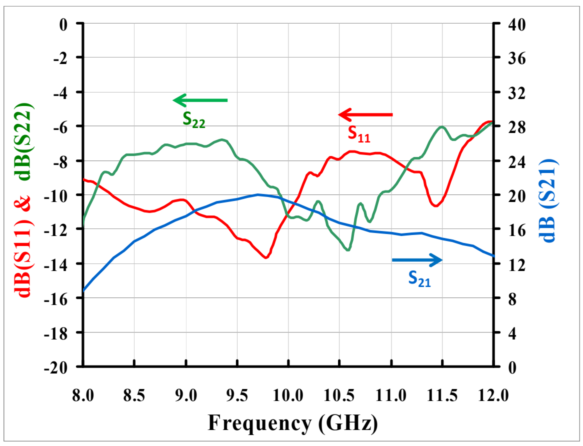

Fig. 5. On wafer pulsed S-parameter measurements of amplifier (Vds_0=20V, Ids_0=2A).

S_{11} and S_{22} are better than -7dB in the [8.5-10.5] GHz bandwidth. S_{21} is better than 14dB with a maximum of 20dB at 9.8 GHz.

Amplifiers were then characterised at large signal input power with drain pulse length of 20µs with 10% of duty cycle. The drain voltage and quiescent current are respectively 25V and 2.5A. Fig. 6 shows the output power, associated gain and PAE of the amplifier over the frequency range of 8.5 GHz to 10.5 GHz at an input power of 32dBm.

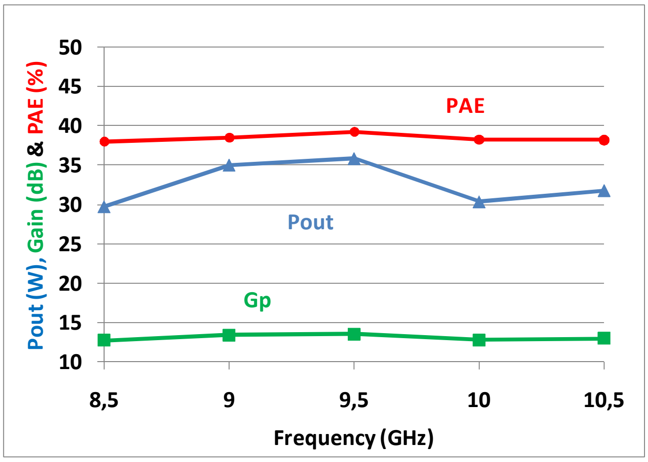

Fig. 6. On wafer measurements of amplifier (batch1) at 32dBm of input power (Vds_0=25V, Ids_0=2.5A).

The amplifier delivers a maximum output power of 45.5dBm (35.8W) with 39.5% of PAE and 13.5dB of associated gain at 9.5 GHz. Over the 2 GHz bandwidth, the output power is above 30W with a very flat PAE between 38% and 39.5%. The compression level of 4dB enables the amplifier to deliver its best PAE. The small signal gain is 17.7 dB at 9.5 GHz.

Amplifiers were then mounted in typical test Jig presented in Fig. 7. The chip is glued directly on the Jig without additional heat spreader.

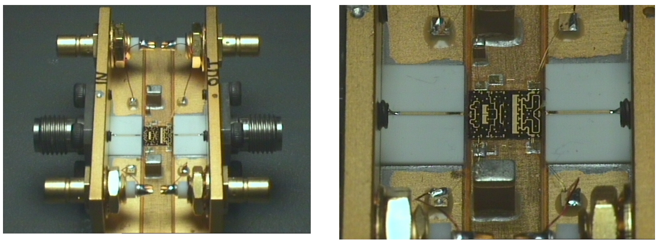

Fig. 7. Typical amplifier mounted in test Jig.

Fig. 8 shows the results for various pulse conditions: short pulse of 5 µs length with 10% of duty cycle and for long pulse condition of 50 µs length with 20% of duty cycle.

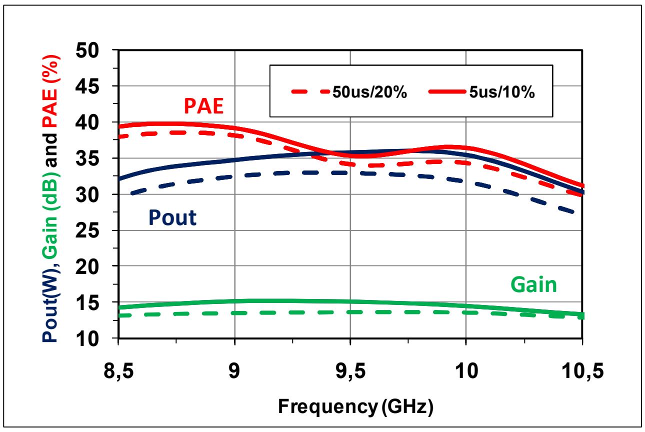

Fig. 8. Output power, Gain and PAE of amplifier in test Jig at input power of 32dBm (Vds0=25V, Ids0=2.3A) for different pulse conditions.

Between the two pulse conditions the output power decreases by 3W in the bandwidth corresponding to around 8% of power losses. The PAE decreases by around 2 pts. The high level of output power and PAE are well retrieved. The differences of behaviour in the bandwidth can be explained by the use of input and output wire bondings for RF connections.

VI. Amplifier Results – Batch 2

A second batch of amplifiers was processed without any design modification. Fig. 9 shows on wafer performances at 10.5 GHz. The amplifier shows 2dB more gain than amplifier from batch n°1 and power performances slightly shifted towards high frequencies.

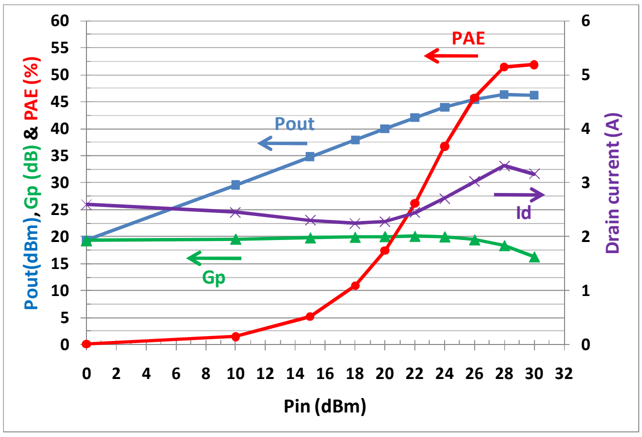

Fig. 9. Gain, Ouput power, PAE and drain current of amplifier (batch2) at 10.5 GHz versus the input power (Vds_0=25V, Ids_0=2.2A, pulsed 20µs/10%).

The amplifier delivers a maximum output power of 46.3dBm (43W) corresponding to a power density of 6.7 W/mm with 52% of PAE and 16.3dB of associated gain. To our knowledge, this result represents State-of-the-Art PAE obtained with X-band GaN MMIC amplifier with over 10W of output power. Fig. 10 shows the power performances measured from 8.5 GHz to 11 GHz.

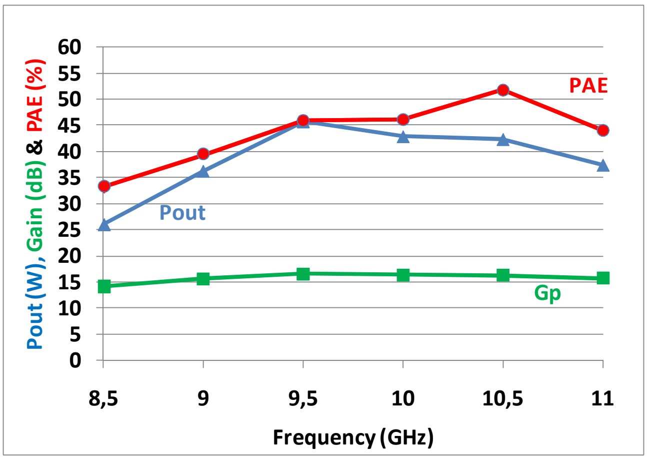

Fig. 10. Gain, Ouput power and PAE of amplifier (batch2) at pin=30dBm (Vds_0=25V, Ids_0=2.2A, pulsed 20µs/10%).

The output power is above 35W with PAE higher than 40% on 2 GHz bandwidth. Fig. 11 represents, to our knowledge, the state of the art results of GaN HPA MMIC in X-Band. While many results have been already reported with PAE up to 67% with lower output power, this paper reports a PAE of 52% with 43W of output power showing that high power and high PAE can be achieved at X-band using GaN technology.

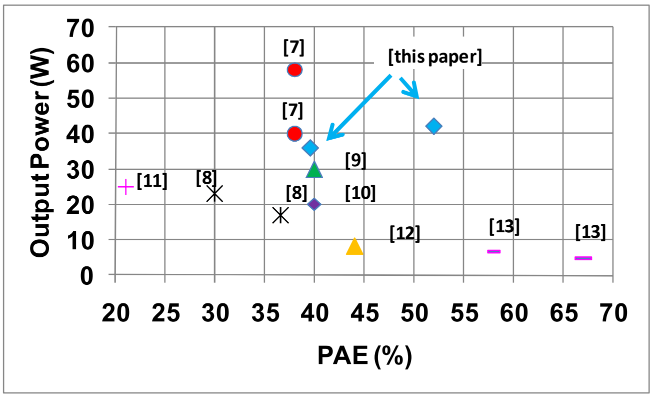

Fig. 11. State-of-the-Art GaN MMIC HPAs in X-Band

VII. CONCLUSIONS

In this paper we present results obtained on X-band MMIC amplifiers using AlGaN/GaN HEMT 0.25µm gate length technology developed in the frame of the European KORRIGAN contract.

A first batch of 18mm² MMIC amplifiers exhibited a maximum output power of 45.5dBm (35.8W) with 39.5% of PAE and 13.5dB of associated gain at 9.5 GHz. Over the 2 GHz bandwidth, the output power is above 30W with a very flat PAE between 38% and 39.5%. On wafer and in test Jig measurements were performed under pulse conditions.

A second batch allows us to obtain State-of-the-Art results: An output power of 43W with 52% of PAE was achieved at a drain bias voltage of 25V showing that high power and high PAE can be obtained in X-band using GaN technology. An output power of above 35W with PAE higher than 40% over 2GHz of bandwidth were measured. This paper demonstrates once again the great interest of GaN technology for X-band radar applications.

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