Performances of AlInN/GaN HEMTs for Power Applications at Microwave Frequencies

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Abstract— **We report a comparative study on AlInN/GaN HEMTs on SiC substrates having four different processes and epitaxies. The outstanding performances of such devices will be explained thanks to intensive characterizations: pulsed-IV, [S]-parameters and load-pull at several frequencies from S to Ku bands.**

The measured transistors with 250nm gate lengths from different wafers delivered in cw: 10.8 W/mm with 60 % associated PAE at 3,5 GHz, 6.6 W/mm with 39% associated PAE at 10,24 GHz, and 4.2 W/mm with 43 % associated PAE at 18 GHz.

I. Introduction

AlInN/GaN HEMTs are now competing with AlGaN/GaN HEMTs in several laboratories, and several publications have been recently edited showing very impressive power performances at microwave frequencies [1-4], despite the weak maturity of the processes. One of the main advantages of this material compared to AlGaN/GaN is the lattice match between the $Al_{82}In_{18}N$ and the GaN, leading to a reduction of the mechanical constraints, and potentially of the dislocation densities compared to AlGaN/GaN, while having higher polarization effects [5-7].

In this paper we present the latest results obtained at Alcatel-Thales III-V Lab, and particularly large-signal measurement results, showing the strong potential of this new technology, and confirming the theoretical expectations [8]. This study has been done on several wafers with different processes or epitaxial growths, and their impact on the devices characteristics is extensively studied thanks to characterizations such as pulsed-IV and [S]-parameters.

II. Epitaxial Growth and Device Processing

Four wafers have been characterized, named A, B, C, and D. Their characteristics are presented here.

Epitaxial layers were grown of SiC substrate by Low Pressure Metal Organic Chemical Vapour Deposition (LP-MOCVD) using a 2-inch single wafer reactor. The heterostructures consist in a 1.7µm insulating GaN buffer layer, a 1 nm thick AlN spacer layer and an undoped AlInN layer with approximately 18% of Indium content. Different thicknesses of this layer have been grown on the different wafers, as presented at Table I. At this content, AlInN grown on GaN is near lattice matched conditions, i.e. almost without strain. Adding an AlN spacer layer at the AlInN/GaN interface allows to enhance the carrier mobility, as reported in [9].

Contactless sheet resistance measurements are reported in table I for each wafer. After Molybdenum based alignment marks lift-off, ohmic contacts were formed by rapid thermal annealing of Ti/Al/Ni/Au multilayer at 900°C during 30s under nitrogen ambient. Their average resistance was measured to be 0.15±0.02 Ω.mm. Argon ion implantation was used for device isolation. 250 nm Ni based T-Gates were formed by e-gun evaporation after electron beam lithography. The fourth wafer has different gate metallization than the other ones, inducing a gate resistance reduction by a factor 2 (*cf* Table II, the resistance values provided are measured on specific gate-metal meander line test devices). The devices were passivated with a 250 nm thick Si_3N_4 layer deposited by plasma enhanced chemical vapour deposition. A Ti/Pt/Au multilayer deposited by e-gun was used as interconnections. Multifinger device 3D interconnects were fabricated with plated gold bridge technology on photosensitive BCB.

TABLE I
EPITAXIAL CHARACTERISTICS

Wafer	**A**	**B**	**C**	**D**
eInAlN (nm)	10	10	7	11.5
Rsheet (Ω)	320	320	300	311
Ns (cm-2)	$1.5.10^{13}$	$1.5.10^{13}$	$1.9.10^{13}$	$1.3.10^{13}$

TABLE II
GATES METALLIZATION AND RESISTANCE

Wafer	**A**	**B**	**C**	**D**
Gate type	Ni/Au	Ni/Au	Ni/Au	Ni/Pt/Au
Rg (Test device) (Ω)	44	48	47	23

III. Pulsed IV-Measurements

Pulsed IV measurements have been performed on 2x100µm transistors from the four different wafers described before.

The Table III presents some of the most important parameters extracted from these IV measurements.
Idss is expressed for Vdsi=10V on the networks at (Vgsq=0V, Vdsq=0V). *Vp* is the pinch-off voltage of the device, measured at Vds=5V.

The trapping effects were also characterized for 2x100µm transistors, using the method described in [10]: during the pulsed measurements, the devices under test are biased at chosen quiescent points (*Vgsq*, *Vdsq*). As the emission of charges is very slow compared to their capture, the instantaneous current *Idsi* measured during pulses depends either on the quiescent voltages or on the instantaneous voltages (*Vgsi*, *Vdsi*). The combination of quiescent bias points used is:
- (1) (*Vgsq*=0, *Vdsq*=0),
- (2) (*Vgsq*=*Vp*, *Vdsq*=0)
- (3) (*Vgsq*=*Vp*, *Vdsq*= 25V and 35V here);

The gate-lag (GL) is quantified by comparing (1) and (2), and the drain-lag (DL), by comparing (2) and (3).

In order to get a meaningful quantification of the lag effects, they are expressed in terms of potential power degradation: the achievable power is calculated thanks to the formulation giving the class A theoretical max power:

$$Poutmax = \frac{1}{8}.Imax(Vmax - Vknee)$$

Where: $$Vmax = 2.Vbias - Vknee$$

The difference between the estimated output powers calculated for each of the three IV networks is expressed in percents.
This calculation for each IV network leads to:

$$GL(\%) = 1 - \frac{(\Delta I'.\Delta V')}{(\Delta I.\Delta V)}$$

$$DL(\%) = 1 - \frac{(\Delta I''.\Delta V'')}{(\Delta I'.\Delta V')}$$

Parameters of these equations are graphically obtained, as shown at figure 1.

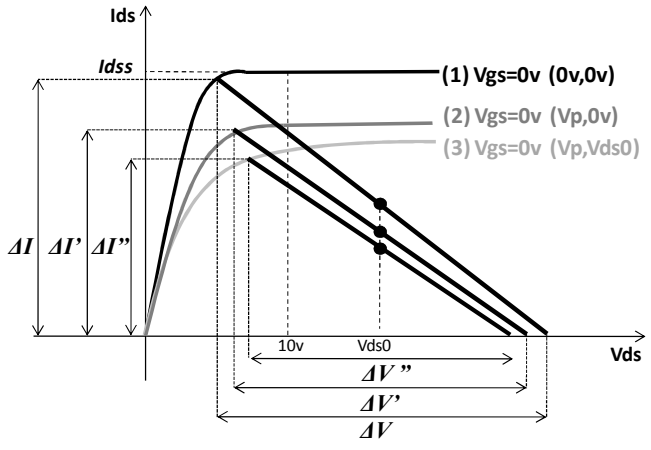

Fig. 1 Graphical estimation of the theoretical output power to calculate the impact of the lag effects.

The breakdown voltage is obtained thanks to the drain current injection technique presented in [11].

TABLE III
Pulsed-IV Parameters

Wafer	A	B	C	D
Idss (mA/mm)	1.2	1.2	1.28	1.22
Vp (V)	-2.65	-2.8	-2.7	-3.8
Gate-lag (%)	4	6	3	0
Drain-lag at Vds=25V (%)	9	12	19	17
Drain-lag at Vds=35V (%)	15	22	29	23
Vbk (V)	≈45*	≈83	≈70	>65*

**The breakdown voltages on wafers A and D could not be well estimated due to buffer current leakage, which alter the measurement results.*

The Idss values are very high and are in accordance with the high sheet carrier densities ns measured and presented in table I. In return, the breakdown voltages are quite low, hence limiting the drain bias voltages for power applications to lower values than the ones usually used with 250 nm gate length AlGaN/GaN HEMTs.

The lag effects differ from a wafer to another, but it has to be noted that the gate-lag effects are negligible for all the wafers. The drain-lag effects induce a power dispersion estimated between 9 and 19%.

IV. Small-Signal Measurements and Modelling

[S]-parameters have been measured on 8x75µm devices at Vds=15V, Ids=200 mA/mm, in order to obtain the frequency performances of these devices. They are presented at Table IV. The MSG/MAG transition frequency was lower than 20 GHz on the first three wafers, preventing their use in K band applications. It reaches 22.5 GHz for the last one thanks to the strong improvement of the gate resistance by using a Pt diffusion barrier in the gate metallization (*cf* Table II).

Small-signal models have been extracted from these measurements in order to evaluate the correlation between the fabrication aspects and the electrical performances. Some parameters of these models are presented at Table V. The gate resistance values extracted confirm the interest of the Ni/Pt/Au gate metallization, Rg being almost divided by two in the wafer D compared to the wafers A, B and C.

Besides, there is not a clear correlation between the values of the capacitance Cgs and the barrier layer thickness, which was expected to diminish with its increase. This is the case for Cgd, but not in a proportional manner.

TABLE IV
Small-Signal Parameters

Wafer	A	B	C	D
MSG/MAG trans. (GHz)	15.5	18	16	22.5
Max gain @ 10GHz (dB)	13.8 MSG	13.2 MSG	14.1 MSG	12.7 MSG
Max gain @ 20GHz (dB)	7.8 MAG	8.3 MAG	8 MAG	10.1 MSG

TABLE V
EQUIVALENT SMALL-SIGNAL MODEL PARAMETERS

Wafer	A	B	C	D
Rg (Ω)	2	1.8	2	1.05
Cgs (pF/mm)	1.88	1.842	1.473	1.56
Cgd (pF/mm)	0.151	0.172	0.293	0.193
Gm (S/mm)	0.373	0.482	0.467	0.415
Gd (S/mm)	0.015	0.015	0.019	0.017
Cds (S/mm)	0.192	0.348	0.368	0.193

V. LARGE-SIGNAL MEASUREMENTS

A. CW load-pull measurements at 3.5 GHz

Measurements have been performed on a 12x100 µm transistor from the wafer B in cw at 3.5 GHz in class A, at a quiescent drain current Ids_0=420 mA/mm. This wafer presents the lowest lag effects of the four wafers, and the best breakdown voltage.

We obtained a record performance of 10.8 W/mm and 60% of associated PAE at Vds=30 V, and a record PAE of 70% with an associated output power of 4,2 W/mm at Vds=15 V. The very linear increase of the output power versus the drain bias voltage shows the limited impact of the drain-lag on the transistors from this wafer.

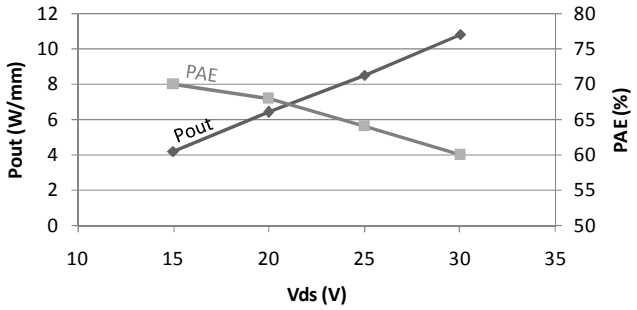

Fig. 2 Power performances of a 12x100µm transistor from the wafer B in cw , for different drain bias voltages in class A, (Ids=500mA) . The linear increase of the output power versus the drain bias voltage shows the little impact of the traps.

B. CW load-pull measurements at 10 GHz

Load-pull measurements in cw performed on wafer A have been presented in [2], and a record performance of 10,3 W/mm with 51% of PAE has been obtained at Vds=30 V for 4x75 µm devices in class AB.

New measurements were carried out on 8x75 µm transistors from the wafer D at 10.24 GHz in cw, at Ids_0=300 mA/mm, and at Vds=15, 20, 25 and 30 V. For each bias voltage, the load impedance was optimized in order to maximize the output power. The maximum power obtained is 3.5 W/mm with a PAE of 51% at Vds=15 V and 6,6 W/mm with a PAE of 39% at Vds=30 V. The devices showed almost no ageing at Vds=15, 20 and 25 V during the whole measurement campaign. At Vds=30 V, the devices exhibited 7,1 W/mm and 41% of PAE at the first measurement, and then the devices stabilized rapidly at the performances presented here.

The weak impact of the trapping effects can be attested by the limited decrease of the mean drain current in function of the input power before the gain compression, as explained in [12].

Moreover, it has to be underlined that despite the fact that the technology is still under development, we noted a very high reproducibility of the measurements performed on several devices of the wafer.

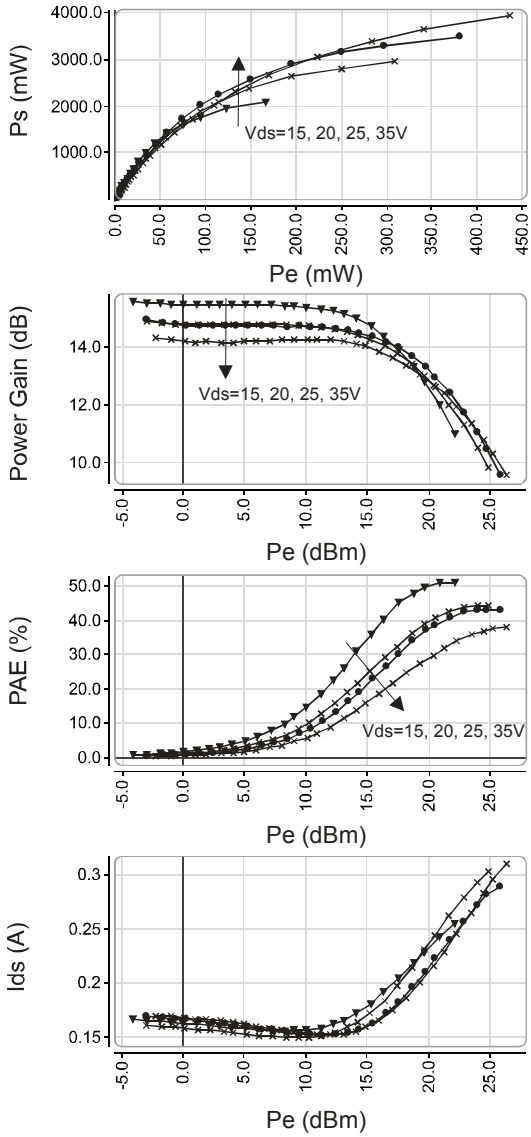

Fig. 3 Power performances of a 8x75 µm transistor from the wafer D in cw , for different drain bias voltages (15, 20, 25 and 30V) in class AB, (Ids=300 mA/mm) .

C. CW load-pull measurements at 18 GHz

In order to evaluate the power performances of AlInN/GaN components up to 18 GHz, we performed load-

pull measurements in cw on 8x75µm transistors from the wafer A. The performances obtained for the optimal load impedance for power added efficiency (PAE) are presented in Fig. 4.

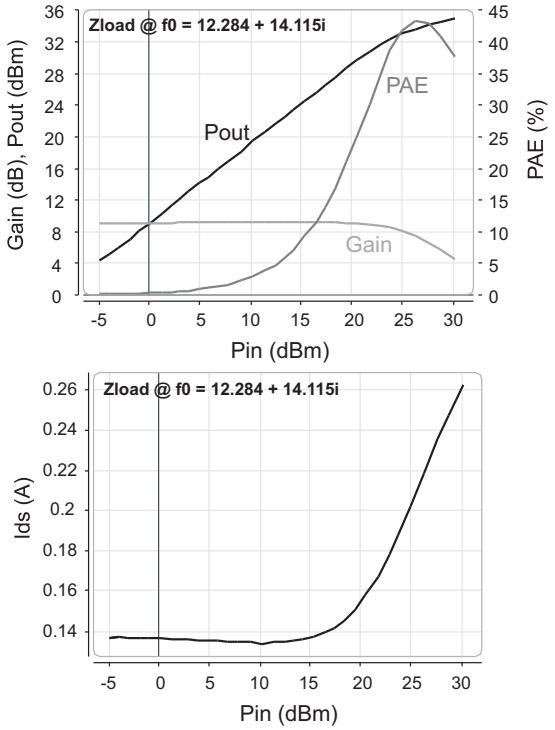

Fig. 4 Power performances of a 8x75 µm transistor from the wafer A obtained at 18 GHz in cw, Vds=20 V, Ids=250 mA/mm (class AB) on the optimal load impedance for PAE Zload=12,3+j14,1.

We obtained an output power of 34.1 dBm (2.5W) which correspond to 4.2 W/mm with a PAE of 43% and an associated gain of 6.5 dB. This relatively high value of PAE, as well as the negligible decrease of the mean drain current, shows tacitly the low level of drain-lag of these devices.

VI. Conclusions

An overview of the potentialities of the AlInN/GaN based HEMTs processed at Alcatel-Thales 3-5lab has been presented here. Despite the fledgling maturity of the technology, the measured devices exhibit excellent power performances, even in Ku band. High levels of PAE are obtained thanks to very limited trapping effects, which seem to be one of the main advantages of the AlInN/GaN compared to the AlGaN/GaN.

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