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Published in
IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES,
Volume 59, No. 3, March 2011, pp. 699-706.

doi:10.1109/TMTT.2010.2095033

Two-Stage GaN HEMT Amplifier With Gate–Source Voltage Shaping for Efficiency Versus Bandwidth Enhancements

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***Abstract*—In this paper a two-stage 2-GHz GaN HEMT amplifier with 15-W output power, 28-dB power gain, and 70% power-added efficiency (PAE) is presented.**

The power stage is designed to operate under class F conditions. The driver stage operates under class F^{-1} conditions and feeds the power stage with both fundamental and second harmonic components. The inter stage matching is designed to target a quasi-half sine voltage shape at the intrinsic gate port of the power stage. The goal is to reduce aperture angle of the power stage and get PAE improvements over a wide frequency bandwidth.

In addition to the amplifier design description, this paper reports original time-domain waveform measurements at internal nodes of the designed two-stage power amplifier using calibrated high-impedance probes and large signal network analyzer. Furthermore, waveform measurements recorded at different frequencies show that aperture angle remains reduced over large frequency bandwidth. In this study, a PAE greater than 60% is reached over 20% frequency bandwidth.

***Index Terms*—Aperture angle, classes F and F^{-1}, GaN power amplifier (PA), power-added efficiency (PAE), waveform measurements.**

I. Introduction

THE POWER amplifier (PA) remains a critical component in radio communication systems because it is an important energy consumer that impacts significantly the overall power consumption budget of a radio transmitter. Consequently, designing high-efficiency amplifiers is of prime importance to reduce power consumption, cooling requirements, and cost in RF transmit subsystem and to improve reliability aspects.

AlGaN/GaN HEMT technology has demonstrated a strong potential for high-efficiency high-power microwave amplification because of high electron mobility, high power density, and high breakdown voltage. High power-added efficiency (PAE) performances of microwave PAs are reached by implementing appropriate source and load matching conditions at harmonics. A lot of stuides have been carried out to investigate and demonstrate optimization strategies and procedures to enhance PAE performances of microwave PAs [1]–[16]. During the past years, many high-efficiency class F, class F^{-1}, class J, class E, and class D^{-1} GaN amplifiers have been reported [17]–[19]. High-efficiency performances and limitations of microwave PAs can be appreciated by observing the shape of voltage and current waveforms at transistor ports. Minimized overlapping between drain–current and drain–source voltage indicates a minimized dissipated power. Recently we have reported in [20] and [21] an experimental study and calibrated time-domain waveform measurements concerning PAE enhancement conditions of GaN HEMTs with active second harmonic injection at the gate port.

Following these studies, in this paper we present a two-stage GaN HEMT PA design. The driver stage provides appropriate second harmonic injection to the input of the power stage. An appropriate inter stage matching network has been designed to get a quasi-half-sine-wave gate–source voltage at the input of the power stage. In addition to the design of the PA, the main focus of this paper is to examine the aspect of enhanced PAE performances when the frequency is shifted away from the center frequency. This aspect concerning PAE versus bandwidth is not so frequently reported to authors' knowledge. Furthermore, an original point of the paper stands in accurate gate–source voltage waveform measurements at internal nodes of the amplifier at different operating frequencies to highlight appropriate operating conditions favorable to maintain very good PAE performances over a wide bandwidth.

This paper is organized as follows. In Section II, the principle used in this work to improve the PAE of a class F power transistor driven by a half-sine gate–source voltage is recapitulated and illustrated with simulation results. In Section III, the proposed two-stage PA design is presented and discussed. In Section IV, measurement results are given to validate the design methodology. A particular emphasis is laid on time-domain measurements at internal nodes of the PA using calibrated high-impedance probes and a large signal network analyzer (LSNA). Measurements of the gate–source voltage of the power stage are performed at different operating frequencies and are compared to the measurements of the gate–source voltage waveform of a single-stage class F amplifier having a conventional quarter-wavelength line topology at the gate port used either

Manuscript received October 05, 2010; revised October 11, 2010; accepted October 30, 2010. Date of publication December 17, 2010; date of current version March 16, 2011. This work was supported by the French Space Agency and by Thales Alenia Space.

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Digital Object Identifier 10.1109/TMTT.2010.2095033

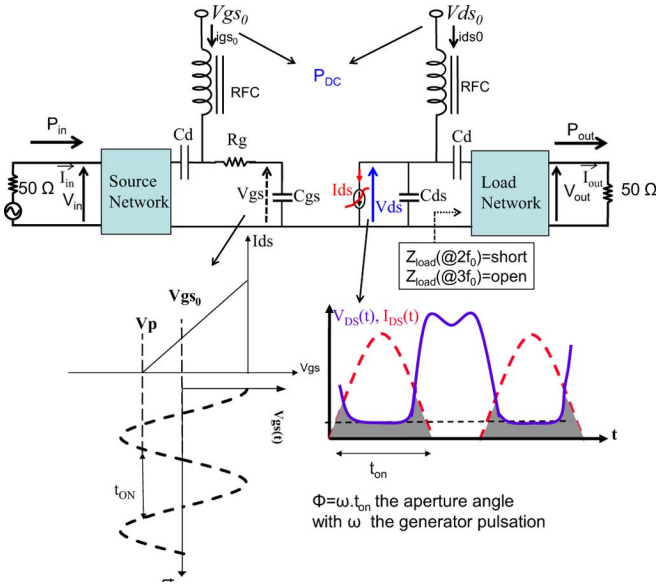

Fig. 1. Microwave class-F amplification principle and intrinsic waveforms.

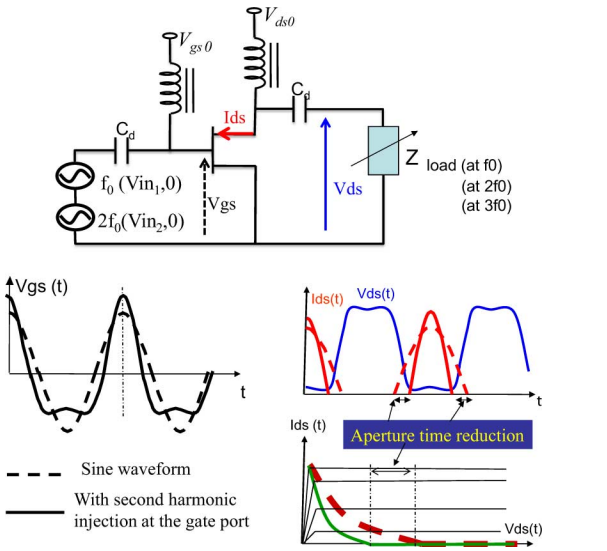

Fig. 2. Simulation methodology with second harmonic (H2) injection at gate port.

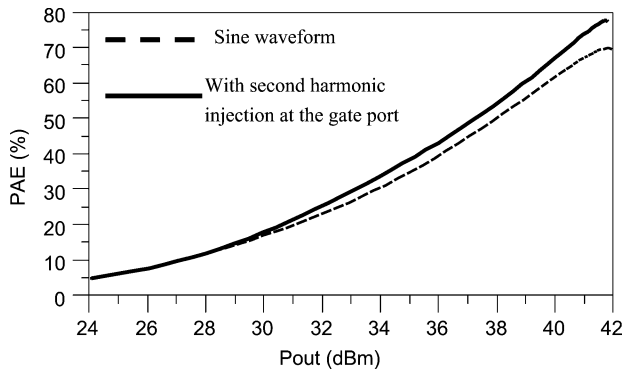

Fig. 3. Simulated PAE versus output power without (dotted line) and with (solid line) gate–source voltage shaping.

for biasing the gate and having a short-circuit termination at the second harmonic.

II. PAE Improvement of Class F GaN PA With a Half-Sine-Shape Gate–Source Voltage

At microwave frequencies, high-efficiency PAs are tuned at the first three harmonics. For class F operation, the intrinsic drain–source voltage of transistors approximates a square wave and the intrinsic drain–current approximates a half sine wave, as illustrated in Fig. 1.

The gate–source bias voltage Vgs_0 is close to or a little above the pinch-off voltage V_P. The RF gate–source voltage is a sine wave and load impedances at second and third harmonics are, respectively, close to a short and an open. Voltage and current waveform overlapping illustrated by the gray area in Fig. 1 must be reduced as much as possible to maximize efficiency.

A technique to improve PAE performances is to drive the gate of the transistor with a quasi-half-sine-wave voltage. To achieve such a gate–source voltage shaping, second harmonic (H2) injection is needed at the gate port. When applied to a class F amplifier, this technique lowers the turn on time $(t_{\rm on})$ of the drain–source current without affecting the square wave drain–source voltage, as reported in [20]. As a consequence, drain voltage and current overlapping is reduced and PAE performances are improved.

A nonlinear model of a 15-W die GaN HEMT from Cree, Durham, NC, has been extracted and harmonic-balance simulations have been performed using ADS software, as illustrated in Fig. 2. Time-domain waveforms plotted in dot lines are obtained when a sine-wave gate–source voltage $Vgs(t)$ is applied (generator at $2f_0$ is turned off). Time-domain waveforms plotted in solid lines are obtained when a quasi-half-sine-wave gate–source voltage is applied (both generators at f_0 and $2f_0$ are turned on). The ratio between the second harmonic and fundamental harmonic components is tuned to approximately 1/7. The phase shift between fundamental and second harmonic components is close to 0°.

The aperture time reduction of the drain–source current and the corresponding dynamic load line modification obtained with half sine gate–source voltage shaping and observable in Fig. 2 illustrates the decrease of the overlap between drain–current and drain–source voltage.

Fig. 3 shows simulated PAE of the class F amplifier versus output power with and without gate–source voltage shaping. PAE enhancement of seven points is expected at high power.

Time-domain voltage and current waveforms, as well as load lines recorded at 41.8-dBm output power are plotted in Figs. 4 and 5. A significant decrease of the turn on time $(t_{\rm on})$ of the drain–current can be clearly observed when a half-sine gate–source voltage waveform is applied.

A driver needed for an appropriate gate–source voltage shaping of power transistor is described in Section III.

III. Two-Stage PA Design

The proposed two-stage amplifier topology is illustrated in Fig. 6.The same HEMT GaN die (CGH60015D from Cree) is used for the driver stage (transistor Q_1) and for the power stage

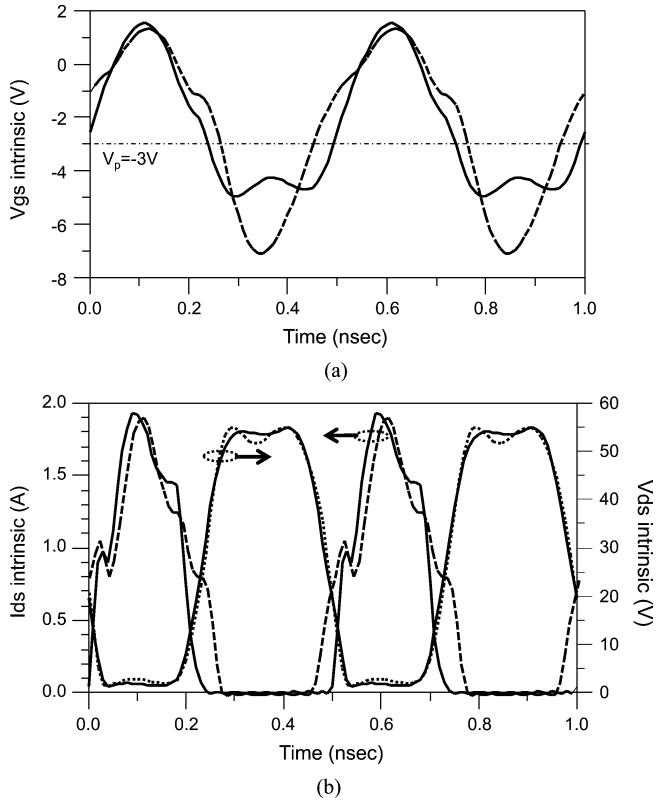

Fig. 4. Simulated voltage and current waveforms [(a) gate–source voltage and (b) drain–current and voltage]: sine shape gate–source voltage (dotted line), half sine shape gate–source voltage (solid line).

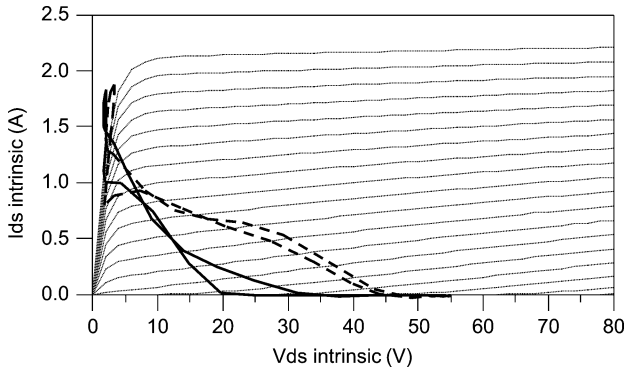

Fig. 5. Simulated load line without (dotted line) and with (solid line) second harmonic injection at the gate port.

(transistor Q_2). Q_1 is biased at $V_{\rm gs0} = -2.5$ V and at a low drain voltage ($V_{\rm ds0} = 7$ V) so that it does not affect the overall amplifier efficiency. Q_2 is biased at $V_{\rm gs0} = -2.3$ V and $V_{\rm ds0} = 28$ V.

Load impedance of Q1 is high impedance at the second harmonic and low impedance (close to a short) at the third harmonic. Transistor Q1 used as a driver stage operates under class F-1 conditions. It produces an output half-sine drain voltage that feeds directly the gate port of the power stage.

Transistor Q2 operates under class F conditions with a proper half-sine shape gate-source voltage to enhance PAE, as explained in Section II. Load impedance of Q2 is low impedance

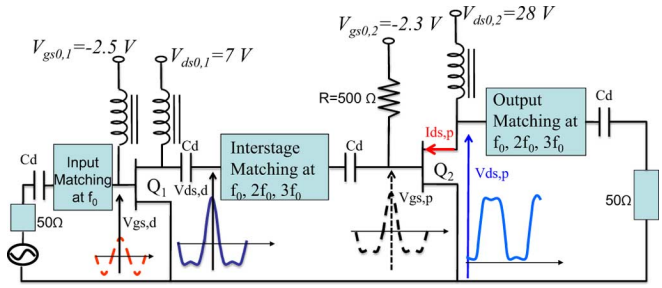

Fig. 6. Two-stage PA principle.

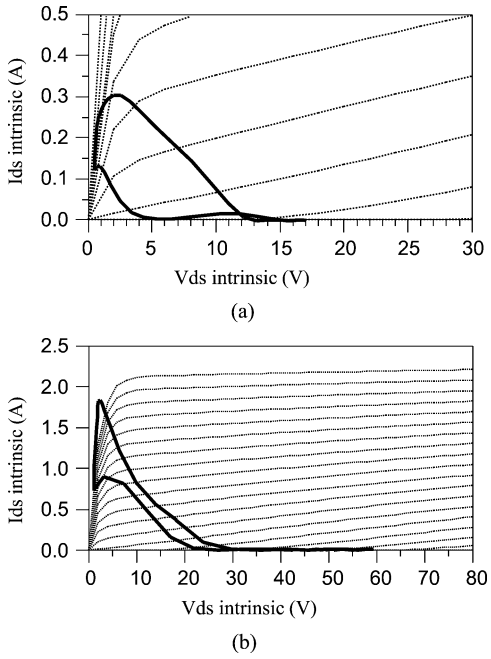

Fig. 7. Simulated intrinsic load line of: (a) Q1 and (b) Q2.

(close to a short) at the second harmonic and high impedance (close to an open) at the third harmonic. Simulated intrinsic dynamic load lines of transistor Q1 and Q2 operating at high level are shown in Fig. 7.

A photograph of the built amplifier is shown in Fig. 8.

Fig. 9 shows the design topology of the inter-stage matching network. The impedance at the third harmonic is shorted by an open stub ($\lambda/12$) connected close to the drain port of Q_1. Z_1, Z_2, Z_3, and the electrical length $\vartheta_{\rm opt}$ are optimized to reach a half-sine waveform at the input of the power stage, and the best load impedance of the driver stage at the fundamental and second harmonic.

The output matching circuit is synthesized to achieve impedance transformation from a 50-Ω load to the suitable optimum impedance at the fundamental, while the second harmonic is terminated into a short by the quarter-wavelength connected close to drain port of power stage. The third harmonic is terminated into an open.

RC networks $(R_{\rm stab1}, C_{\rm stab1}, R_{\rm stab2}, C_{\rm stab2})$, shown in Fig. 10, have been added at the input of the driver stage to ensure stability.

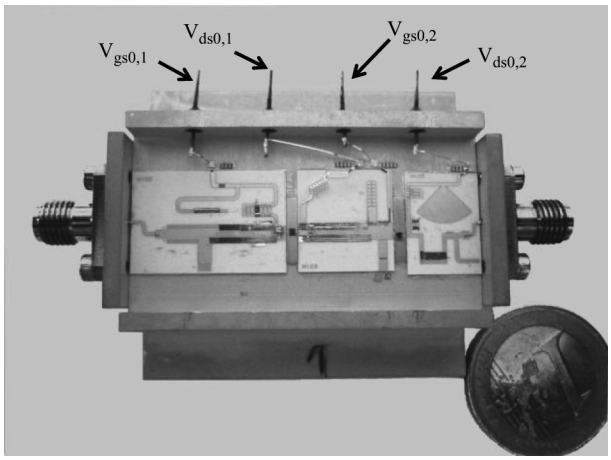

Fig. 8. Photograph of the two-stage amplifier.

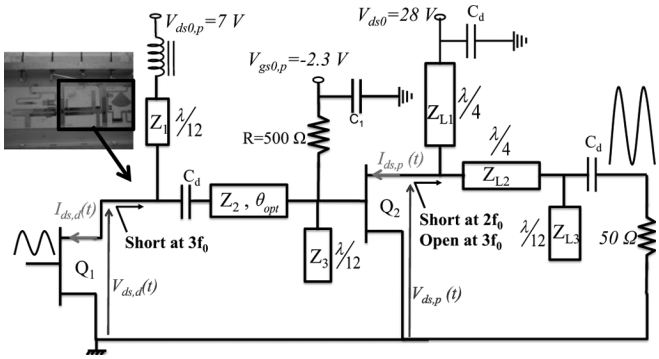

Fig. 9. Inter-stage and output stage design concept.

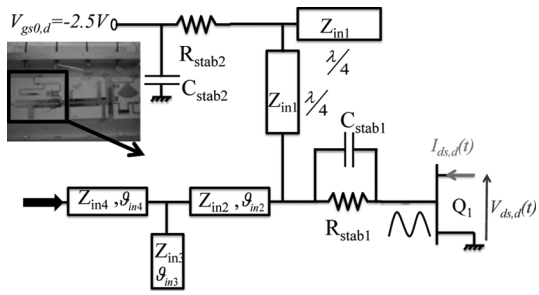

Fig. 10. Input matching network of the driver stage.

IV. Measurement Results

First, conventional input/output power measurements of the built amplifier have been performed. Second, a more in-depth characterization step has been achieved that consists of voltage waveform measurements at internal nodes of the two-stage circuit using an LSNA and high-impedance probes. To demonstrate PAE enhancement provided by our proposed technique, over an enlarged bandwidth, waveform measurements are compared to those measured on a single-stage class F PA. The reference single-stage class F PA shown in Fig. 11 is similar to the power stage of the two-stage PA previously described. The only difference lies in the quarter-wavelength line used either for biasing the gate and having at the input a short-circuit termination at second harmonic.

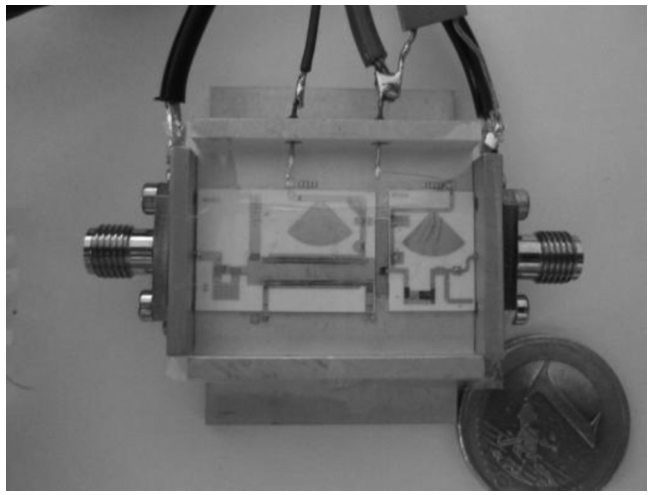

Fig. 11. Photograph of the input/output harmonics-tuned class F PA.

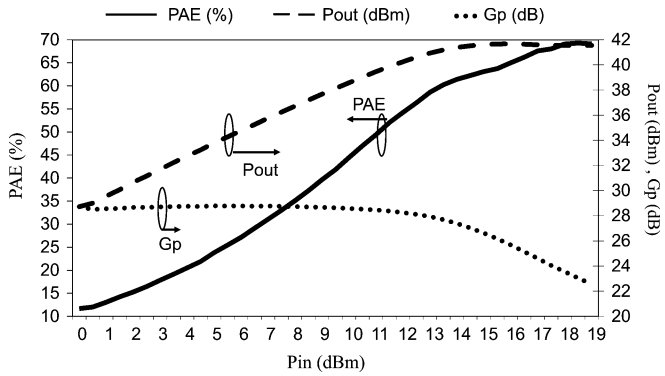

Fig. 12. Measured two-stage amplifier performances versus input power at 2 GHz.

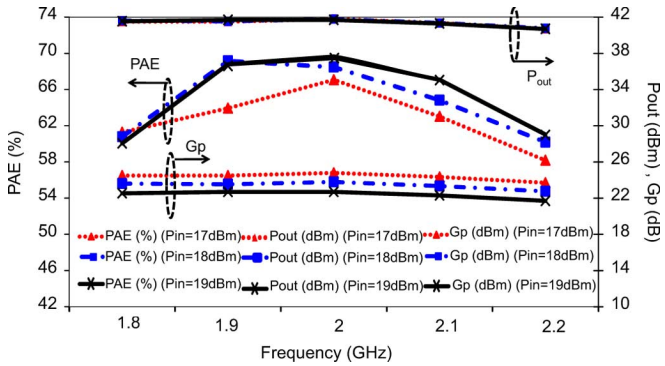

Fig. 13. Measured two-stage amplifier performances versus frequency at 2-, 3-, and 4-dB gain compression.

A. Power Measurements

Output power $(P\mathrm{out})$, PAE, and power gain (Gp) of the two-stage PA measured at 2-GHz center frequency and plotted versus input power $(P\mathrm{in})$ are given in Fig. 12. 28-dB power gain, 41.6-dBm output power, and 70% PAE are obtained. In Fig. 13, output power, PAE, and power gain are plotted versus frequency at 2-, 3-, and 4-dB gain compressions. The PA exhibits a PAE higher than 60% over a 400-MHz bandwidth.

PAE, power gain, and output power of the single-stage PA recorded at 2 GHz are shown in Fig. 14. 66% PAE, 18-dB power

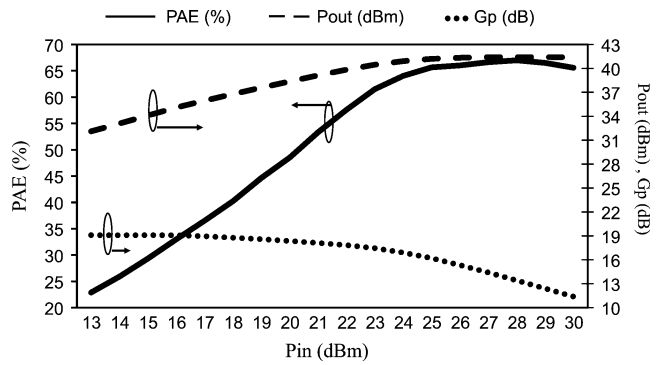

Fig. 14. Measured single-stage class F amplifier performances versus input available power at 2 GHz.

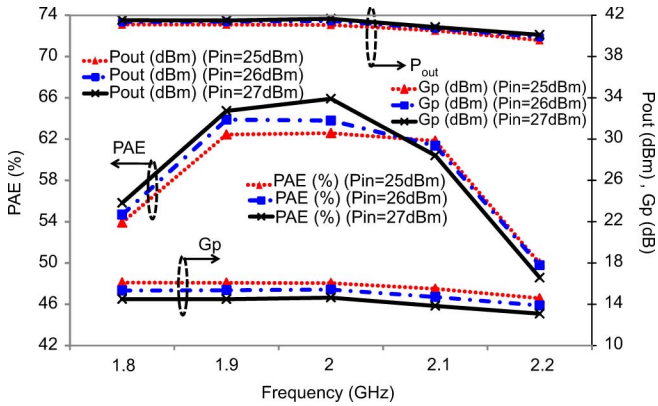

Fig. 15. Measured single-stage class F amplifier performances versus frequency at 2-, 3-, and 4-dB gain compression.

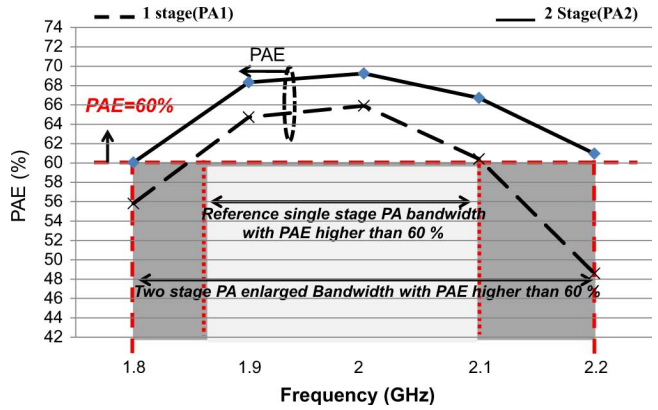

Fig. 16. PAE performances of the two PAs versus frequency at different output power levels.

gain, and 41.6-dBm output power are reached. The same output power as the one provided by the two-stage design is obtained and the PAE is four points lower.

This little difference in terms of PAE can be attributed to little difference in terms of gain compression.

In Fig. 15, output power, PAE, and power gain of single-stage PA are plotted versus frequency at 2-, 3-, and 4-dB gain compressions. It can be observed that the single-stage PA exhibits a PAE higher than 60% on limited bandwidth of 200 MHz.

An interesting aspect, which is the main focus of this paper, can be observed in Fig. 16 where PAE performances of the two

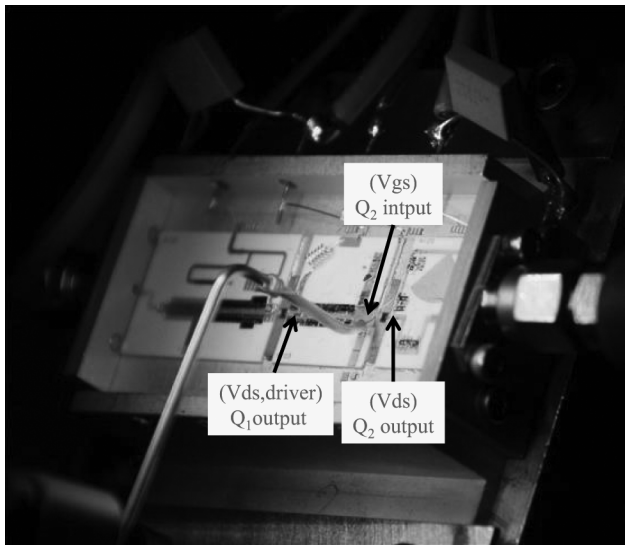

Fig. 17. Built-in amplifier with high impedance probe.

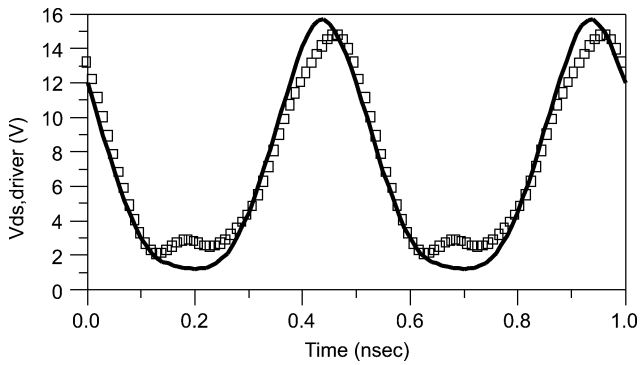

Fig. 18. Drain voltage of the driver stage. Measurement (square), simulation (solid line).

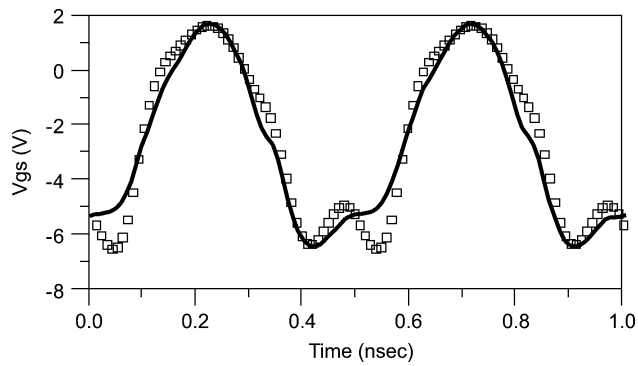

Fig. 19. Gate–source voltage of the power stage. Measurement (square), simulation (solid line).

PAs are plotted versus frequency at about 4-dB gain compression.

The use of a driver stage does not impact the overall PAE of the two-stage PA. It can be observed that the active gate–source voltage-shaping technique reported here offers significant improvement of PAE versus frequency. The frequency bandwidth corresponding to a PAE higher than 60% is augmented by a factor of 2. Time-domain waveforms measured at internal nodes of the PAs are given in the following (Section IV-B).

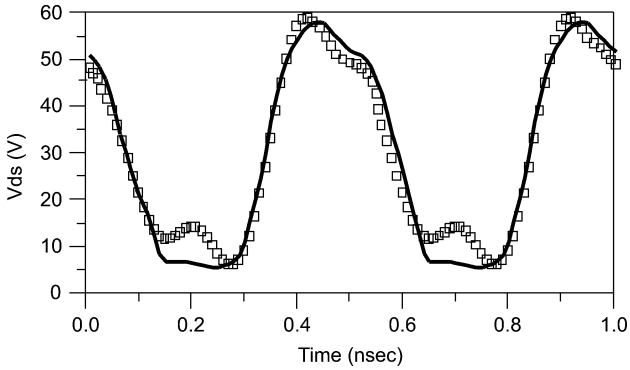

Fig. 20. Drain–source voltage of the power stage. Measurement (square), simulation (solid line).

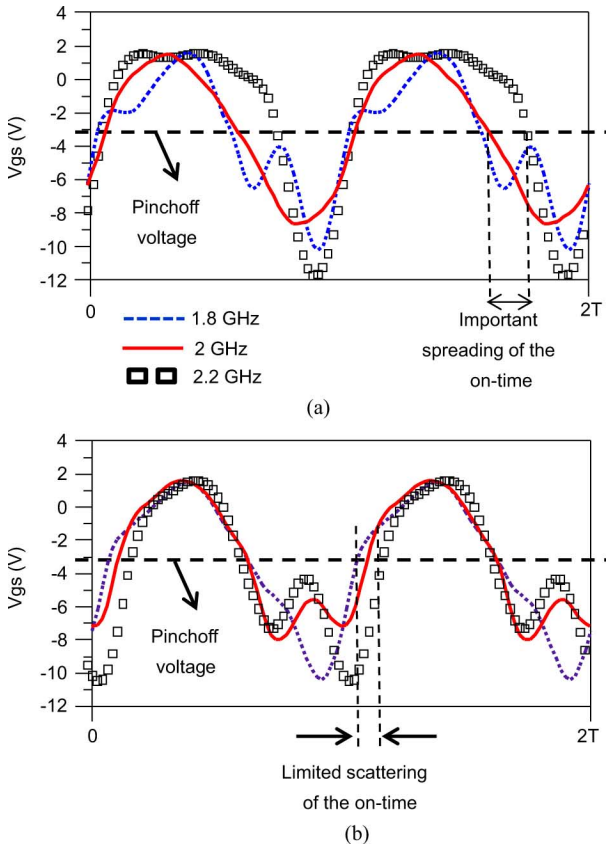

Fig. 21. Gate voltage waveforms measurements (normalize to 2T) at different frequencies (1.8–2.2 GHz). (a) Single-stage amplifier PA1. (b) Power stage of the two-stage PA PA2.

B. Time-Domain Waveform Measurements

Time-domain waveform measurements have been performed by using high-impedance probes (Fine Pitch Microprobes FPM 20× from Cascade Microtech, Beaverton, OR), and an LSNA. Measurement principle and calibration procedure have been already reported in [22]. A photograph of the built-in amplifier and high-impedance probe used for RF voltage measurements is shown in Fig. 17.

1) Waveform Measurements at Center Frequency: Measured drain voltage waveform of the driver stage Q_1 recorded at 41.5-dBm output power and 2-GHz center frequency is plotted in Fig. 18. Such measurements validate the inverse class F operation mode of the driver stage.

Measured gate voltage waveform of the power stage Q_2 recorded at 41.5-dBm output power and 2-GHz center frequency is plotted in Fig. 19. Measurements are in good agreement with simulation results and demonstrate the good gate waveform shaping provided by the proposed inter-stage matching circuit.

Measured drain voltage waveform of the power stage Q_2 recorded at 41.5-dBm output power and 2-GHz center frequency is plotted in Fig. 20. Such measurements validate the class F operation mode of the power stage.

2) Gate–Source Waveform Measurements at Different Frequencies: Gate–source voltage waveforms of the power stage recorded at different frequencies are plotted in Fig. 21. In order to observe the variation of the aperture angle, such voltage waveforms are normalized to two time periods (2T).

Fig. 21(a) corresponds to gate–source voltage waveforms of single-stage PA. Fig. 21(b) corresponds to gate–source voltage waveforms of the power stage of the two-stage PA.

It is shown that good PAE performances versus frequency (previously observable in Fig. 16) are attributed to the fact that there is a limited scattering of the on-time when the operating frequency changes in the case of the two-stage PA reported here compared to the case of the single-stage PA.

V. Conclusion

This paper has presented a two-stage high-efficiency GaN PA. The driver stage operates at saturated level under inverse class F conditions with a low drain bias voltage. The power stage operates under class F conditions and high drain voltage. Such an amplifier addresses constant envelope signal amplification.

The most important aspect reported in this paper concerns the gate–source voltage-shaping technique applied to a class F power stage. An appropriate inter-stage matching circuit has been design to feed the power stage input with a half-sine voltage waveform.

This waveform shaping has been validated by time-domain measurements. Furthermore, it has been demonstrated that this technique enables an enlarged frequency bandwidth at high PAE. In the present case, PAE performances are better than 60% over a 400-MHz bandwidth.

Acknowledgment

The authors wish to acknowledge D. Geffroy, H. Yahi, and C. Baulon, all engineers with Thales Alenia Space, Toulouse, France, for their helpful assistance with fabricating and testing the PAs.

This work was performed in the context of a doctoral thesis with the Department of Nonlinear Microwave Circuit and System, XLIM Laboratory, Limoges University, Limoges, France.

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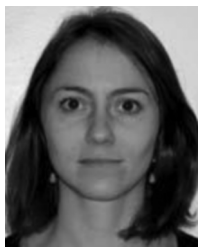

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