Measurements for Optimization of Solid-State Power Amplifiers

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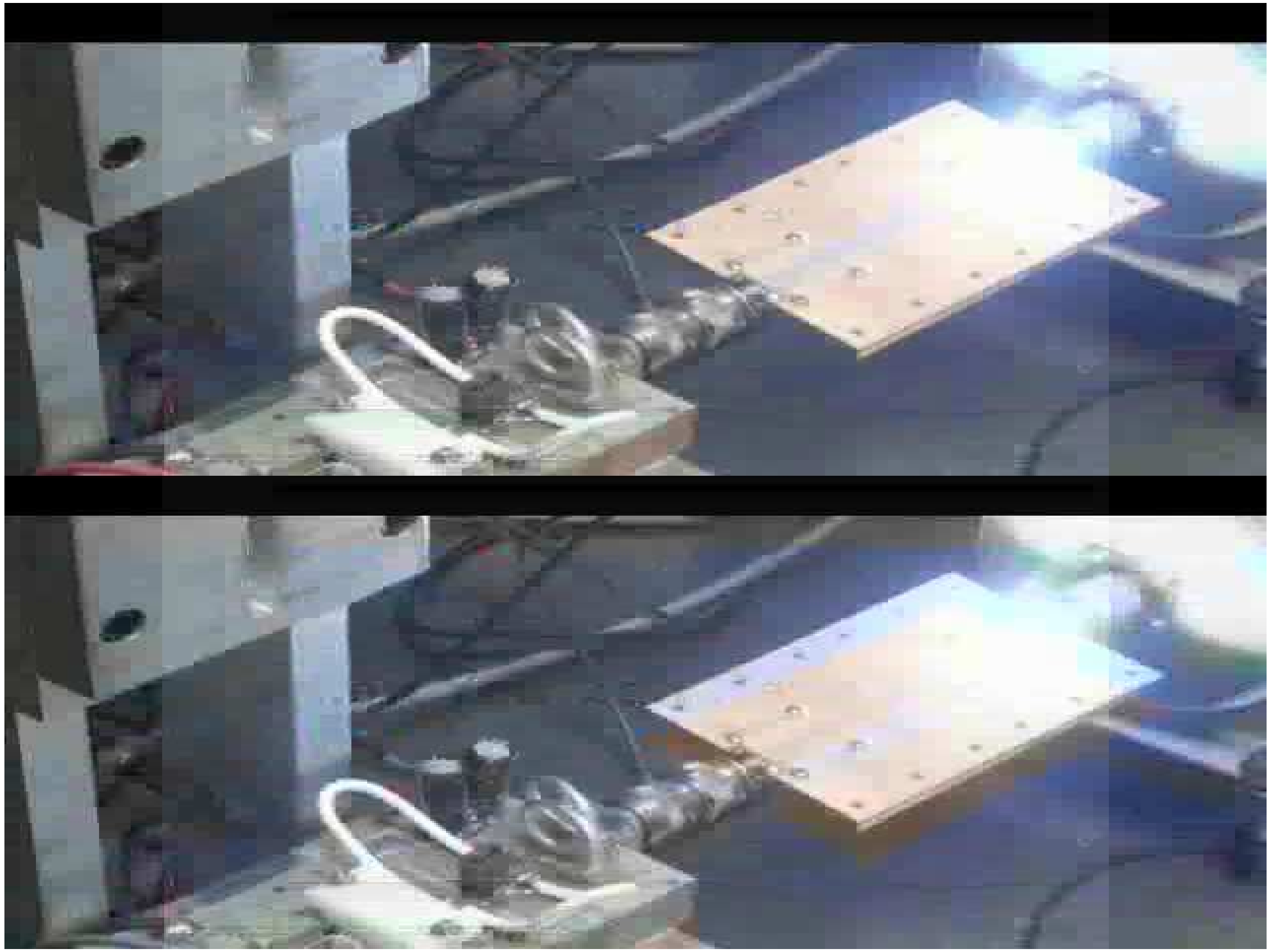
Outline

- Introduction
- Quick overview of classical measurement techniques for NL devices
- Memory effects characterization and modeling
- Waveform engineering based on measurements
- Envelope tracking dynamical biasing / pre-distortion
- High impedance probing
- Conclusion

RF LDMOS – Bias Tee – Transmission line – Mismatched load

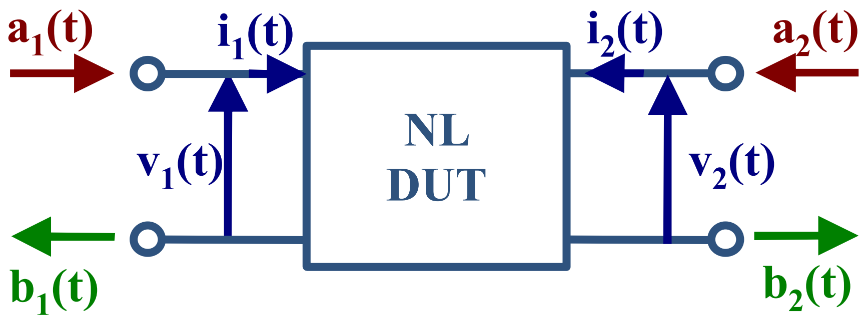


Courtesy of Freescale

☺ This is not exactly what we want, but there is a lot of RF power here!)

Particular case of a nonlinear two-ports device with memory effects

4 instantaneous time-domain variables: I(V) or B(A)



$$\begin{cases} v_i(t) = \sqrt{Z_0}\,[a_i(t) + b_i(t)] \\ i_i(t) = \dfrac{[a_i(t) - b_i(t)]}{\sqrt{Z_0}} \end{cases} \qquad i = (1, 2)$$

- Device commands: incident waves $a_1(t)$, $a_2(t)$

Instantaneous but recent history required

- Device response: reflected waves

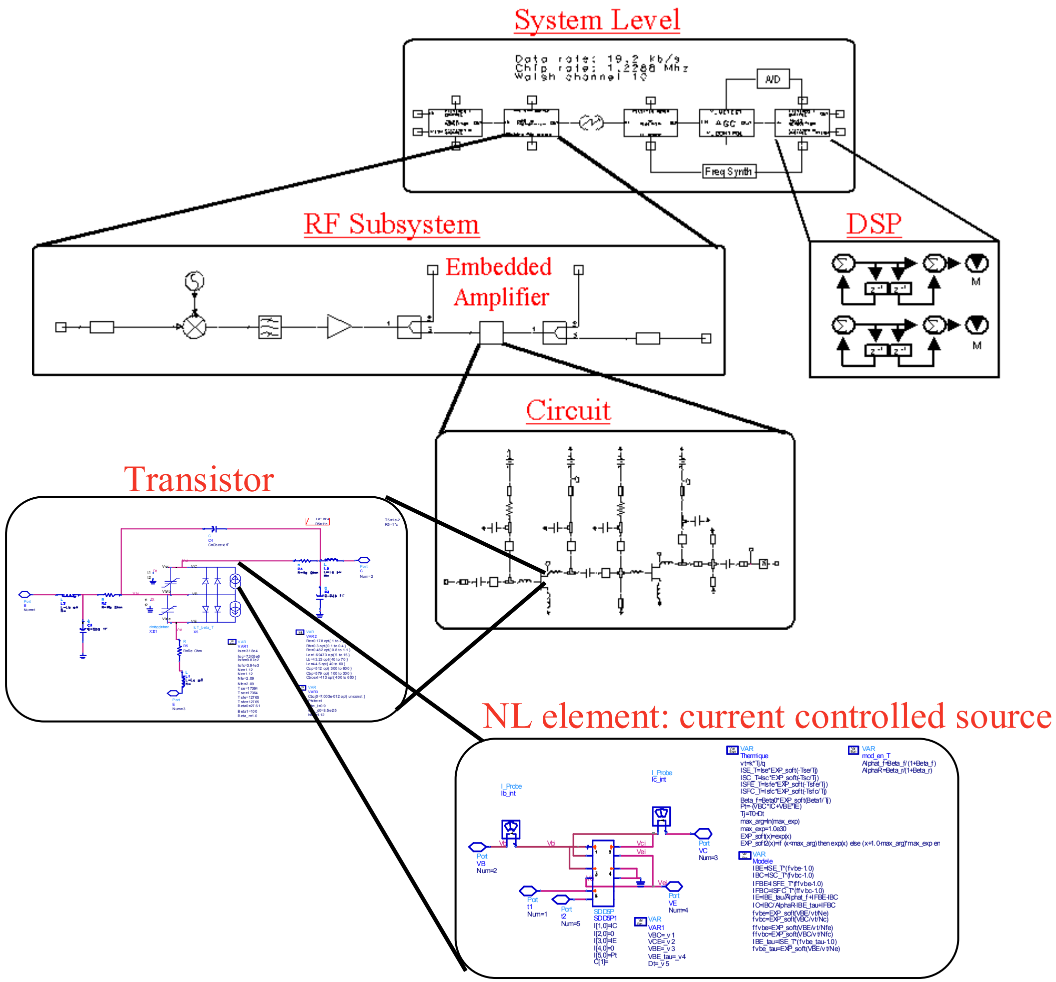
$$\begin{cases} b_1(t) = f_{NL}\,[a_1(t), a_2(t), \mathring{a}_1(t), \mathring{a}_2(t), \dots] \\ b_2(t) = g_{NL}\,[a_1(t), a_2(t), \mathring{a}_1(t), \mathring{a}_2(t), \dots] \end{cases}$$

Large number of terms for LF memory

☹ **Signals with wideband modulations or large peak-to average are distorted**

☺ **These distortions are deterministic, we can compute then (with great efforts!)**

First-pass success of design / foundry process / tests of RF SSPAs



NL Meas. for modeling:
- Transistor Model
- Physical phenomena models
- Memory effects

NL Meas. for design:
- Wideband modulated signals
- Waveform engineering
- Envelope tracking data
- Pre-distortion data

NL Meas. for verification/debug:
- Specifications
- Performances
- Reliability
- High Impedance probing

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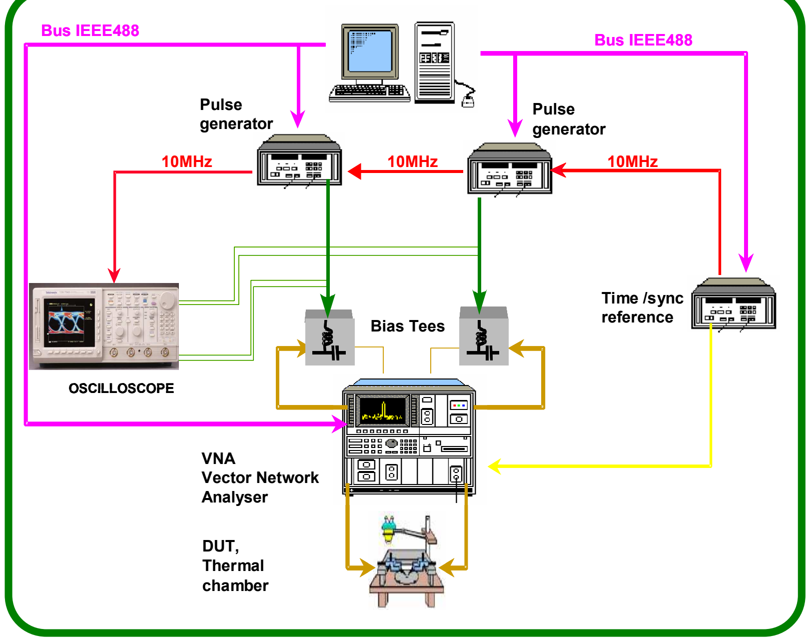
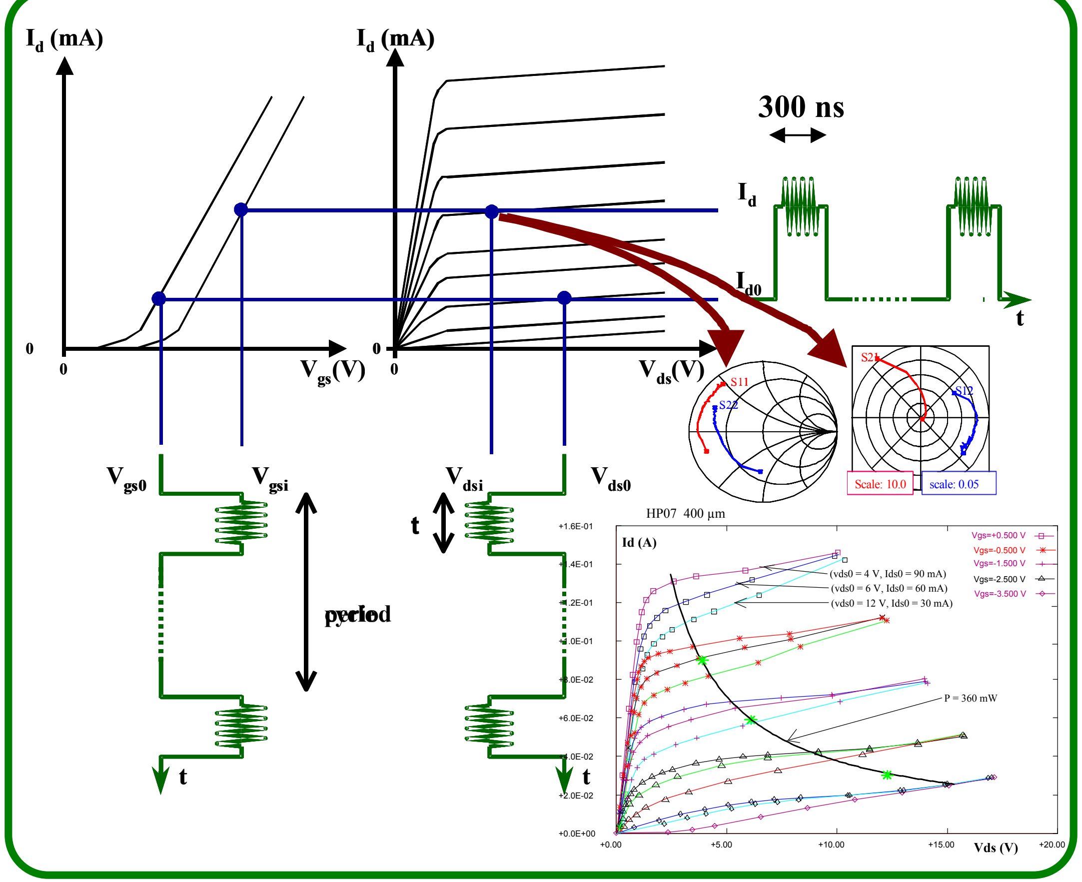
Motivation for short pulses : Control of the device self-heating





Pulsed S-Parameter meas:
- linear elements
- nonlinear C(V)elements
- equivalent scheme model

Pulsed I(V) meas:
- I(V) characteristics
- Thermal characterization
- Trapping effects

☹ **Fast behavior of GaN devices (thermal, traps): ultra short pulses <50ns required**

Pulsed I(V) integrated systems available today

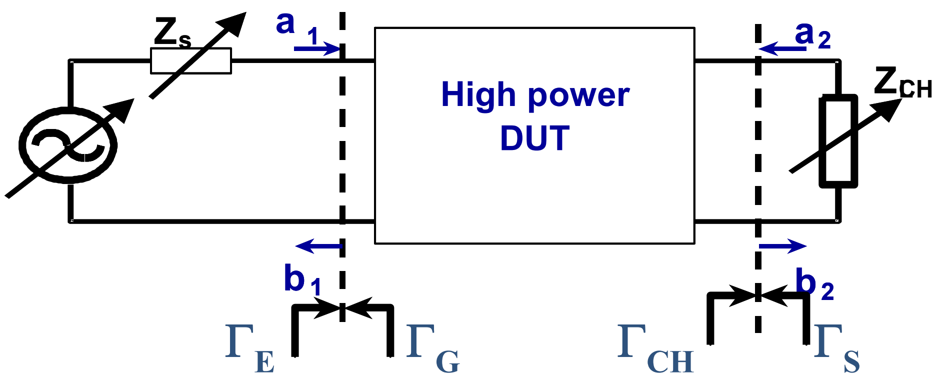
- Auriga/Diva AU4550
- Keithley 4200 SCS
- Agilent B1500A
- Amcad IVCad-PIV
- Focus Microwaves PIV



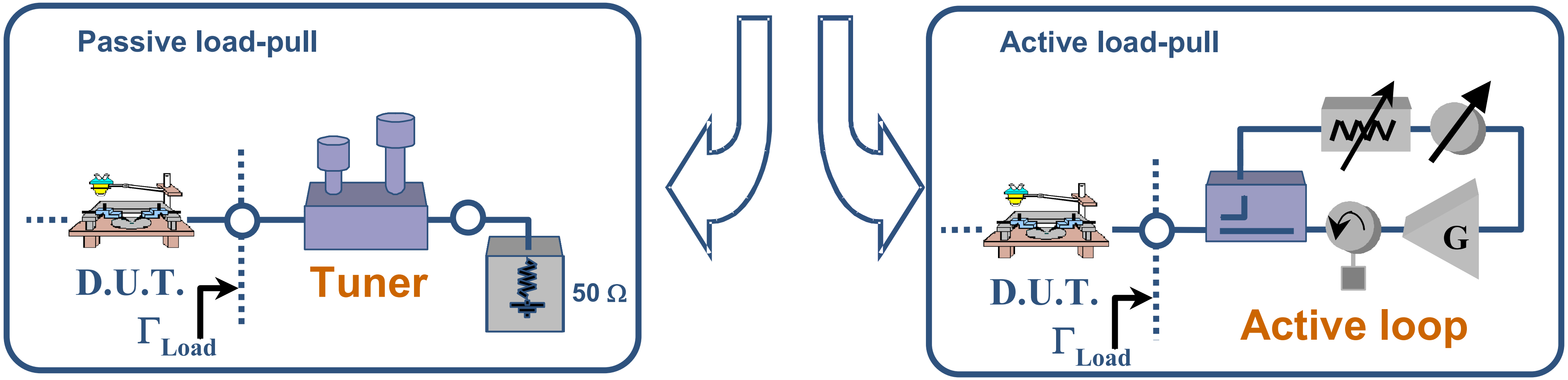


Load-Pull and Source-Pull setups

Measurement of highly mismatched power devices with large signals



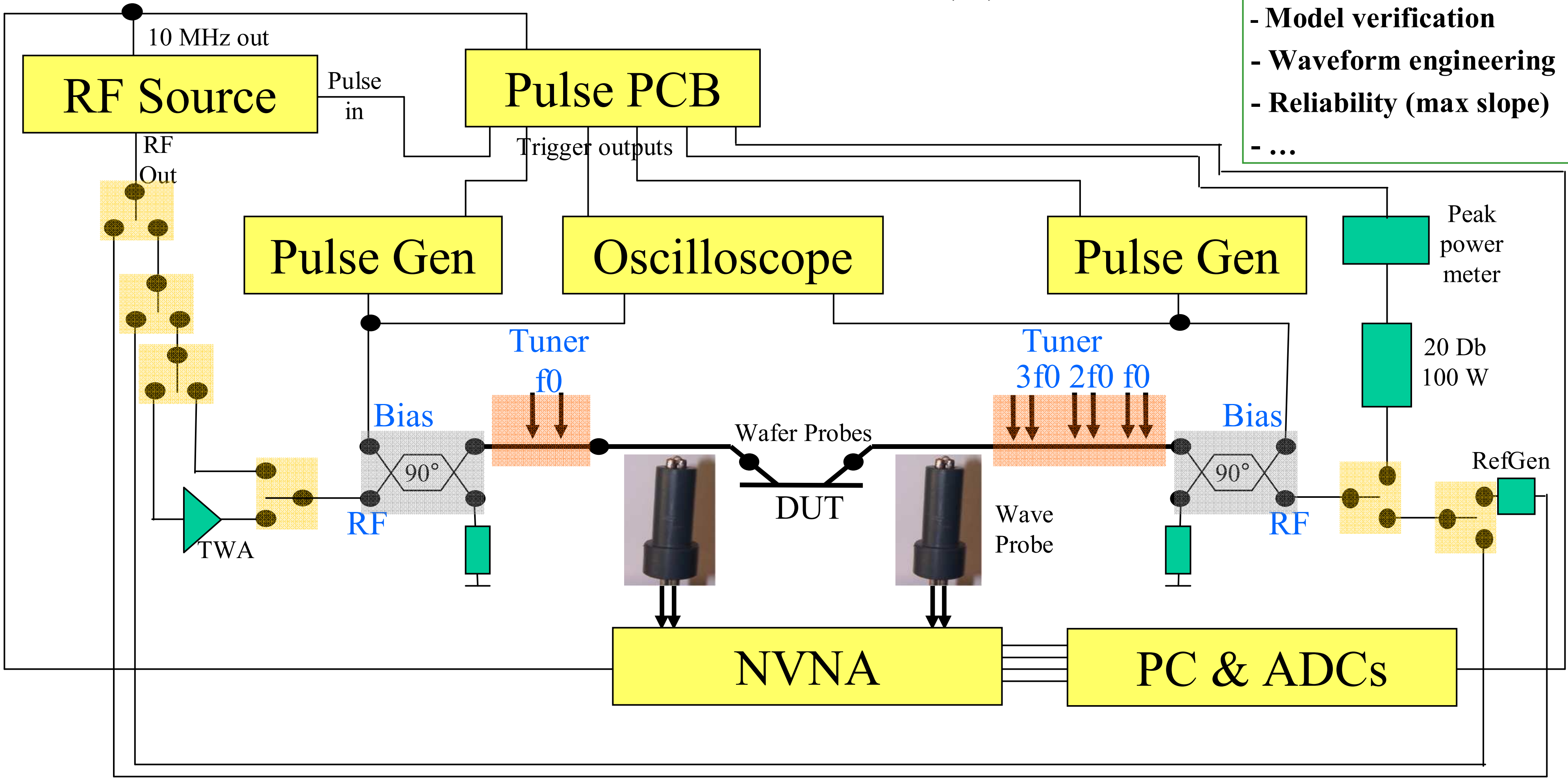
- Optimum impedances for:
  - Output power
  - PAE Max PAE
  - Gain
- Device performances
  - C/I3
  - …



☺ Possible improvements: pulsed or modulated signals, handling of harmonic frequencies

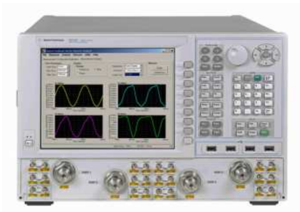
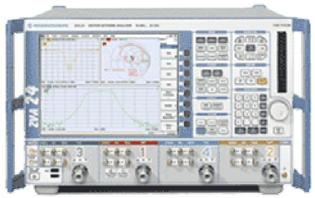
Direct access to source and drain time domain I(V) waveforms

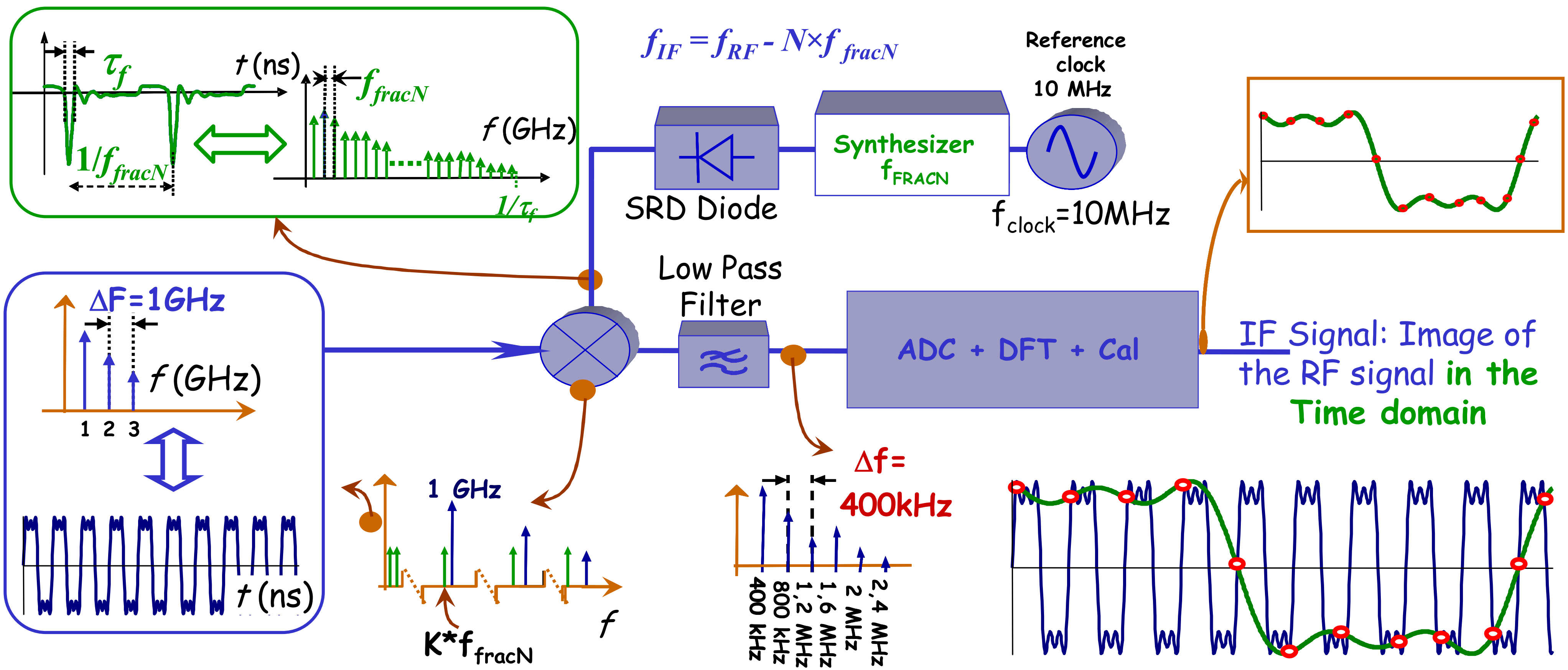
Deep investigations
- **Model verification**
- **Waveform engineering**
- **Reliability (max slope)**
- **…**

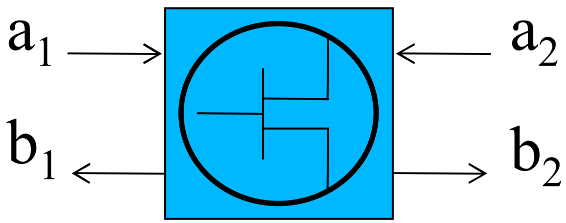


☺ **Special features: Wave probes, NVNA receiver, multi-harmonic tuning, hybrid bias tees**

NVNA (NonLinear Vector Network Analyzer) hardware available today

RF heads / Donwconversion	Mixer-based	Sampler-based
Frequency by frequency acquisition (needs a phase reference gen.)	 Agilent NVNA  R&S ZVA+ NMDG	 Anritsu VectorStar + HFE
One-shot acquisition of all frequencies (a sampler as phase reference)	Impossible	 VTD SWAP X402 (formerly the MTA, the LSNA)



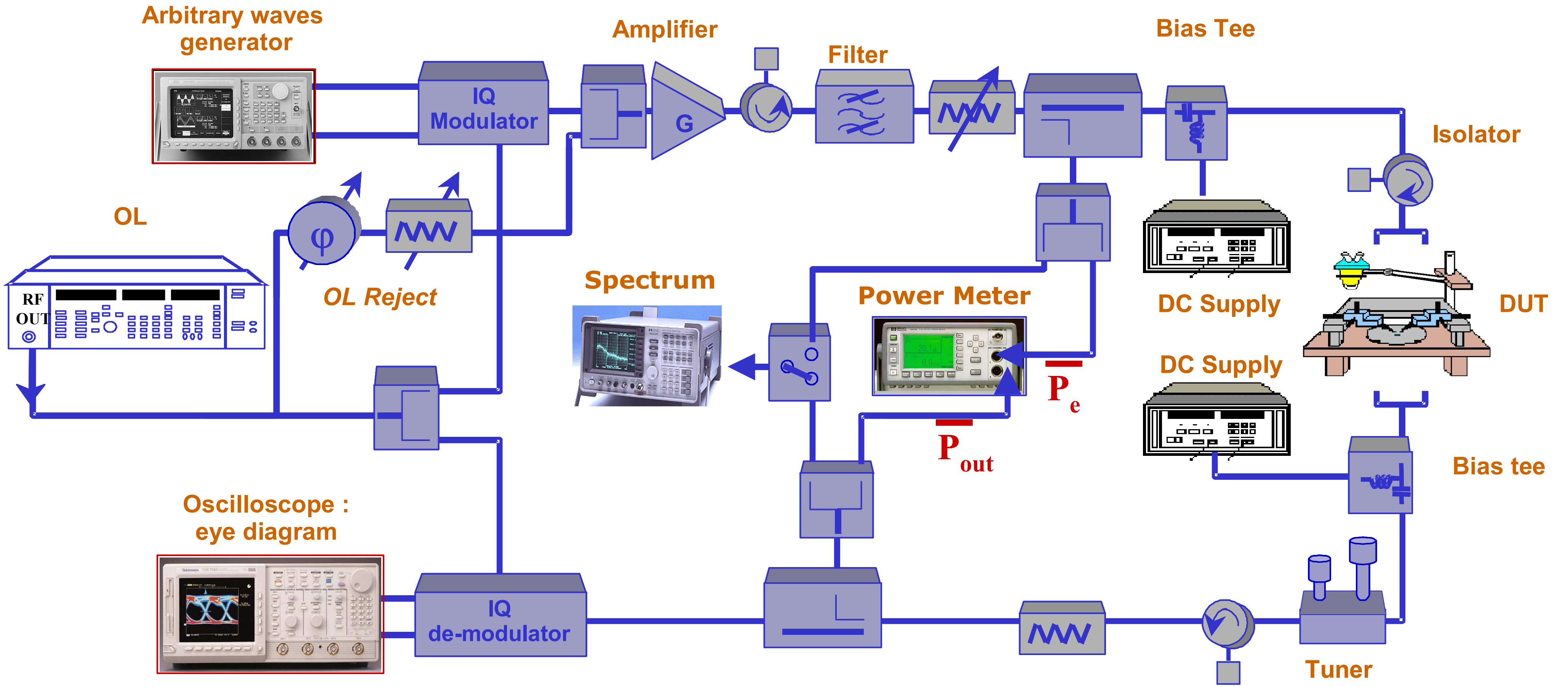


A NVNA features 4 identical channels

(6 are possible for special needs like frequency conversion devices)

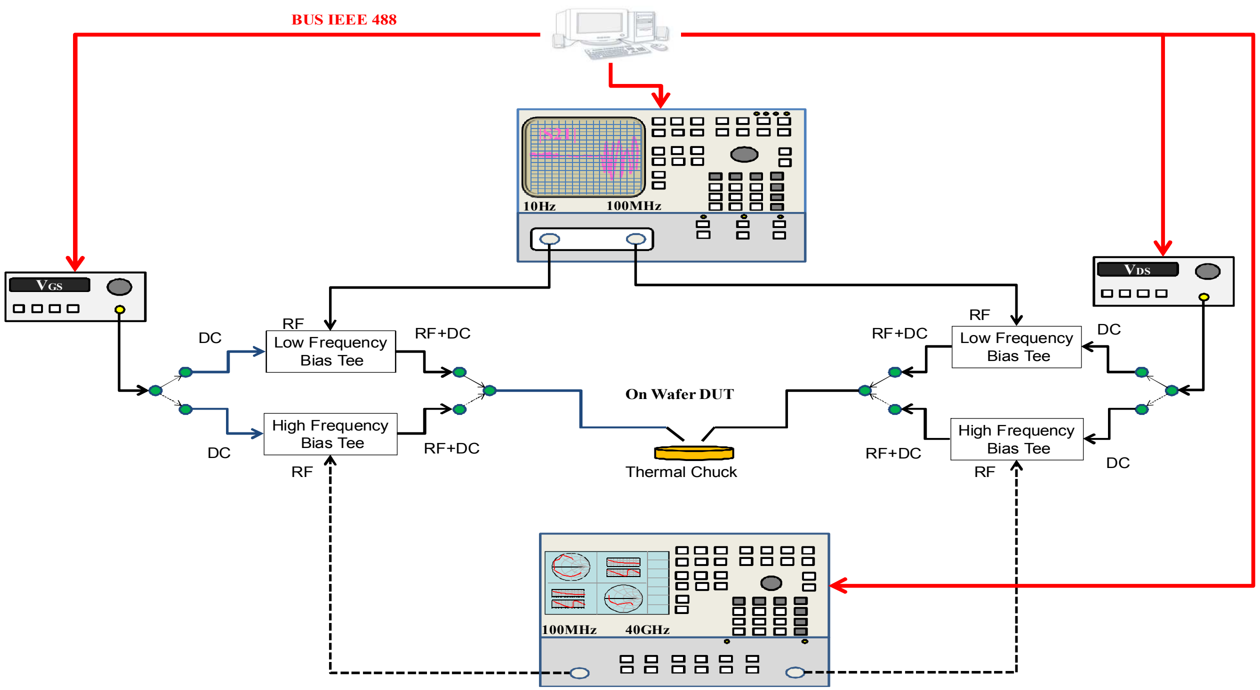
The sampler technique allows extreme pulse mode (50ns, 0.01%)

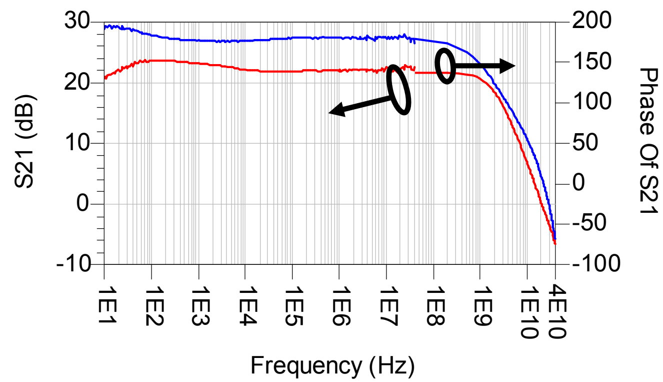
NonLinear behavior of RF power amplifiers when a modulated signal is applied

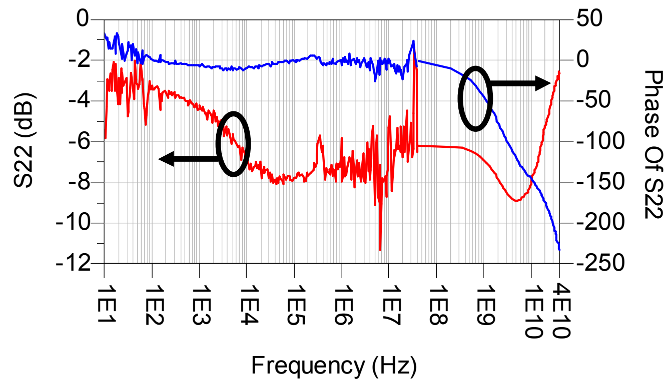


☹ **Needs a specific and complex calibration procedure**

Measurements from 10 Hz to 40 GHz

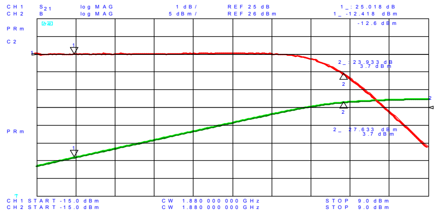




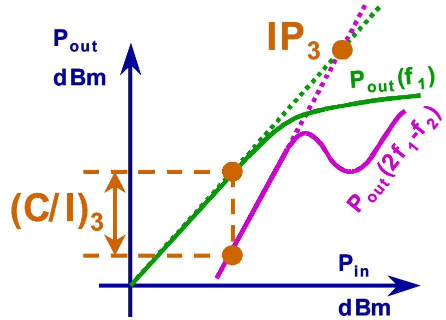


Special low frequency bias tees have been designed

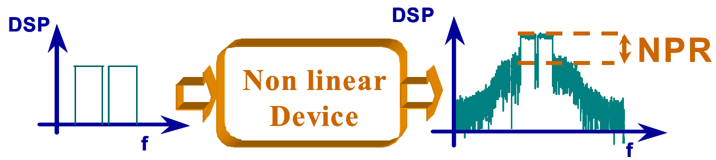
- **Simple RF test signals :**
  - one-tone (CW) : ⇨ S-parameters, AM/AM and AM/PM, constant envelope
    Waveform distortion, compression



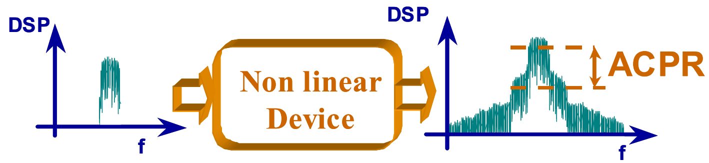
  - 2-tones, 3 tones : ⇨ Intermodulation C/I, IP, LF memory, variable envelope, peak to average
    Envelope distortion



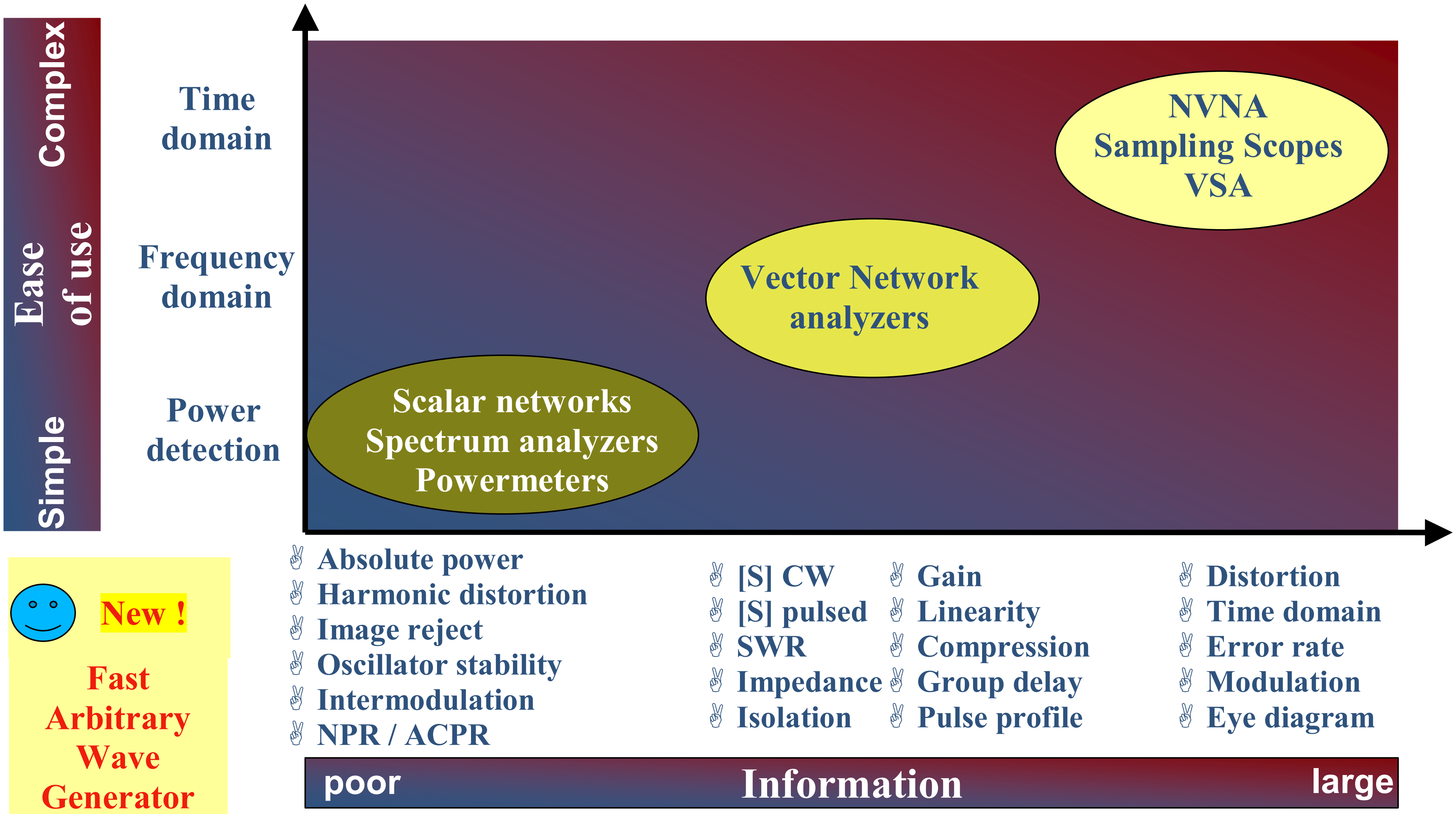
- **Complex RF test signals :**
  - Multitone signals : ⇨ Noise Power Ratio
    Signal distortion



  - Modulated carrier : ⇨ Adjacent Channel Power Ratio



Dynamical behavior of NonLinearities


Complex
Ease of use
Simple
Time domain
Frequency domain
Power detection
NVNA
Sampling Scopes
VSA
Vector Network analyzers
Scalar networks
Spectrum analyzers
Powermeters
Absolute power
Harmonic distortion
Image reject
Oscillator stability
Intermodulation
NPR / ACPR
[S] CW
[S] pulsed
SWR
Impedance
Isolation
Gain
Linearity
Compression
Group delay
Pulse profile
Distortion
Time domain
Error rate
Modulation
Eye diagram
poor
Information
large
New !
Fast Arbitrary Wave Generator

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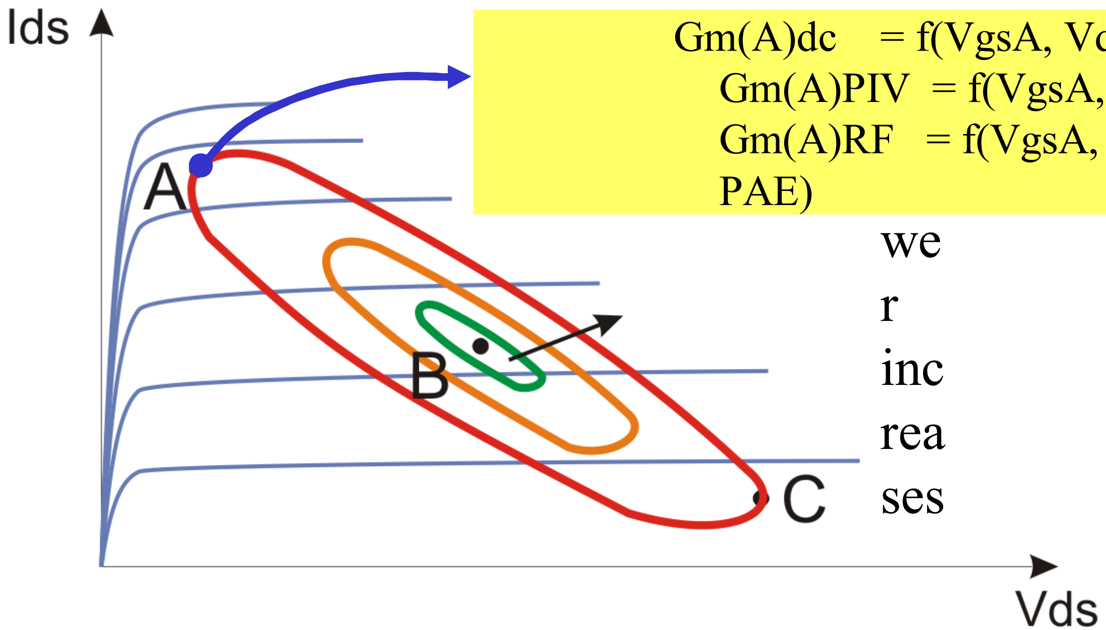
Gm at point A versus measurement conditions



Gm(A)dc = f(VgsA, VdsA, TrapsA, TA)
Gm(A)PIV = f(VgsA, VdsA, TrapsB, TB)
Gm(A)RF = f(VgsA, VdsA, TrapsC, TB & PAE)

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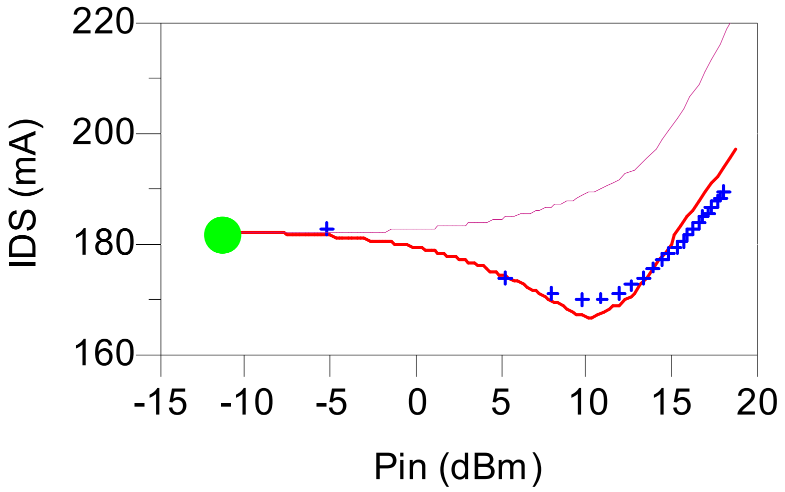
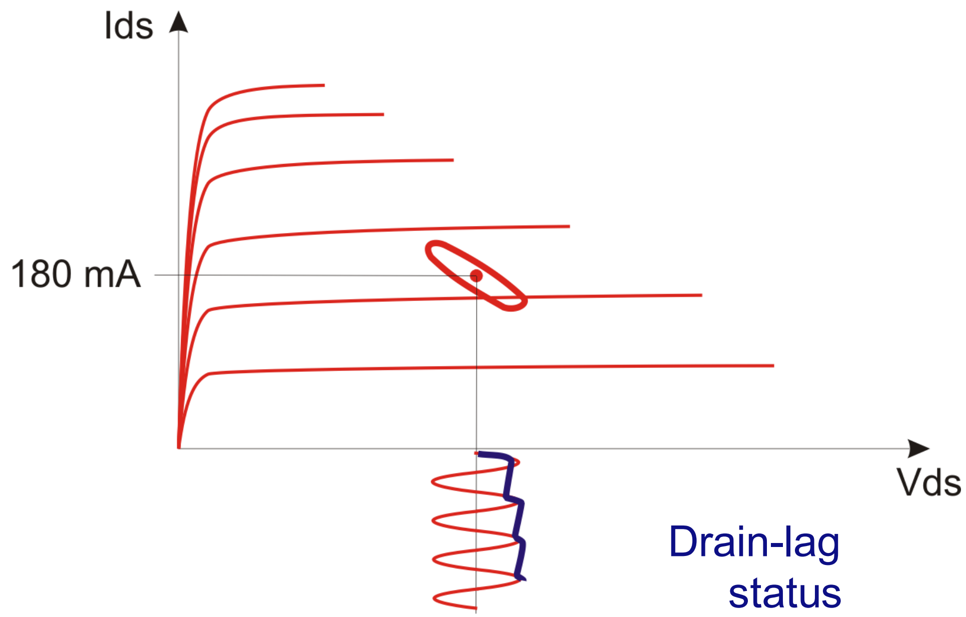
We get 3 very different values of Gm. Y21 ≠ dID/dVDS

Consequences of low frequency memory effects on drain current

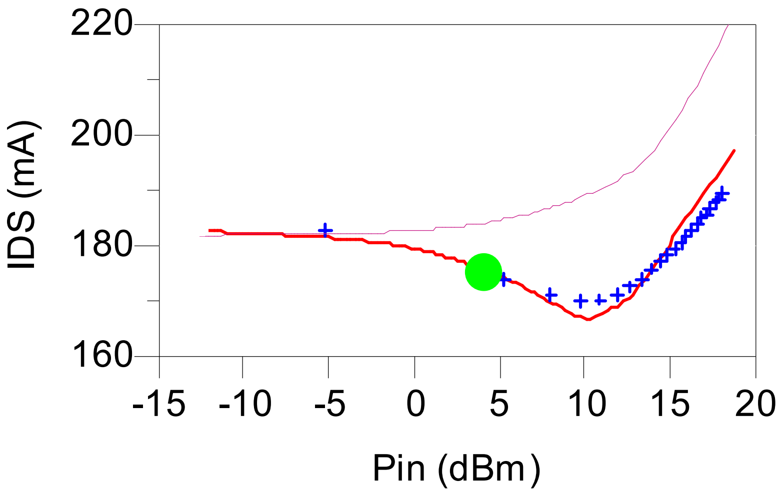
(thermal effect and trapping effects)

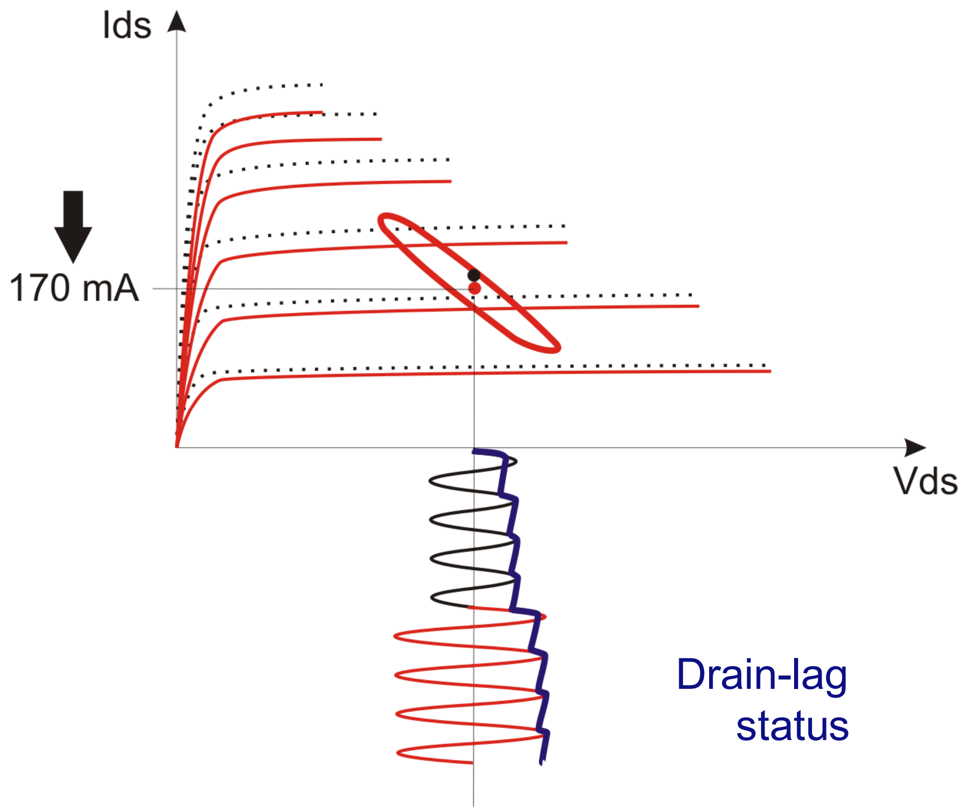
Bias current versus input power (1/4)



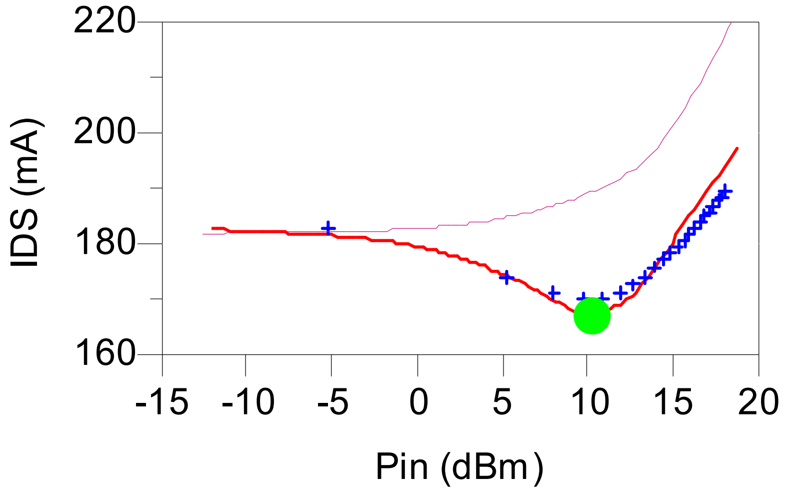


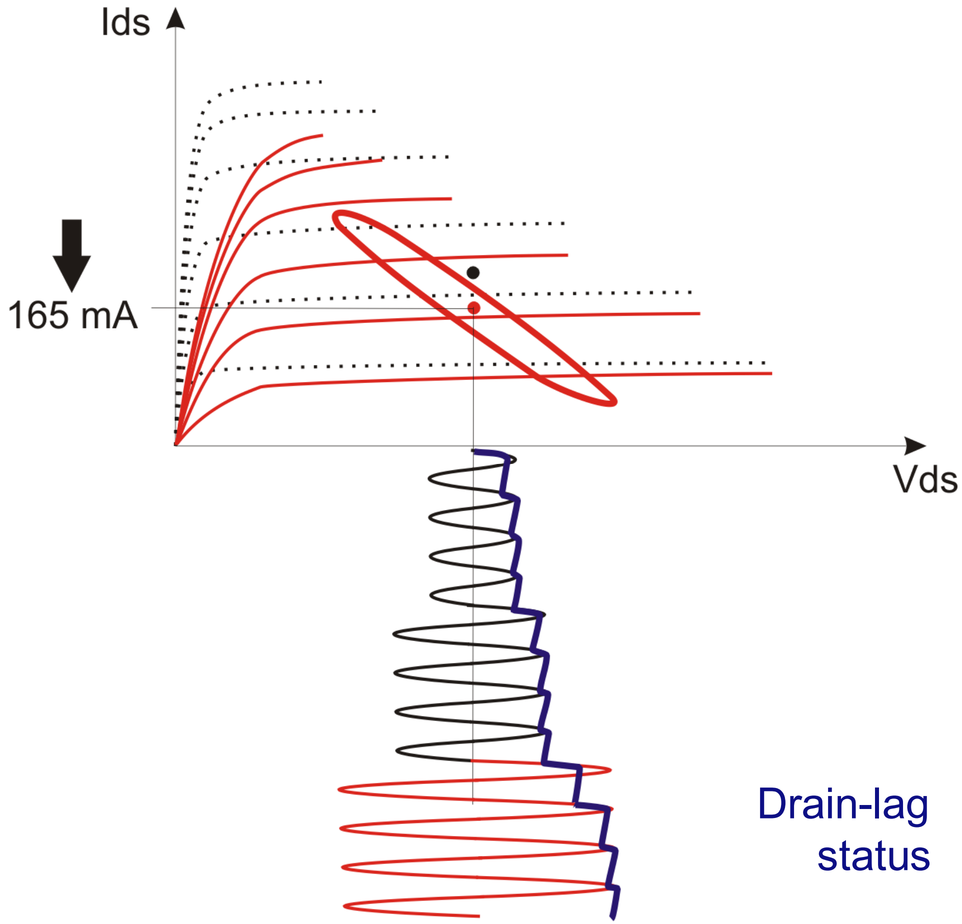
Bias current versus input power (2/4)



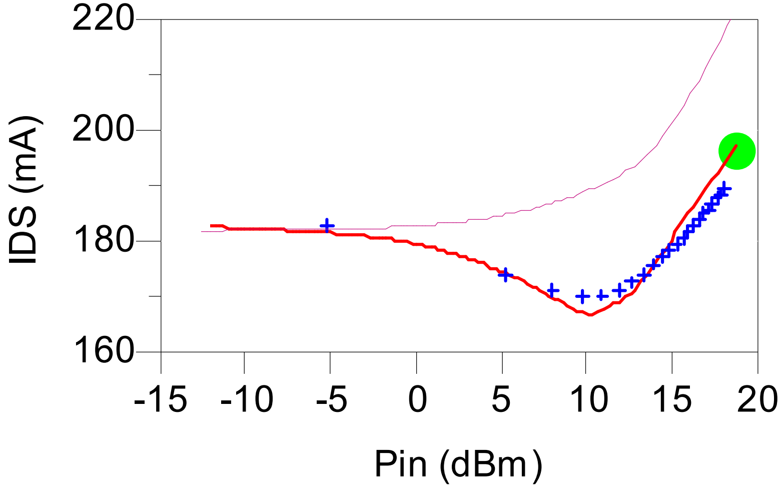


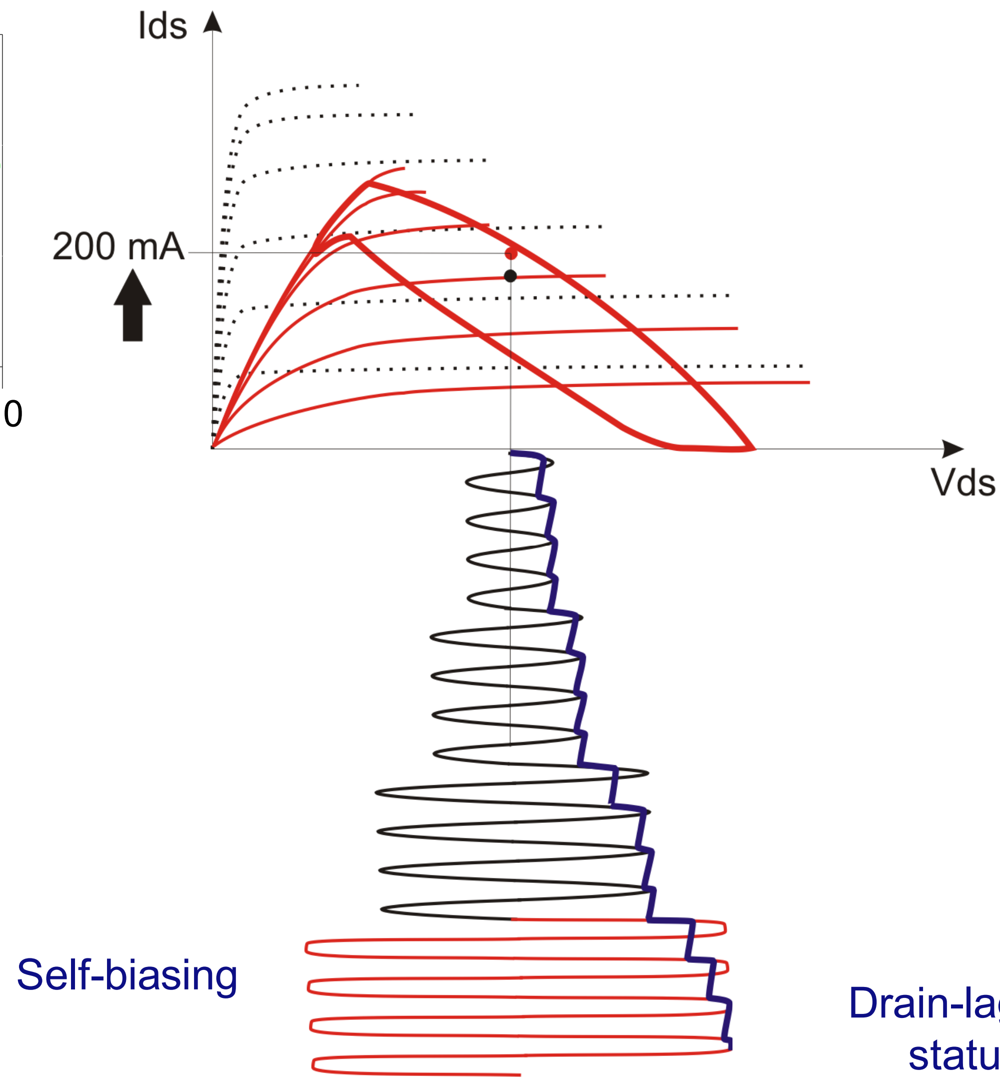
Bias current versus input power (3/4)





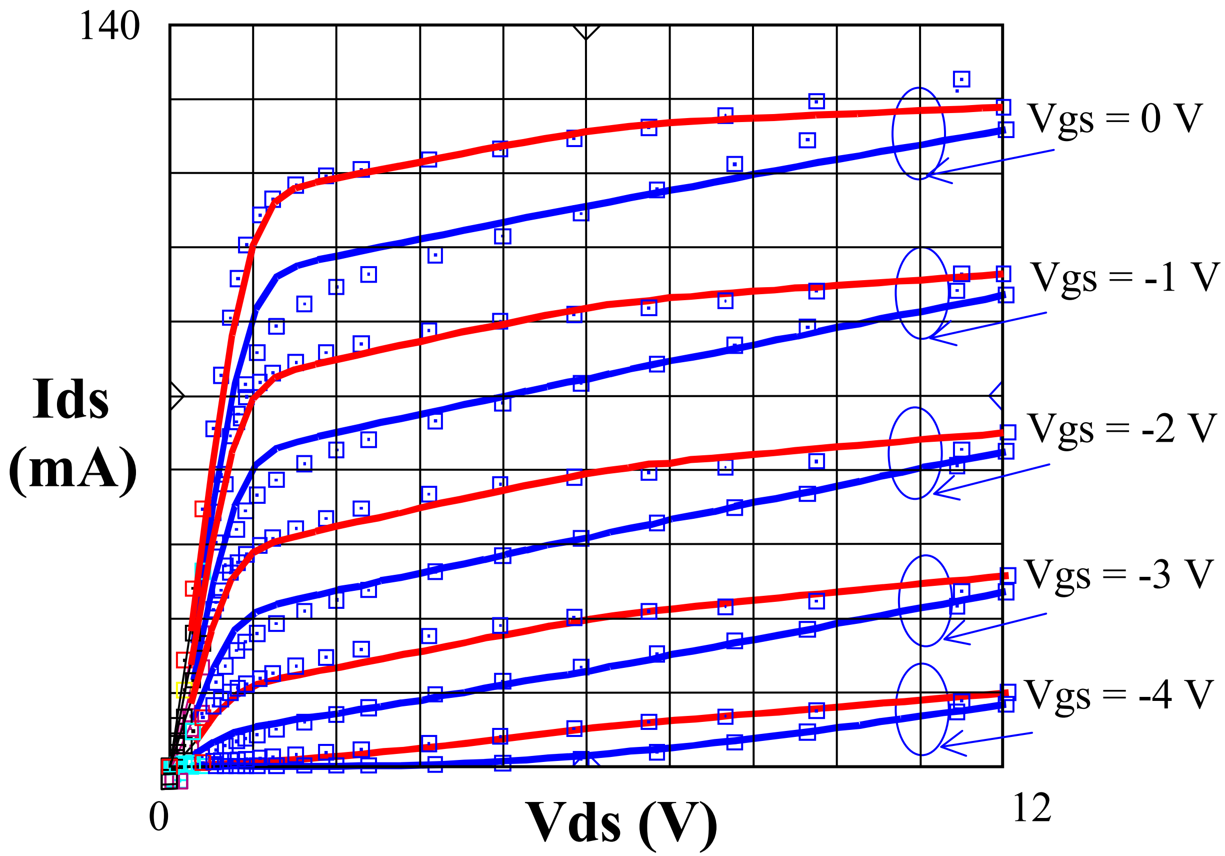
Bias current versus input power (4/4)





The drain-lag traps are filled by VDS maximum value, even at RF frequencies

Effect of PIV DC point on I(V) characteristics



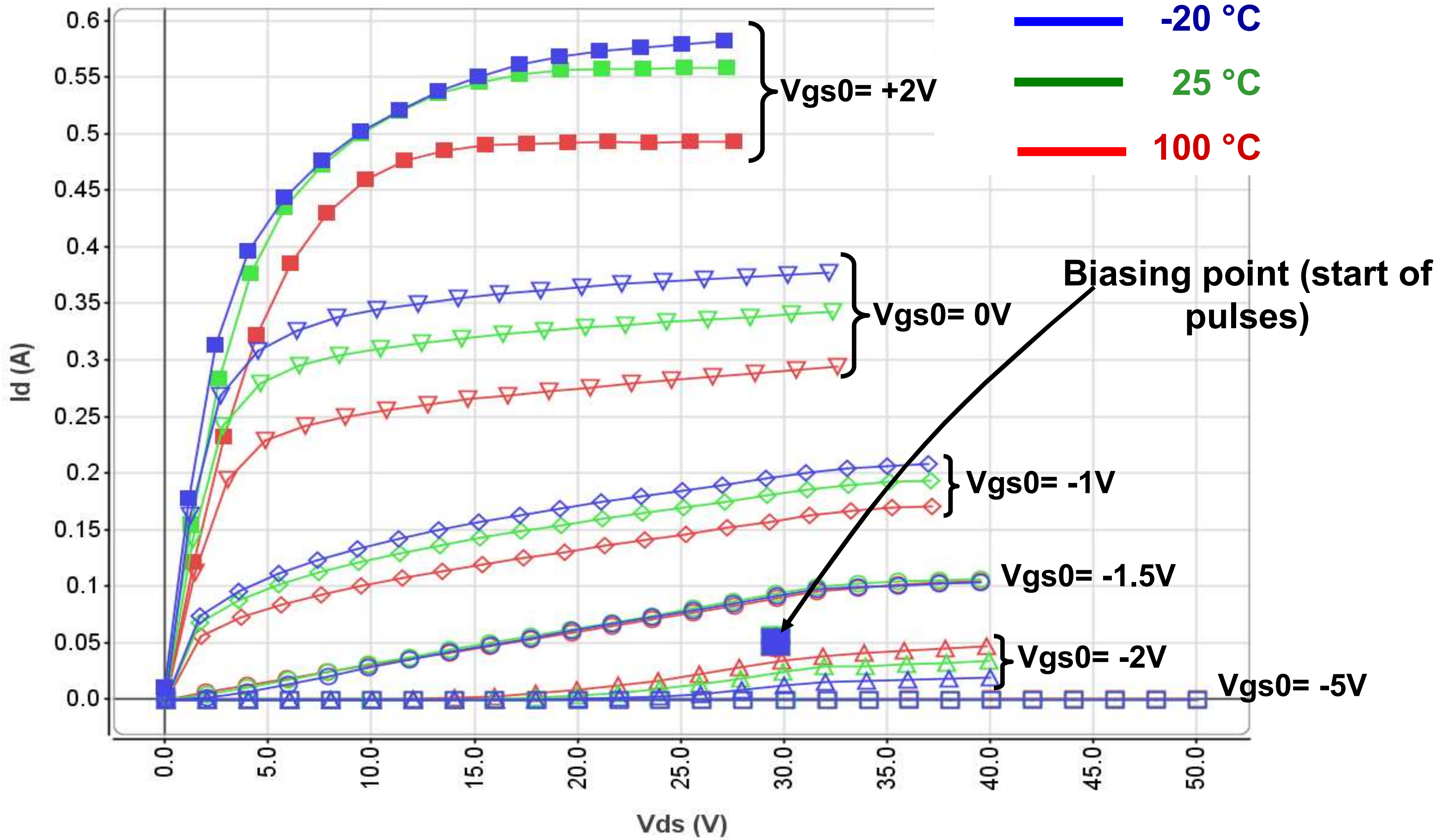
Vds0 = 12V
Ids0 = 30 mA

Vds0 = 4V
Ids0 = 90 mA

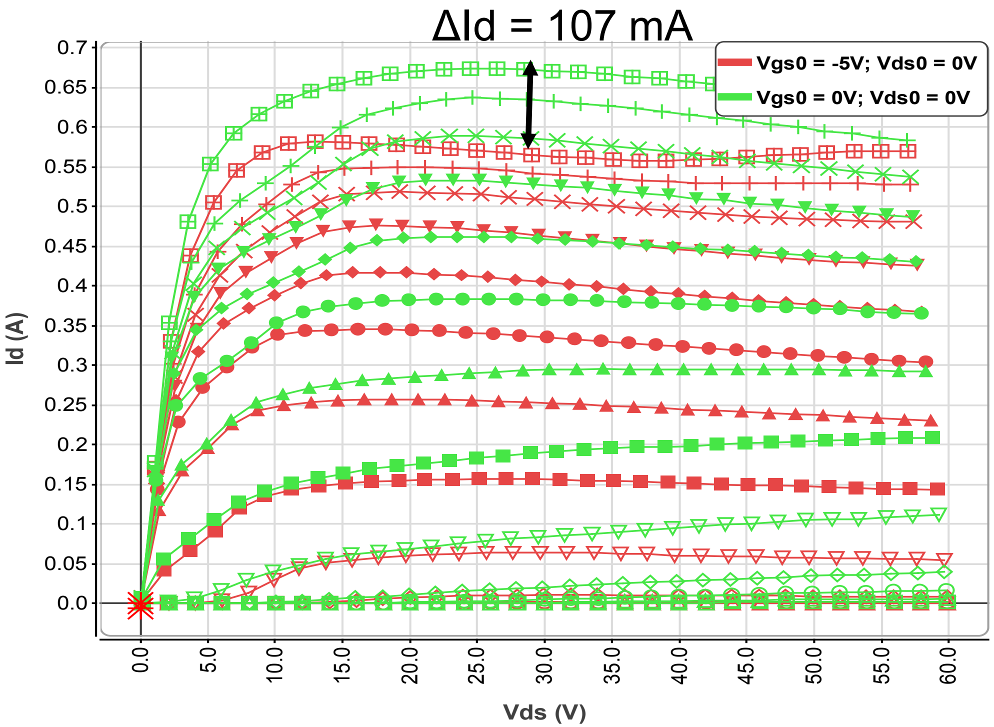
The device temperature is identical, thus the discrepancy is due to drain lag effects

The PIV measurements put in evidence trapping memory effects

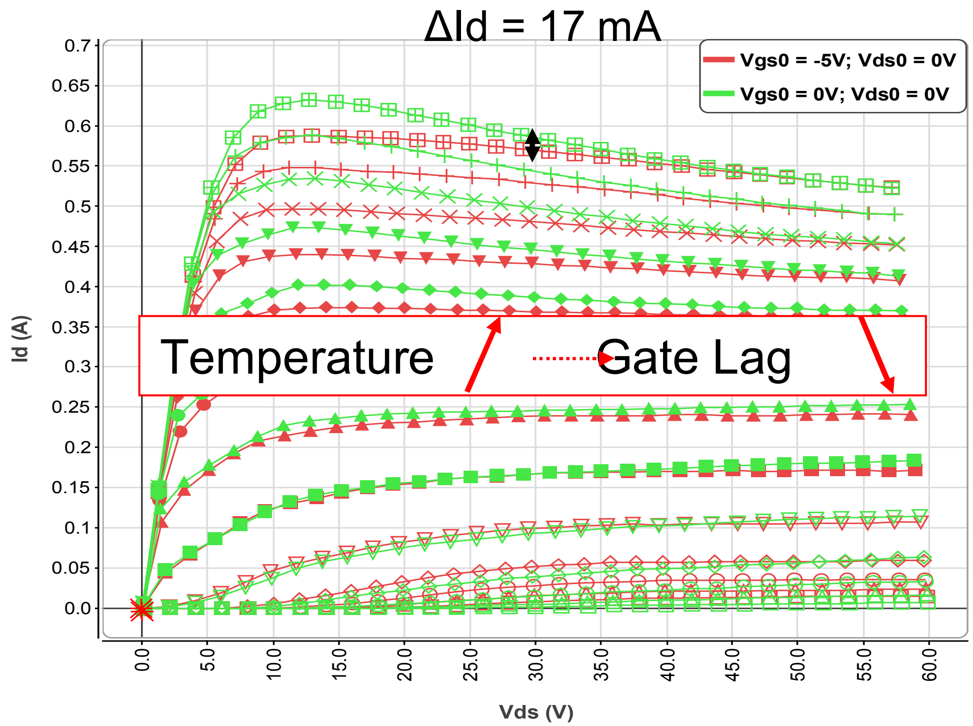
GaN 8x75 µm, Pulses 700ns, Period 1ms, hot biasing point



GaN 8x75 µm, Pulses 700ns, Period 10 µs, cold VDS0=0 biasing point



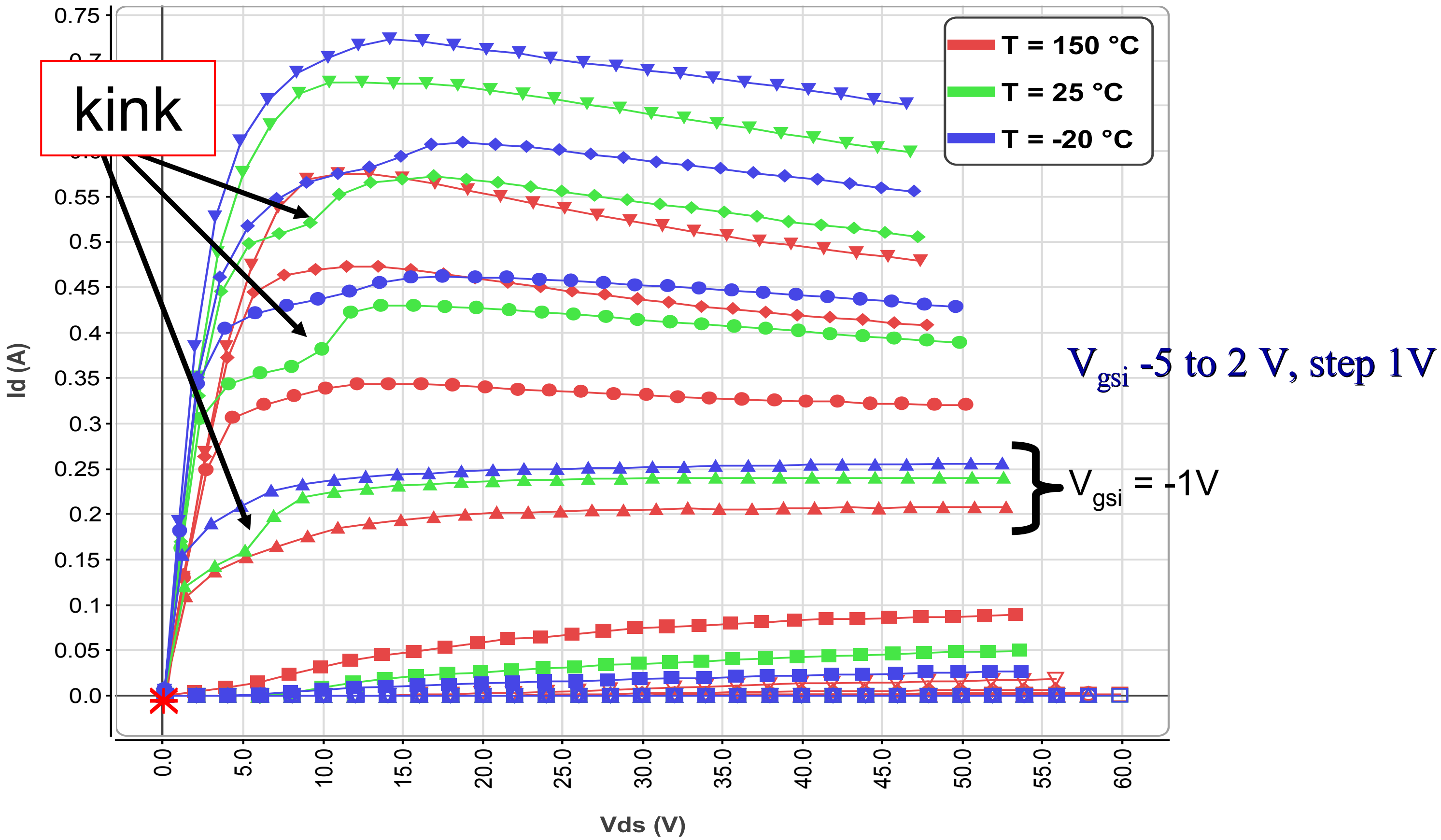
Room Temperature 0 °C



Room Temperature 100 °C

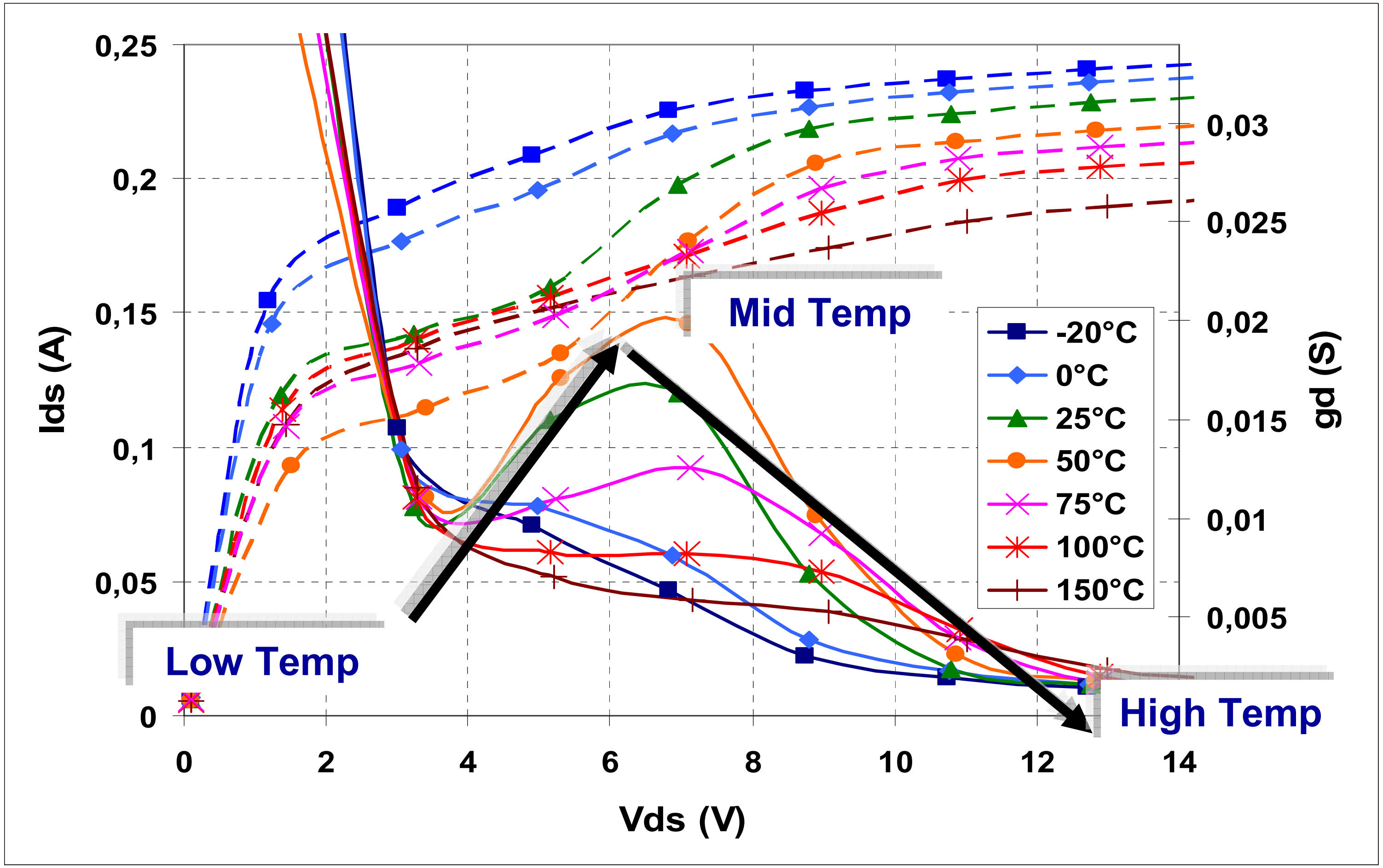
Trap capture and emission time constants are varying versus temperature: Arrhenius

GaN 8x75 µm, Pulses 700ns, Period 10 µs, cold VDS0=0, VGS0=0 biasing point



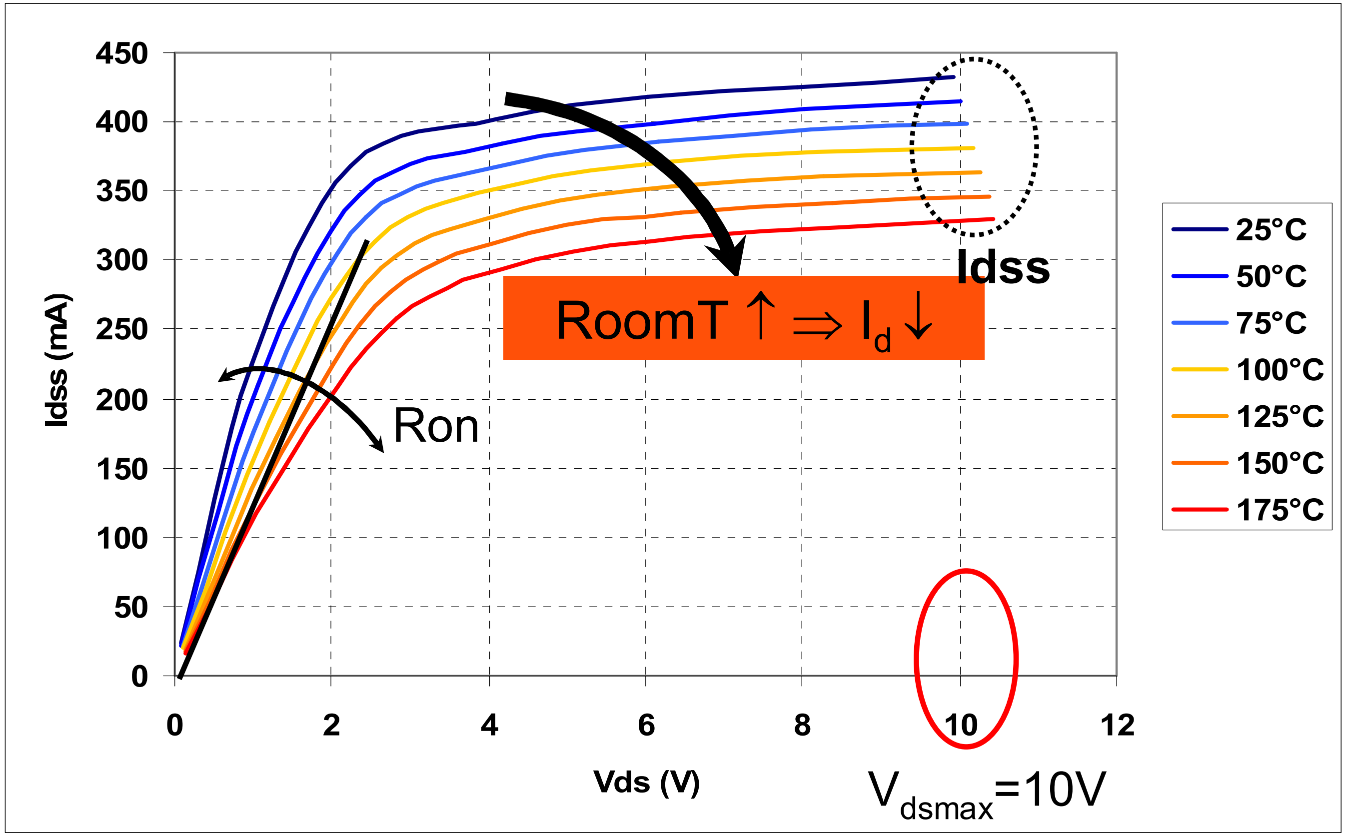
Kink effect only at intermediate temperatures

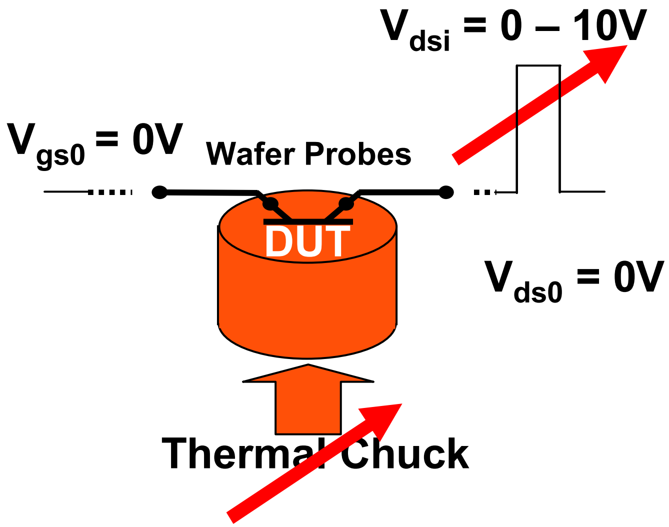
GaN 8x75 µm, Pulses 700ns, Period 10 µs, cold VDS0=0, VGS0=0 biasing point



This effect is explained by the temperature dependance of trap emission time constant

Ron and Idss measurements at different base-plate temperatures





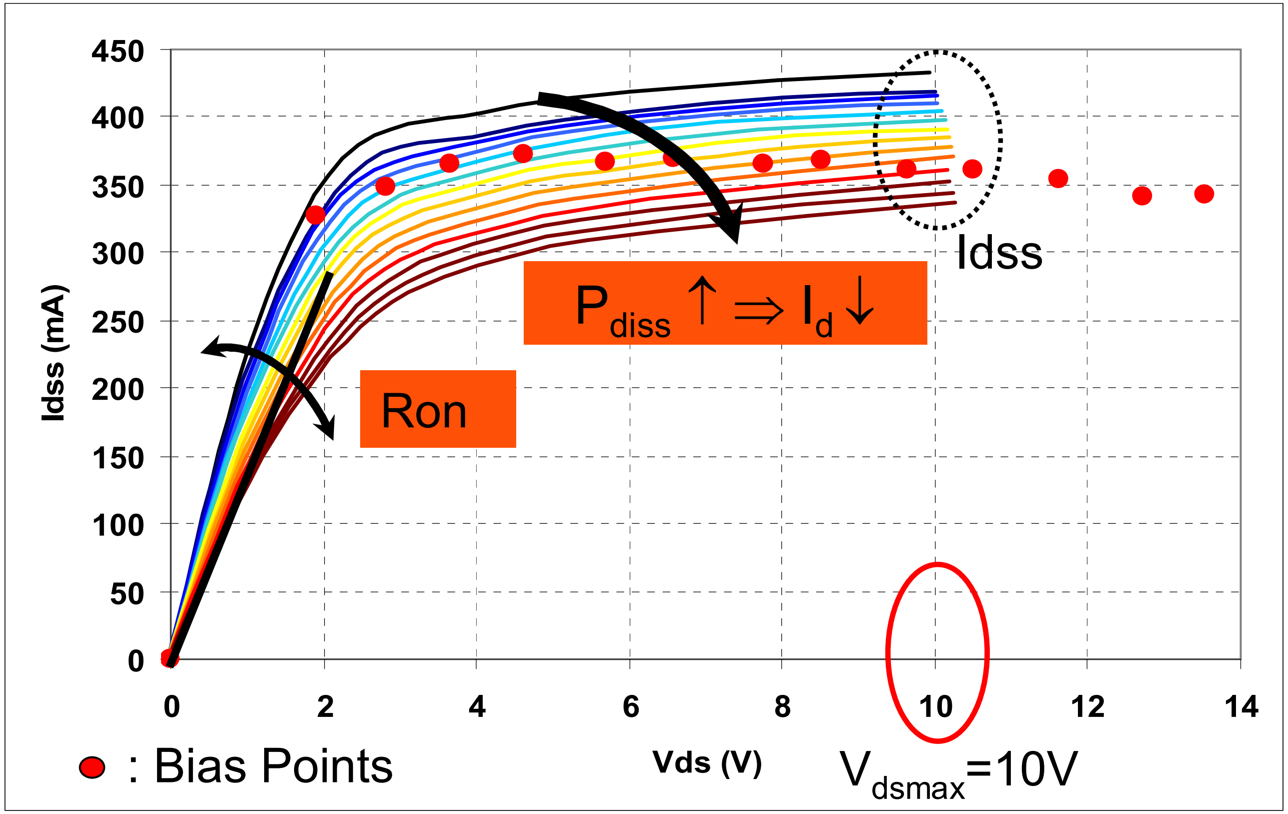
V_{gs0}: gate bias point.

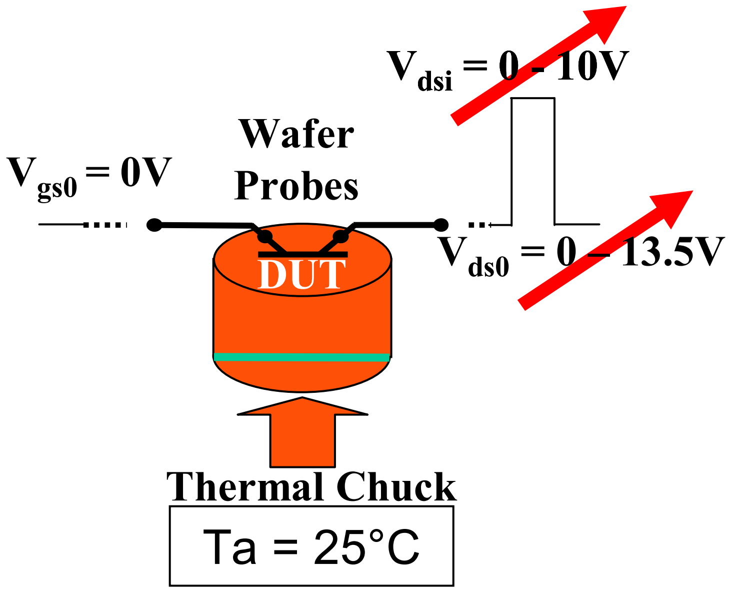
V_{ds0}: drain bias point.

V_{dsi}: drain pulsed point.

Pulsed I-V characteristics (V_{GS} = 0 V) from zero power bias point (V_{DS0} = V_{GS0} = 0 V)

Ron and Idss measurements for different dissipated power

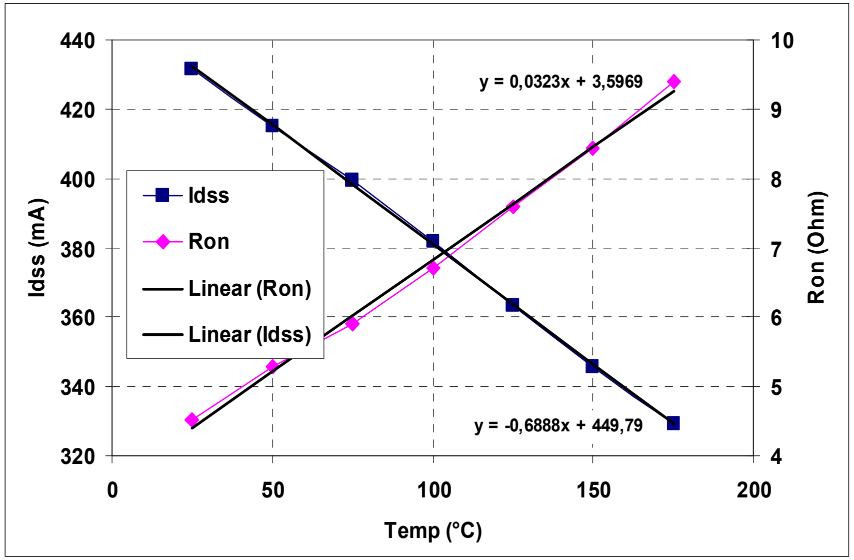




Pulsed I(V) characteristics (V_{GSi} = 0 V) from various quiescent bias points (VGS0 = 0 V, VDS0 = 2-13.5 V) with fixed thermal chuck at 25 °C

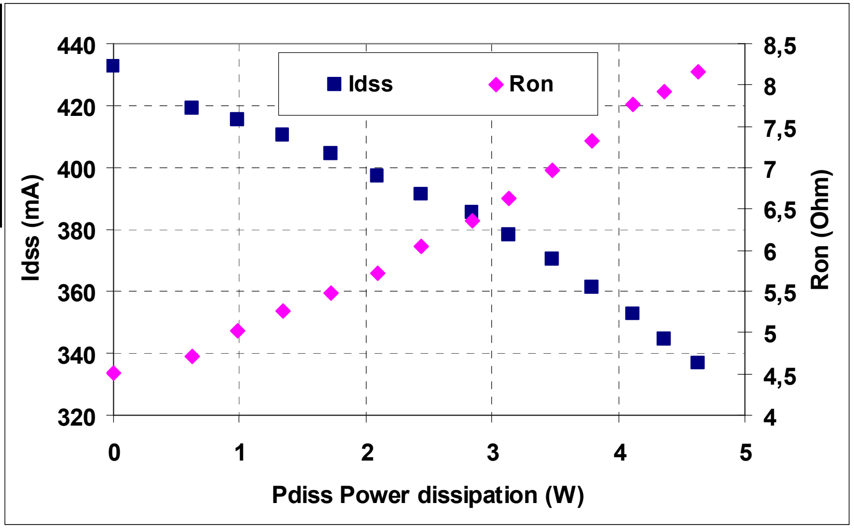
Variable Temp

Constant Pdiss = 0W



Constant Temp=25°C

Variable Pdiss



The Thermal Resistance is the ratio between the Ron slopes

$$R_{ON}(\Delta T) = R_{ON}(T_0) + \frac{dR_{ON}}{dT} \cdot \Delta T$$

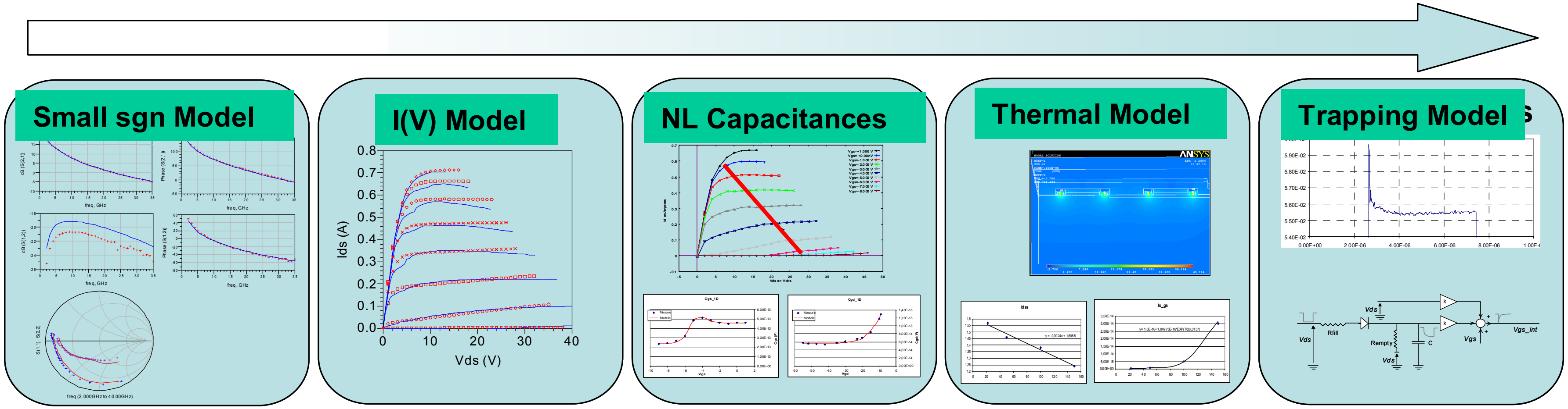
$$R_{ON}(P_{diss}) = R_{ON}(0) + \frac{dR_{ON}}{dP_{diss}} \cdot P_{diss}$$

- T_0=25 °C
- ΔT=T-T_0

$$R_{TH} = \frac{\Delta T}{\Delta P_{diss}} = \left(\frac{dR_{ON}}{dP_{diss}}\right) / \left(\frac{dR_{ON}}{dT}\right)$$

☺ Self-heating during pulses is not an issue because we extract a slope

Classic flow-chart of RF transistor NL modeling

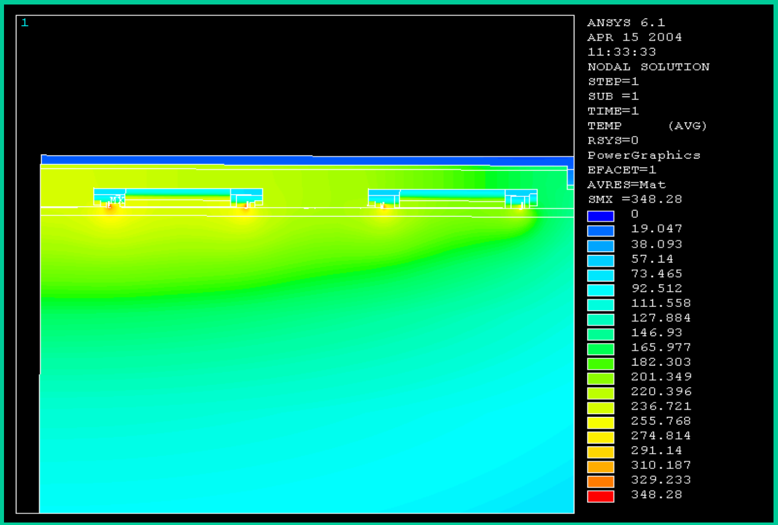


- Rg
- Lg
- Cpg
- Ls
- Cpd
- Ld
- ~~Rs~~, ~~Rd~~ → Rs=f(T), Rd=f(T), Rgd=f(T)

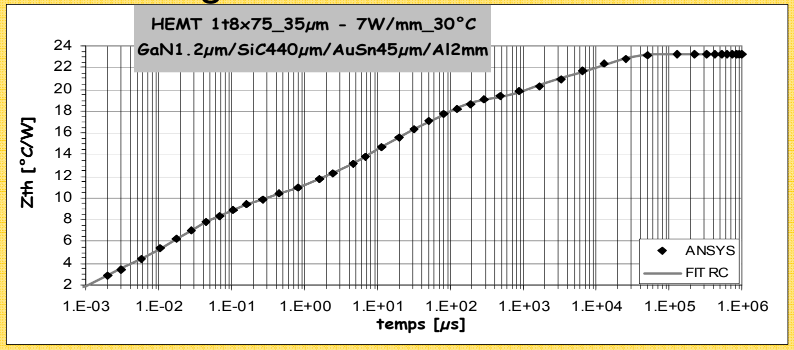
- Ri
- Cds
- τ
- ~~Gm~~, ~~Gd~~ → ~~Dgs=f(Vgs)~~, ~~Dgd=f(Vgd)~~, ~~Ids=f(Vgs,Vds)~~ → Dgs=f(Vgs), Dgd=f(Vgd), ~~Ids=f(Vgs,Vds,T)~~ → Ids=f(Vgs_pièges,Vds,T)
- ~~Cgs~~, ~~Cgd~~ → Cgs=f(Vgs), Cgd=f(Vgd)
- ~~Rgd~~ → Rs=f(T), Rd=f(T), Rgd=f(T)

Dynamical thermal behavior

3-D Thermal simulation

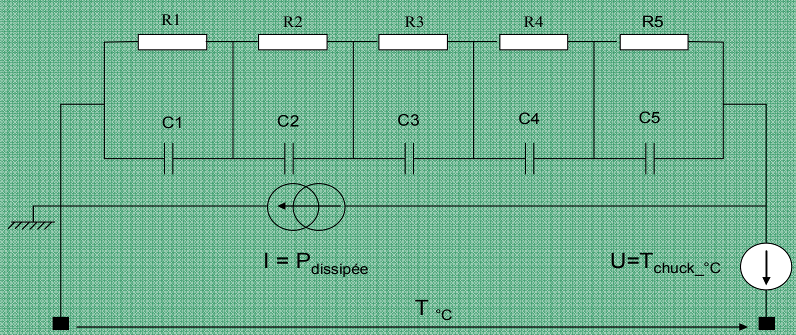


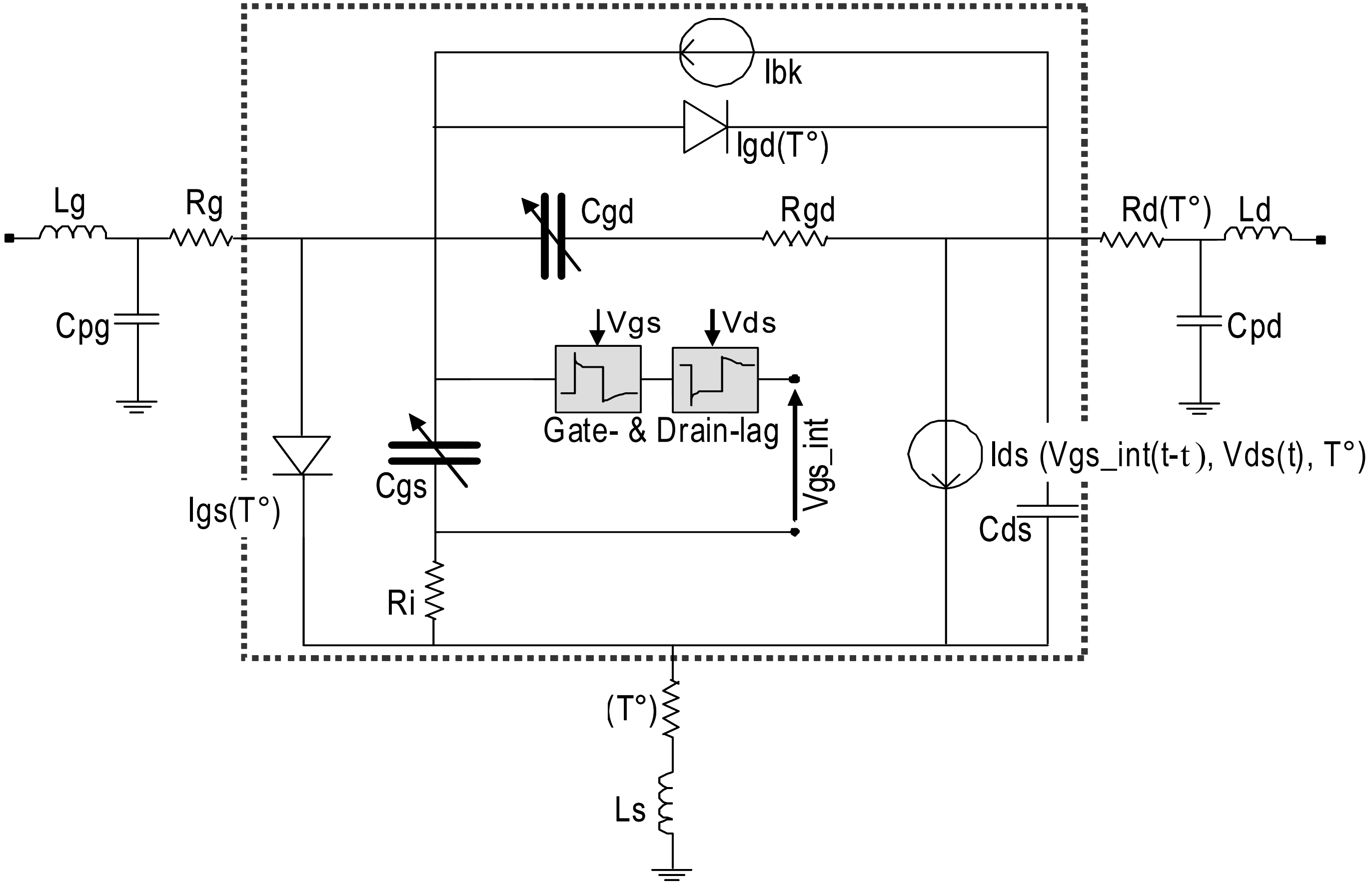
Heating versus time



$$TEMP = 22,8.(1-e-t/\tau 1) + 21,7.(1-e-t/\tau 2) + 7.(1-e-t/\tau 3) + \ldots$$

Thermal equivalent circuit for simulation





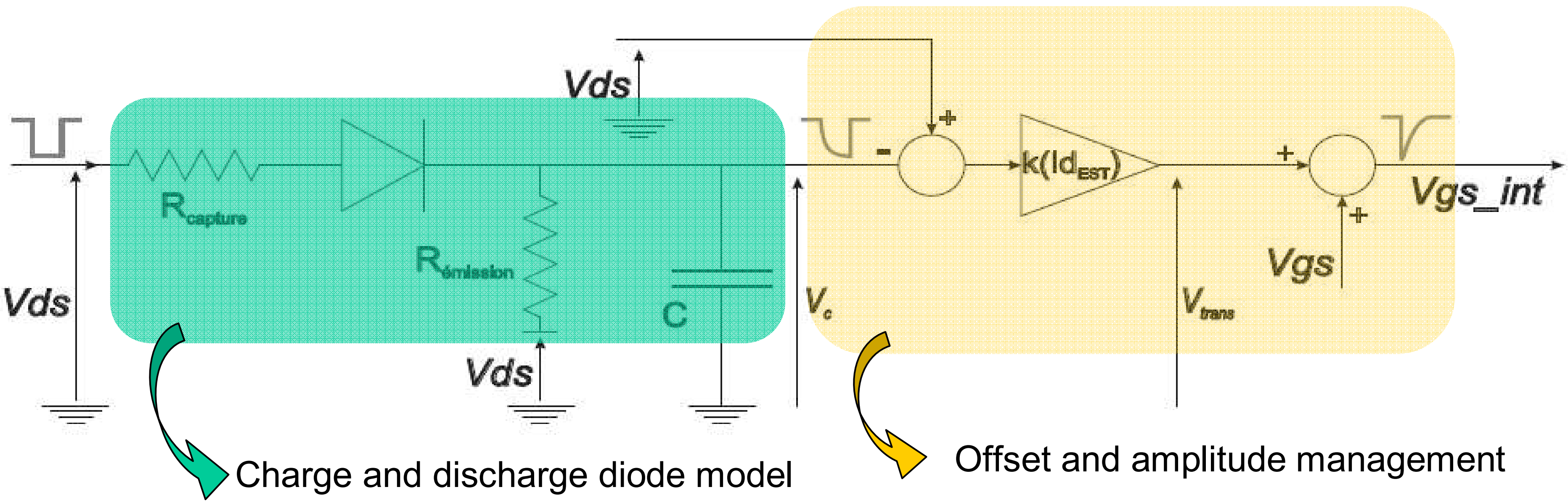
This is a possible FET model amongst many "good agreement" or improved models!

Such a model cannot be perfect everywhere, the targeted application must be considered

Zoom into the trapping effect bloc (for one trap level)

The trap effects on drain current are taken into account by a modified VGS (Vgs_int)

Note the unsymmetrical capture and emission effects modeled by the envelope detector



Conclusions on LF memory effects

- **We have shown some electrical effects of LF memory effects, there are many others:**
  - *at circuit level when large peak to average are applied*
  - *at system level (Bit Error Ratio)*
  - *phase shifts are to be considered for RADAR applications…*
- **We have shown some techniques to characterize LF memory effects**
  - *a lot of work is carried out in labs to find reliable techniques to separate trapping and thermal effects (same frequency range)*
  - *fast pulses and very low frequency measurements are interesting ways*
- **We have shown some possible modeling approach based on equivalent circuit**
  - *Many model topologies, equations and methods are available*
  - *With improved Volterra models (like X-Parameters), long-term memory effects can now be taken into account with models driven by meas. data*

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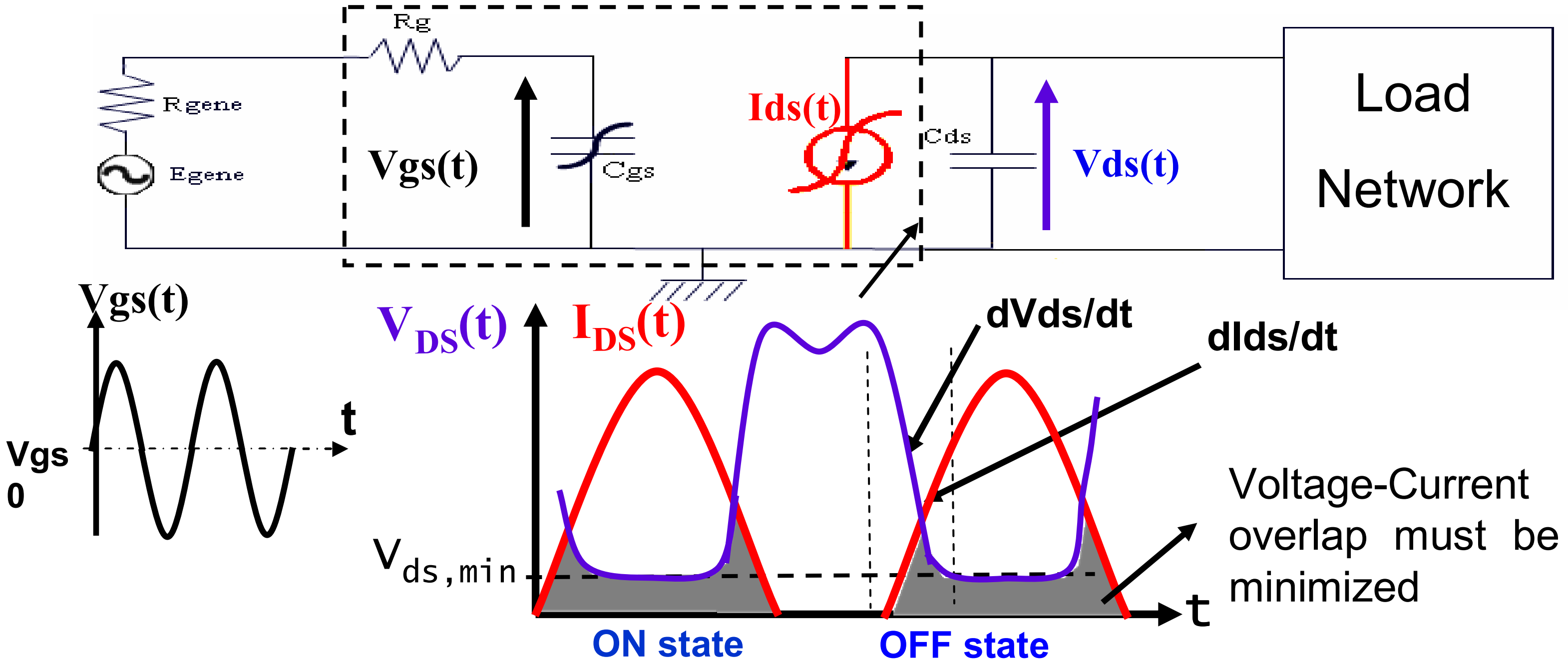
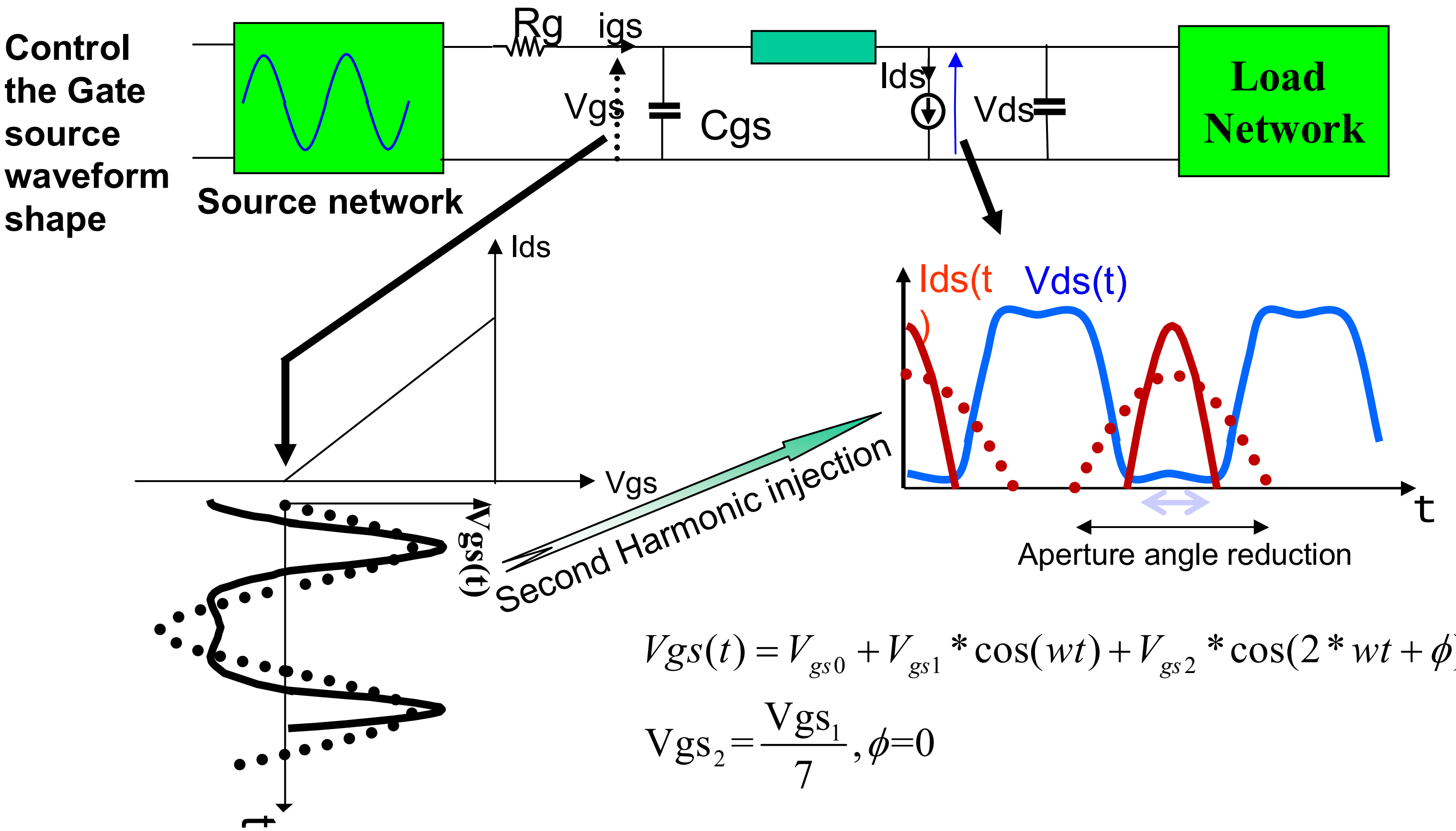
Simplified GaN HEMT model



Voltage-Current overlap must be minimized

- **Minimization of dissipated power:**
  During ON state Vds must be minimum => Low $R_{ds,on}$
  During transitions dV_{ds}/dt and dI_{ds}/dt must be maximum => Low capacitances (Cgs,Cds)

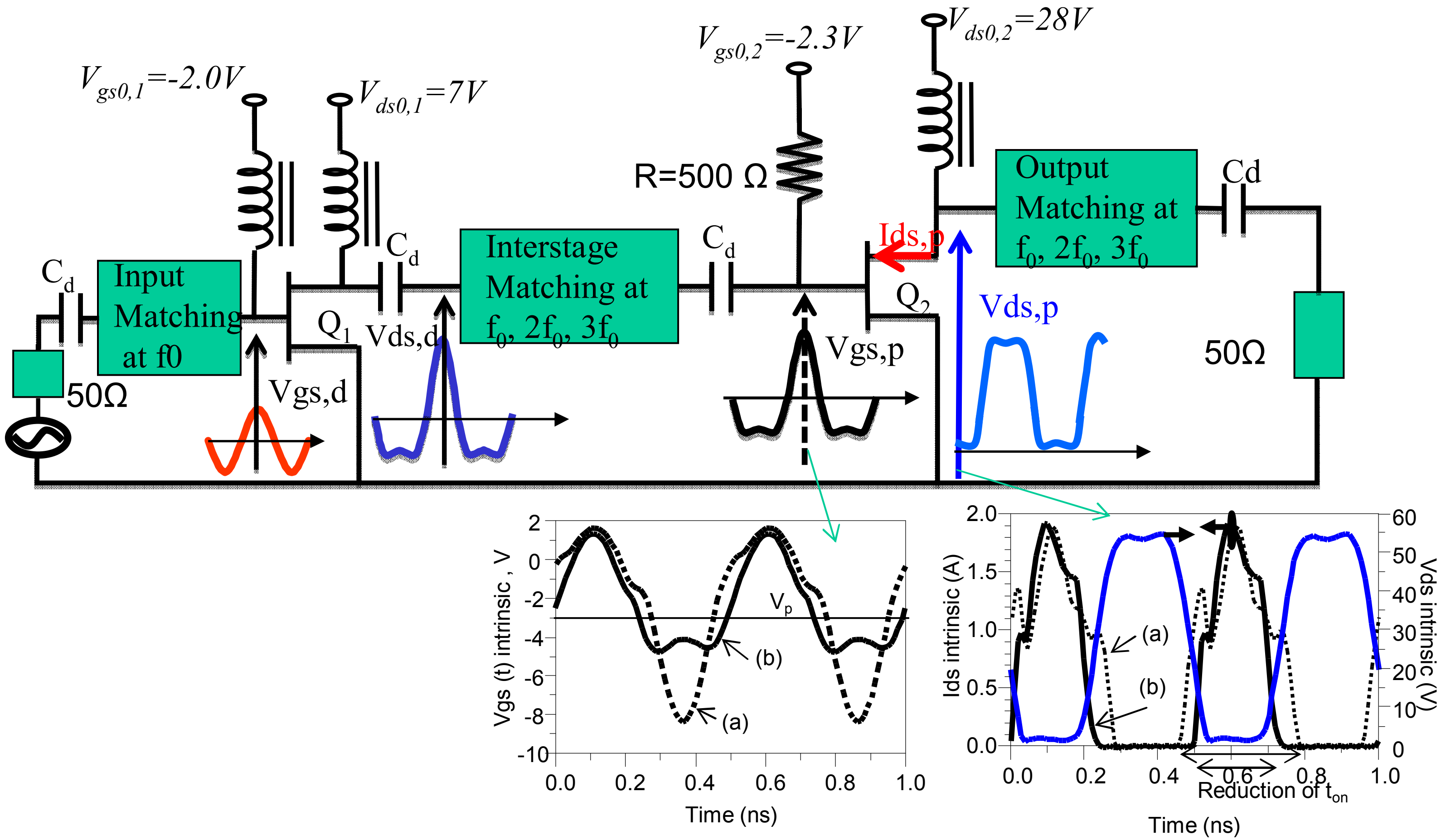
PAE enhancement by gate source voltage shaping



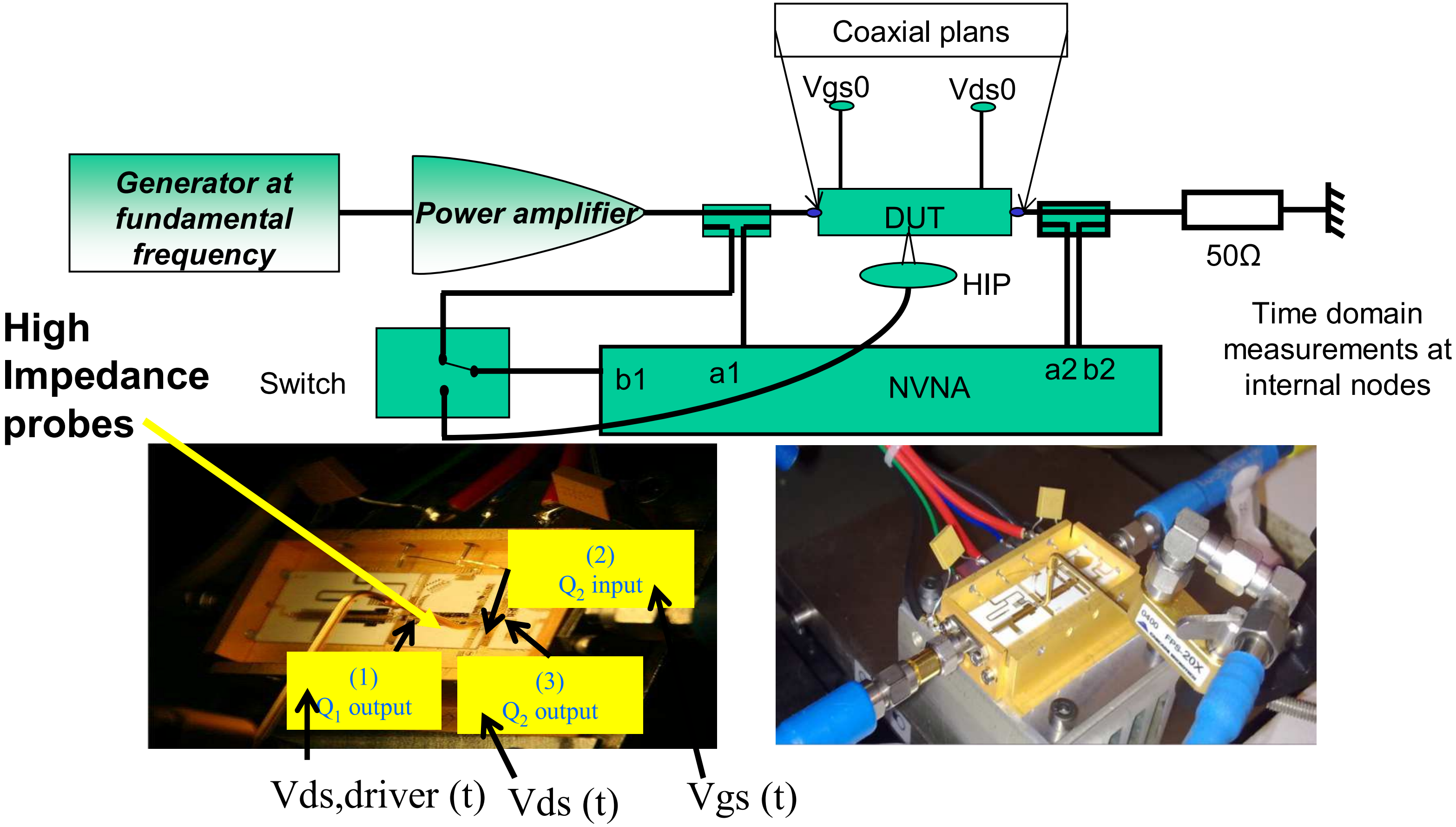
$$Vgs(t) = V_{gs0} + V_{gs1} * \cos(wt) + V_{gs2} * \cos(2 * wt + \phi)$$

$$Vgs_2 = \frac{Vgs_1}{7}, \phi = 0$$

Two stage PA design

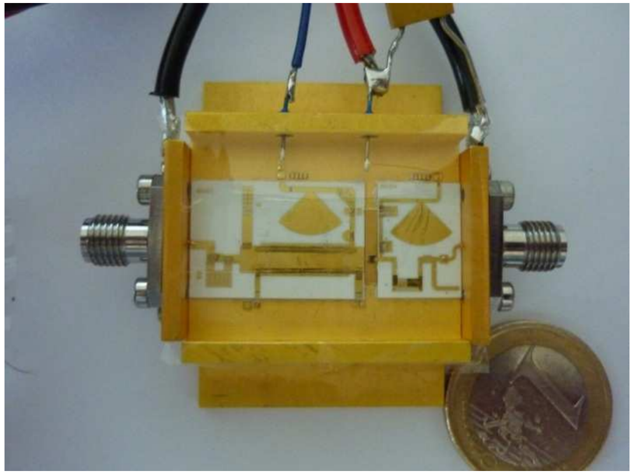


Time domain measurements at internal nodes

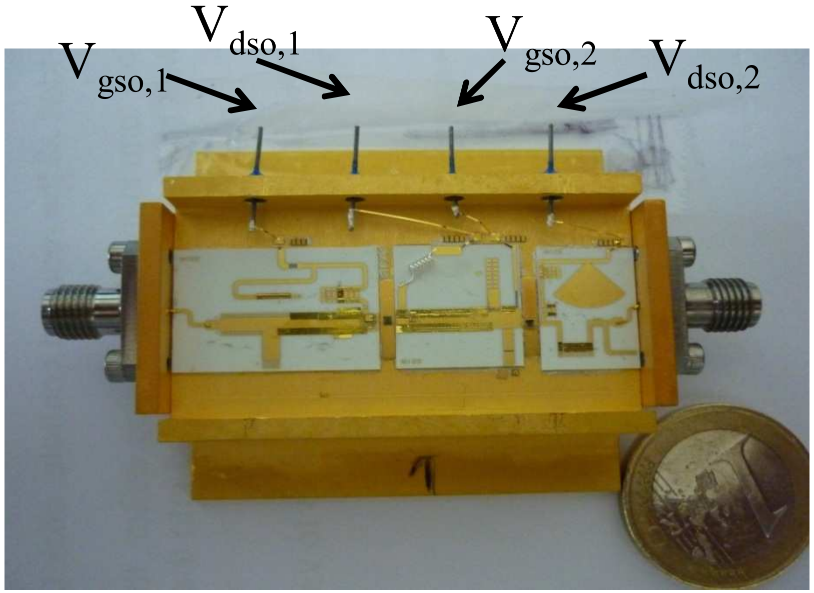


High impedance probing for waveform checking and tuning

Comparison with a conventional class F design

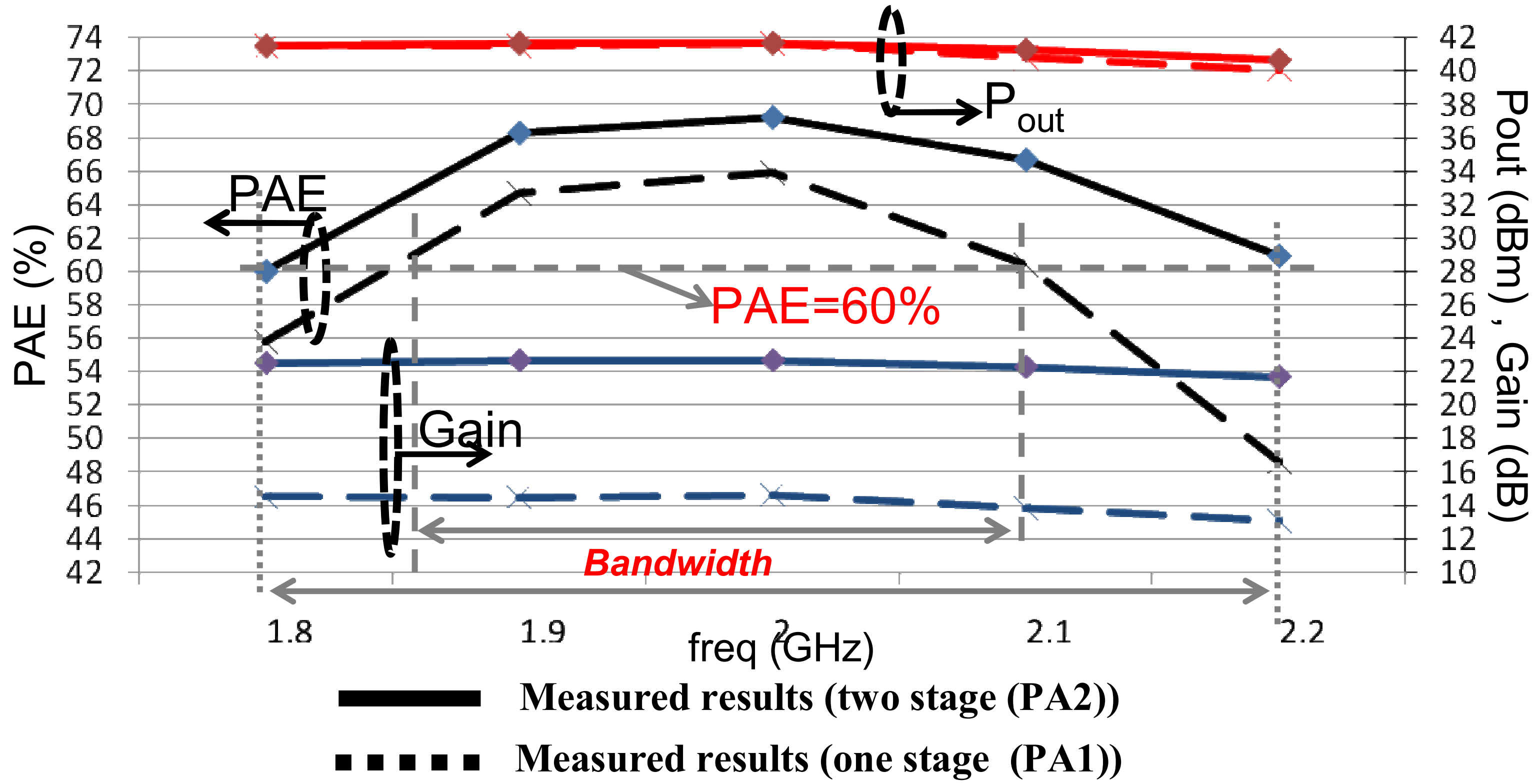


Single Stage
conventional class F PA
(PA1)



Two Stage PA with gate source
voltage waveform shaping
(PA2)

Measurement results at connector ports



Comparison between single and two stage Power Amplifiers (same foundry)
Large Signal Measurement results at 4 dB gain compression

- Introduction
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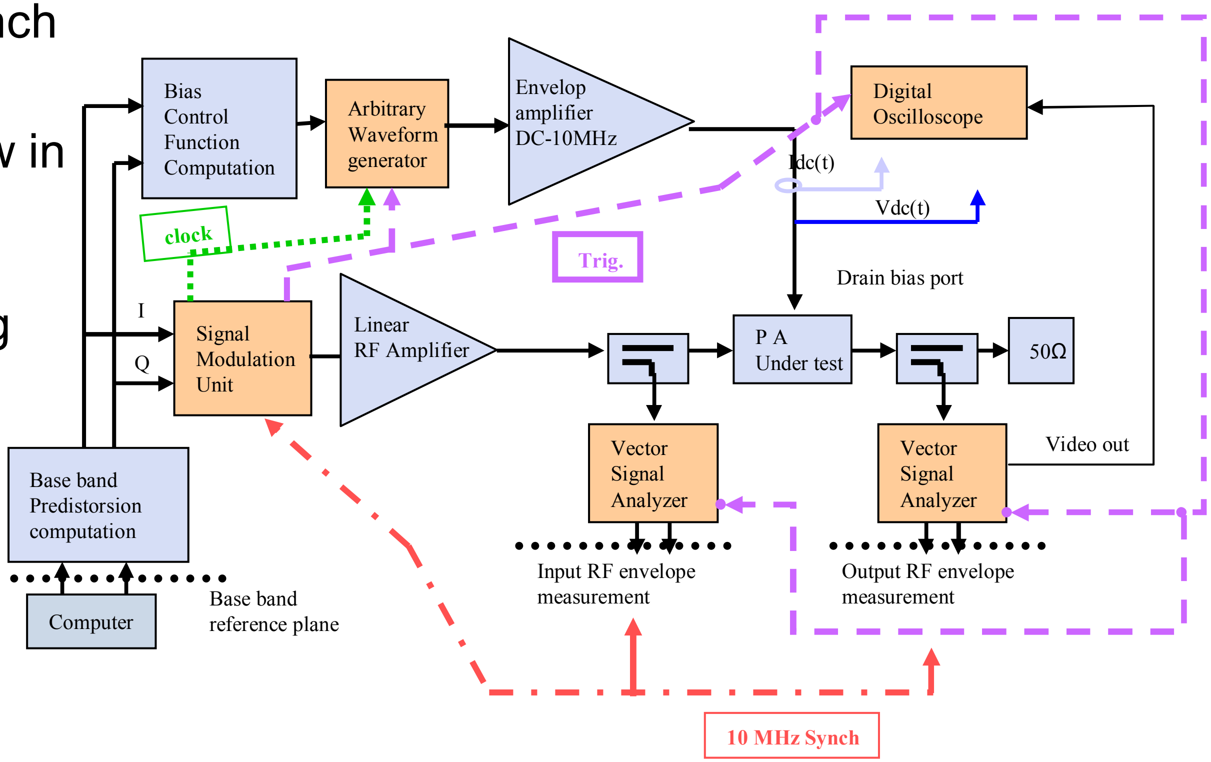
High Efficiency ⇨ Power amplifier architectures based on dynamic biasing techniques

Linearity ⇨ Power amplifier architectures based on digital pre-distortion

➔Development of Specific test-Bench

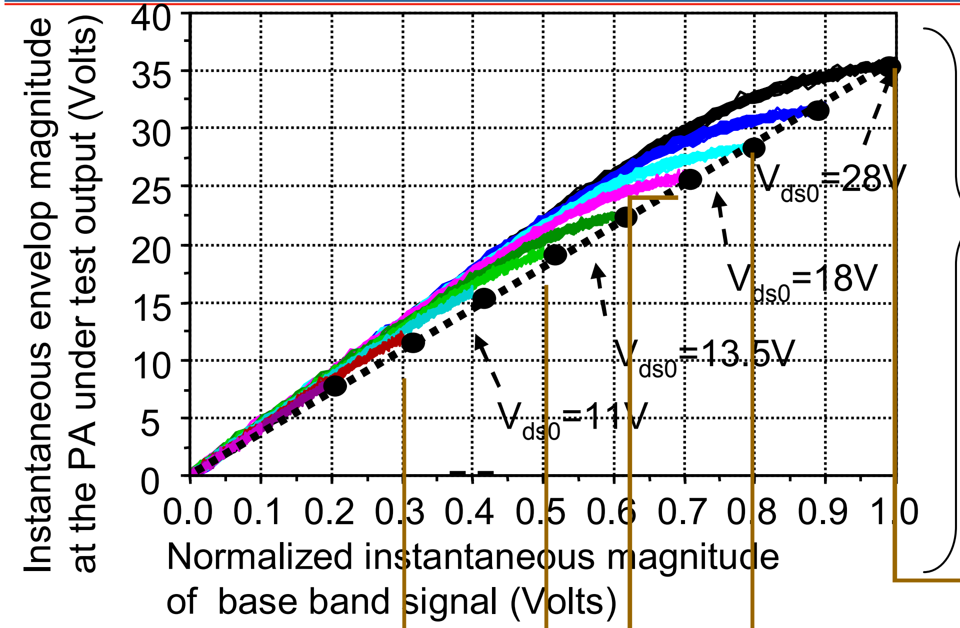
- Identify dynamic drain bias law in presence of memory effects.
- Apply both Envelope Tracking (ET) and Digital Pre-Distortion (DPD) techniques.
- Maximize both PAE and linearity.



Clock synchronization and envelope trigger signals are carefully controlled

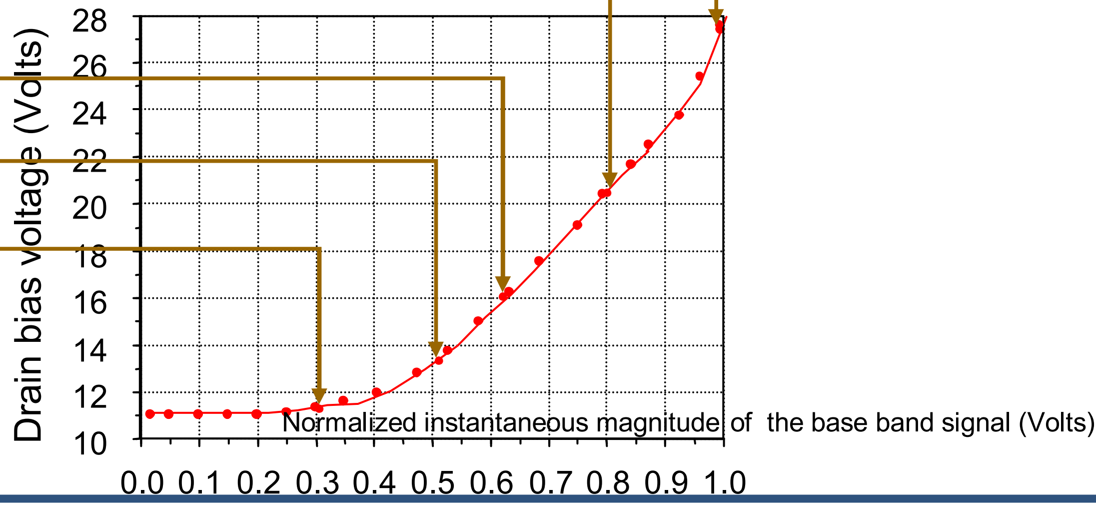
Appropriate time alignment between RF signal envelope and drain bias signal are achieved

Extraction of drain bias law (100 KHz 16-QAM)

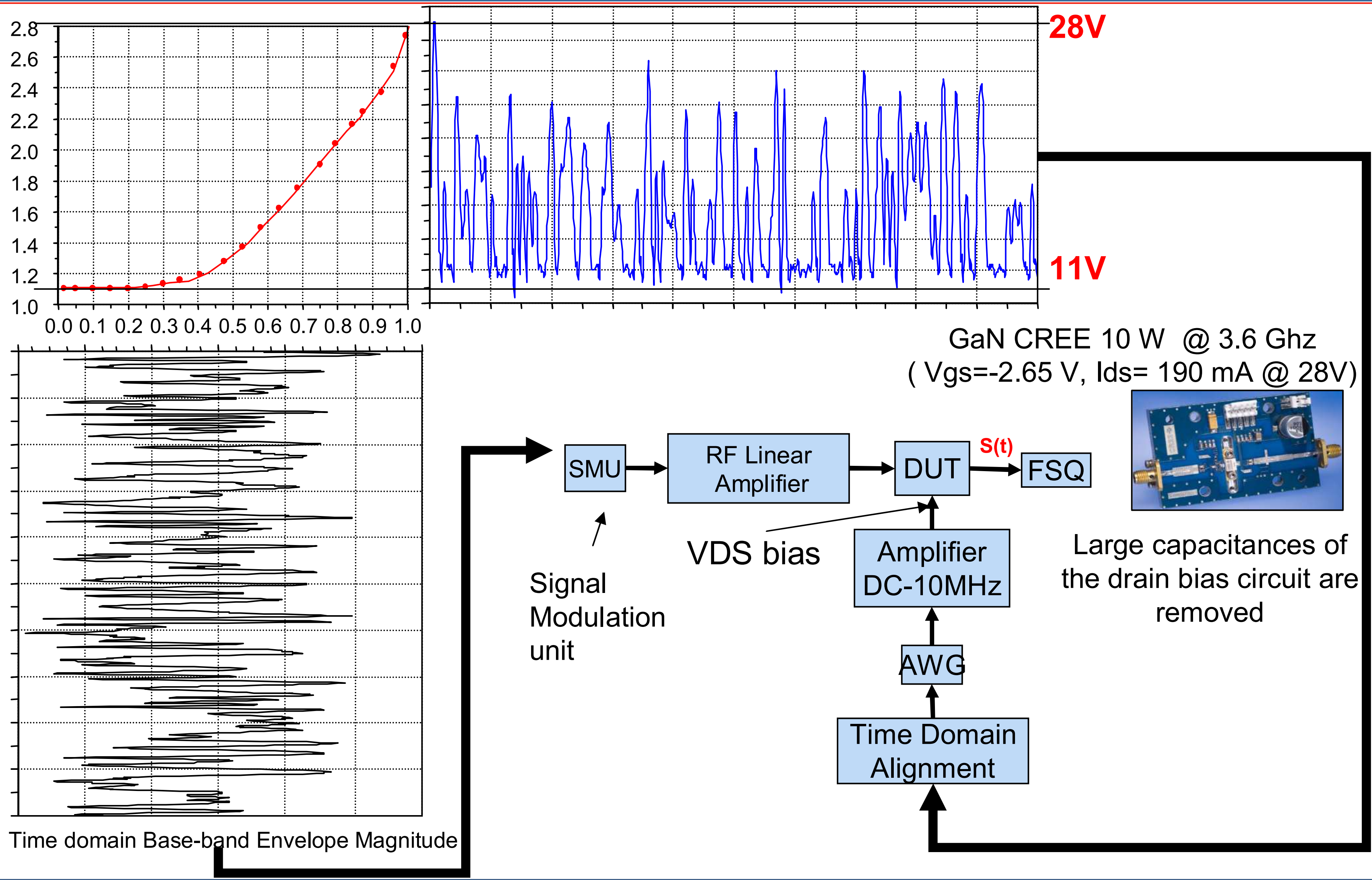


- Modulated signal is applied to the PA input (QAM16 in the present case).
- Fixed DC voltage is applied to the drain bias port.
- Instantaneous input/ output envelop transfer functions are recorded.

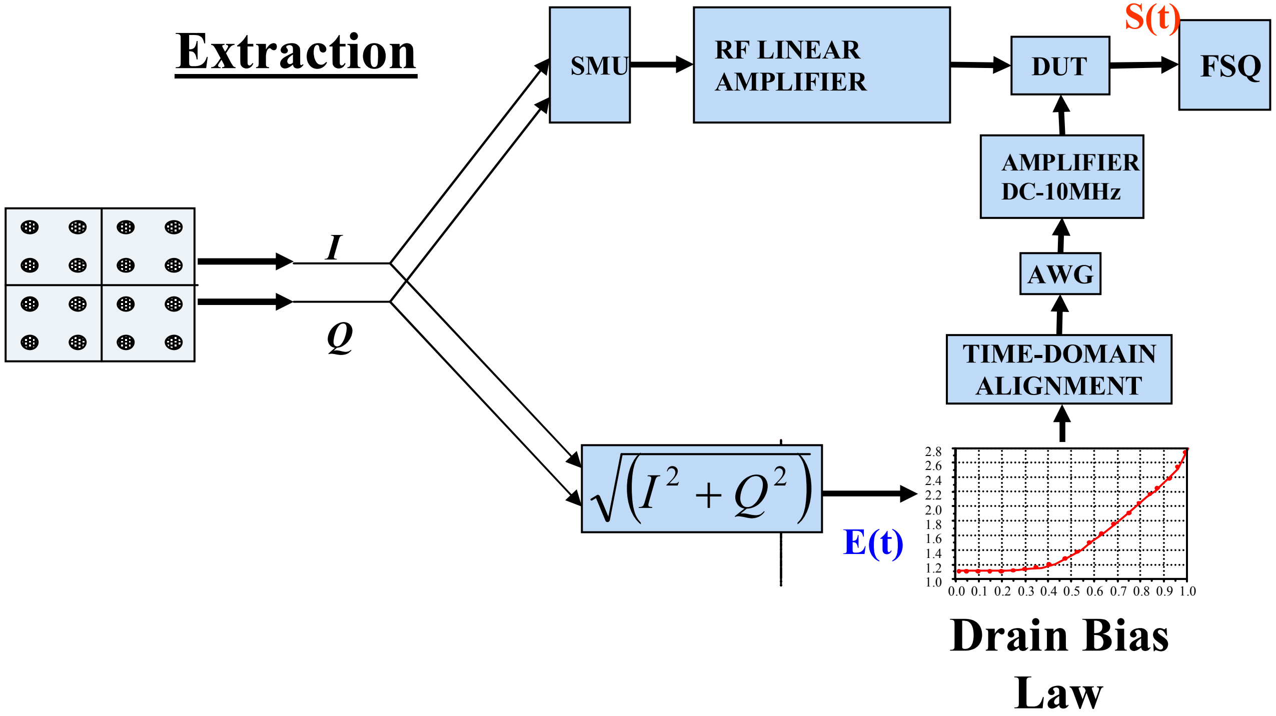
The coordinates of the targeted drain bias law are taken to keep constant saturated gain and high drain efficiency

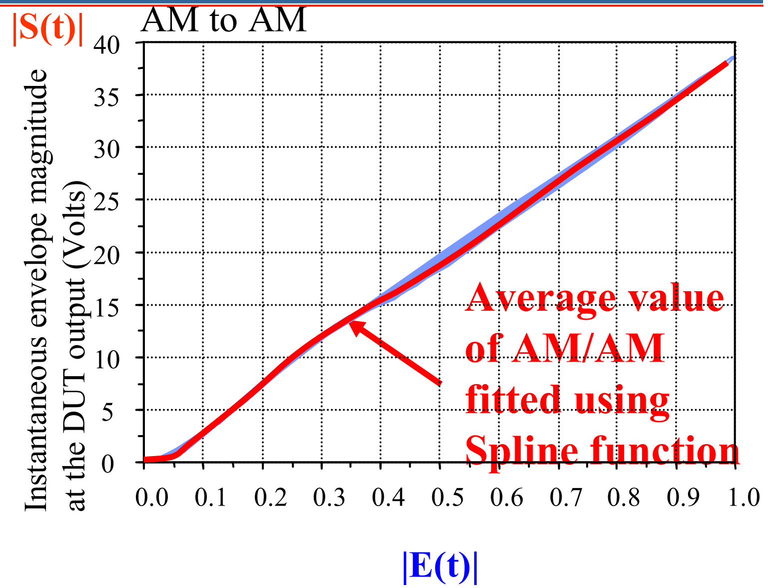


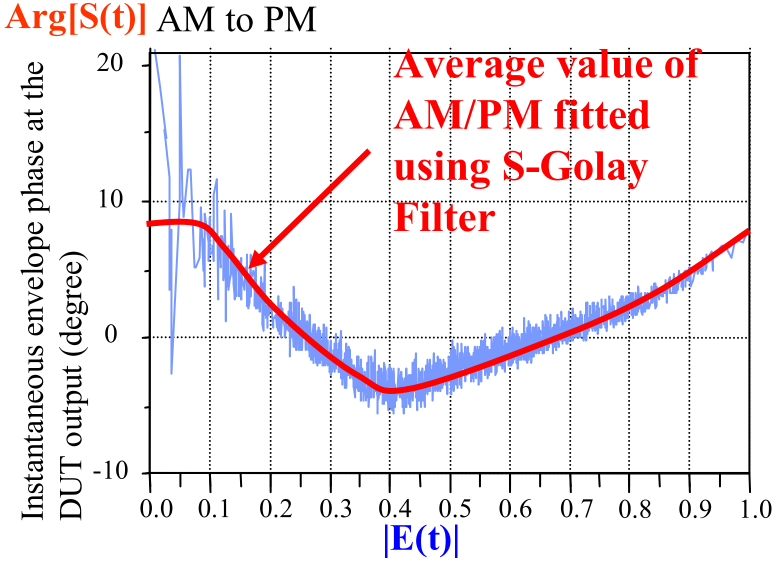
Application of drain bias law (100 KHz 16-QAM)



Extraction







- A simple first order base band predistorsion technique
- It consists in extracting spline functions fitting the average of measured dynamic AM/AM and AM/PM characteristics of the ET amplifier, and inverting them
- Can be improved (DSP, FPGA) to consider LF memories

OFDM Signal 128 sub carriers 16QAM at 1MBit/S
Oversampling Ratio=4 Fe=4MHz

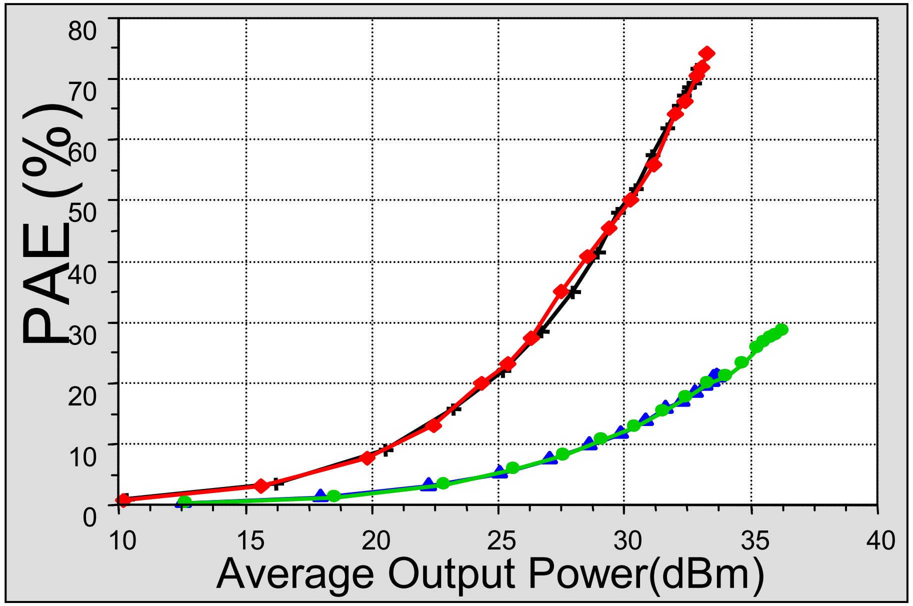
GaN CREE 10 W @ 3.6 Ghz (Vgs0=-2.65 V , IdsQ= 190 mA @ 28V)

Constant Vds

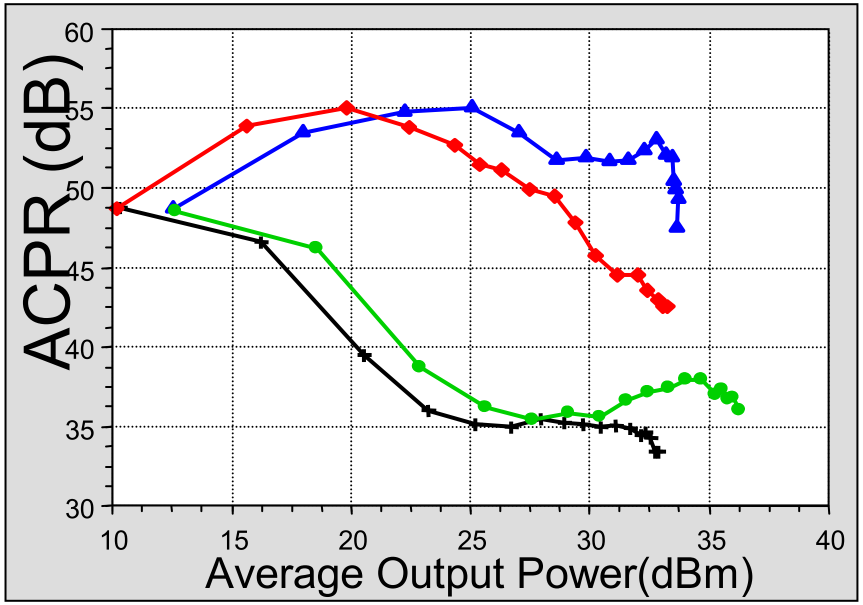
ET

ET + DPD polynomial

DPD Polynomial



Main effect of Envelope Tracking (ET)



Main effect of Digital PreDistortion (DPD)

Outline

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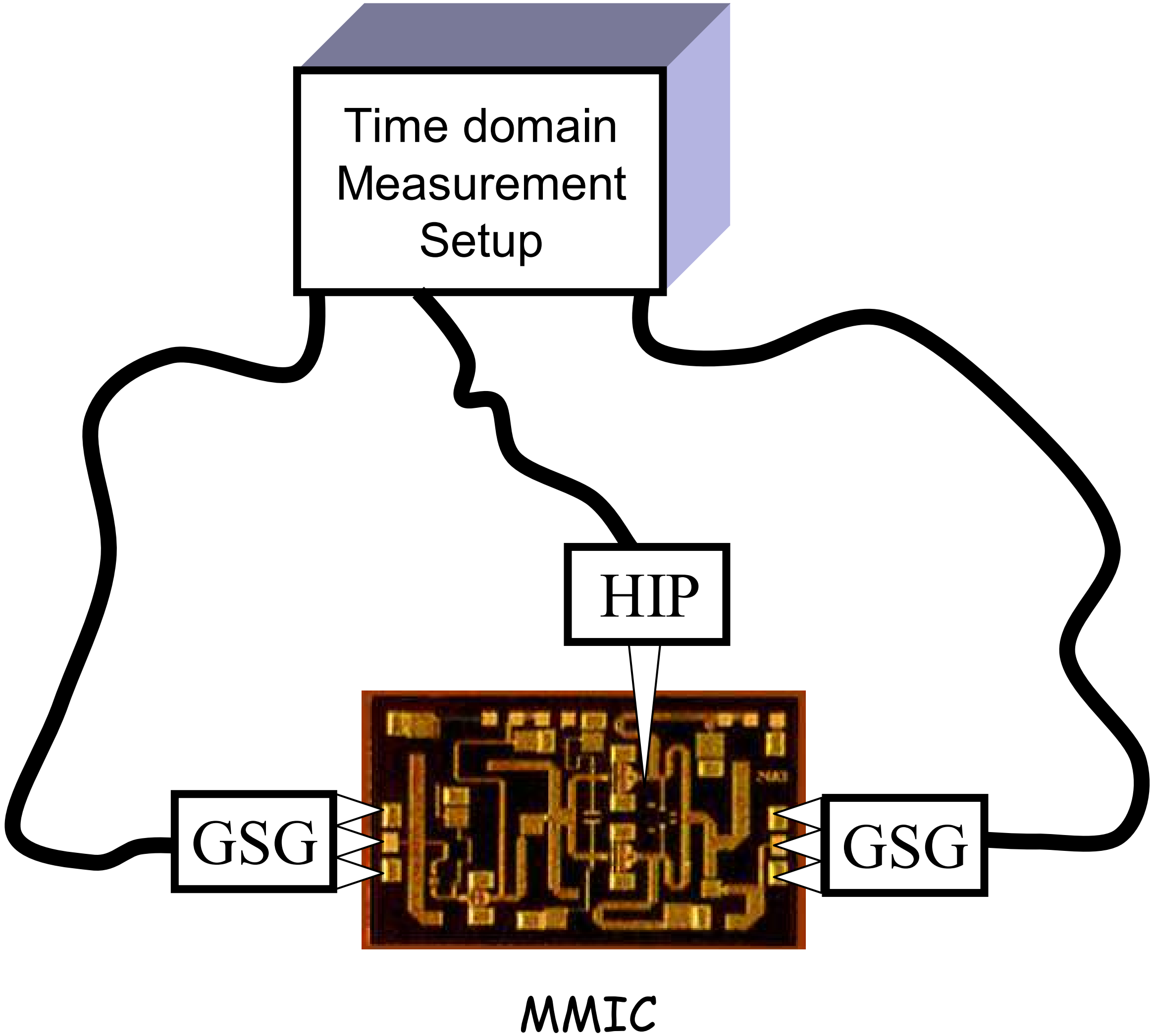
Motivations for High Impedance Probes (HIP)

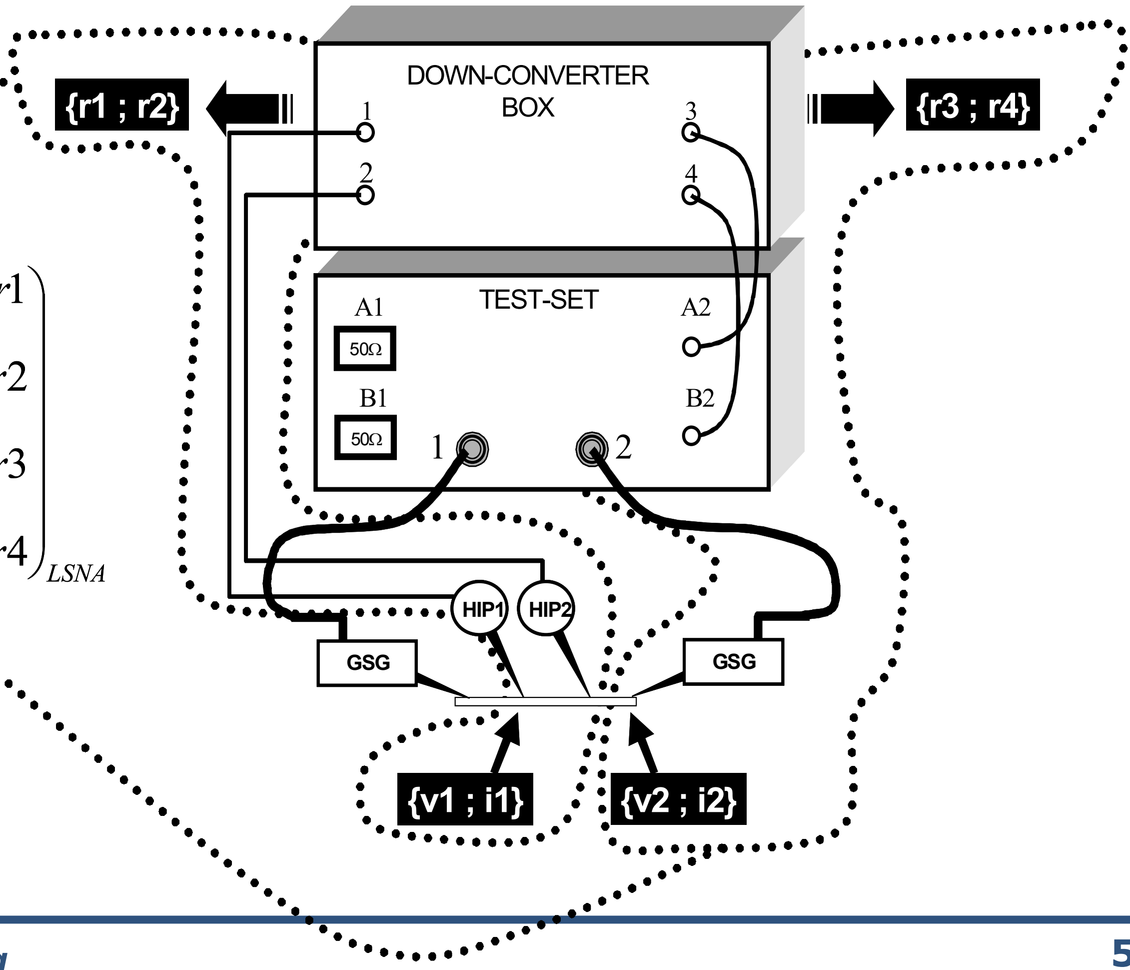


HIP calibration assumption

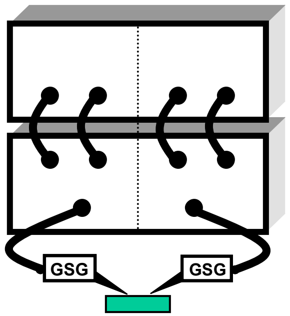
$$V_{ref.\,plane}(f) = \tilde{K}(f).V_{raw}(f)$$

Measurement Setup

$$\begin{pmatrix} v1 \\ i1 \\ v2 \\ i2 \end{pmatrix}_{LSNA} = \begin{bmatrix} \alpha_1^{HIP} & \beta_1^{HIP} & 0 & 0 \\ \gamma_1^{HIP} & \delta_1^{HIP} & 0 & 0 \\ 0 & 0 & \alpha_2^{CAL} & \beta_2^{CAL} \\ 0 & 0 & \gamma_2^{CAL} & \delta_2^{CAL} \end{bmatrix} \bullet \begin{pmatrix} r1 \\ r2 \\ r3 \\ r4 \end{pmatrix}_{LSNA}$$



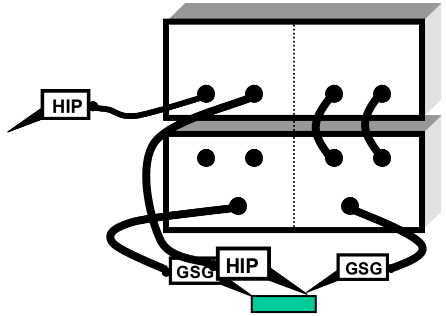
1. NVNA calibration (LRRM)



$$\begin{pmatrix} v1 \\ i1 \\ v2 \\ i2 \end{pmatrix}_{LSNA} = \begin{bmatrix} \alpha_1 & \beta_1 & 0 & 0 \\ \gamma_1 & \delta_1 & 0 & 0 \\ 0 & 0 & \alpha_2 & \beta_2 \\ 0 & 0 & \gamma_2 & \delta_2 \end{bmatrix} \bullet \begin{pmatrix} r1 \\ r2 \\ r3 \\ r4 \end{pmatrix}_{LSNA}$$

→ Ref. plane = voltage standard

2. Calibration with 1 HIP



- HIP @ ref. plane
- « Sweep-sin »
- Measurements :
  - > v_2 (NVNA calibrated)
  - > v_{HIP} (raw data)

→ $$\tilde{K}(f) = \frac{v_2(f)}{v_{HIP}(f)}$$

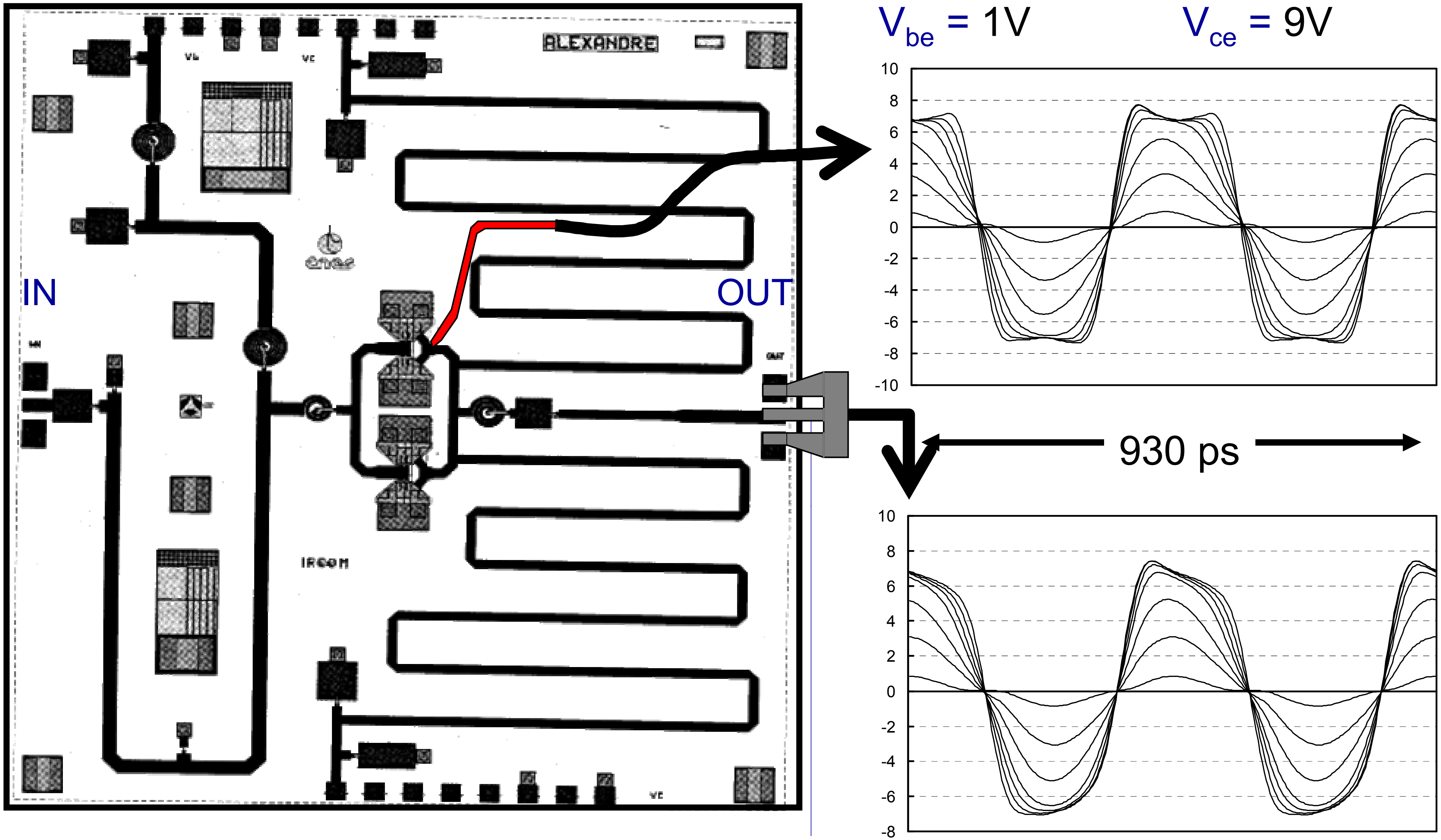
3. Define a new error-matrix (NVNA + 2 HIPs)

Measurement of 2 voltages (M1)

$$\begin{pmatrix} v1 \\ i1 \\ v2 \\ i2 \end{pmatrix} = \begin{bmatrix} \tilde{K}_1 & 0 & 0 & 0 \\ 0 & \tilde{K}_2 & 0 & 0 \\ 0 & 0 & \alpha_2 & \beta_2 \\ 0 & 0 & \gamma_2 & \delta_2 \end{bmatrix} \bullet \begin{pmatrix} r1 \\ r2 \\ r3 \\ r4 \end{pmatrix}$$

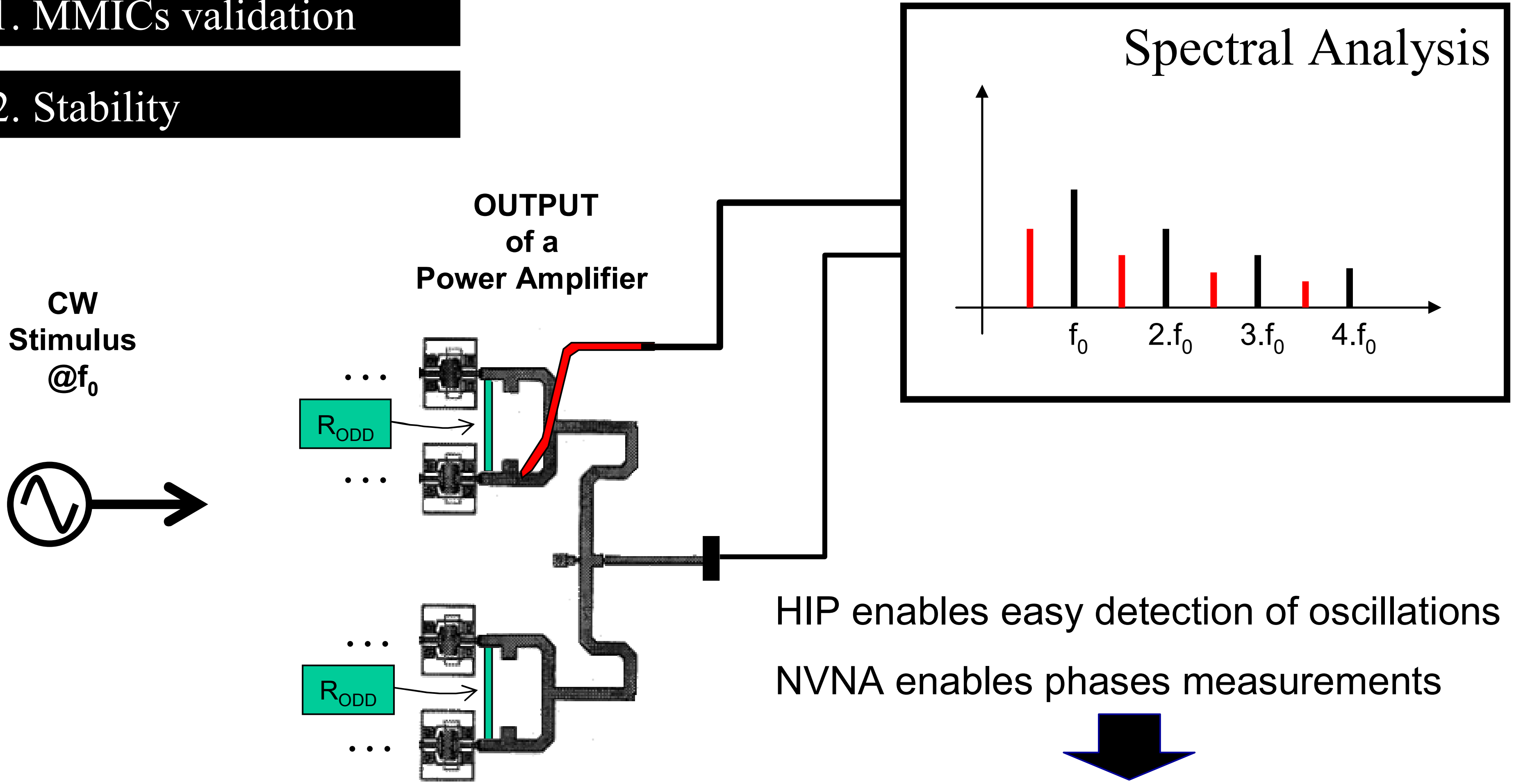
v1(t) ⇔ v1(t)
i1(t) ⇔ v2(t)

HIP measurement applications (1/2)



1. MMICs validation

2. Stability



HIP enables easy detection of oscillations

NVNA enables phases measurements

KNOWLEDGE OF NONLINEAR PHENOMENA

OPTIMAL DESIGN FOR POWER AMPLIFIERS

SIMULATIONS

MEASUREMENTS

Analysis…
Identification…
Understanding…

of

DYNAMICS
NONLINEAR
PHENOMENA

- ~~Time Domain Integration~~ ⟷ Time domain consistency ⟷ ~~Time Domain Characterization~~
- **Harmonic Balance + Envelope Transient** ⟷ Time & space domains consistency ⟷ NVNA+ HIP

↓

Optimized designs of MMICs

- **Introduction**
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- **High impedance probing**
- **Conclusion**

Conclusions

- **NonLinear measurement of RF active devices are mandatory**
  - *for transistor test, modeling and model verifications*
  - *for memory effects identification*
  - *for direct optimization of SSPAs*
  - *for reliability investigations*
  - *….*

TARGET
TOP AMPLIFIER RESEARCH GROUPS IN A EUROPEAN TEAM

- **Research is still going on**
  - *New ways to separate and accurately measure LF memories*
  - *New measurement instruments, new set-ups*
- **Cost of NL measurements is to be considered (Return On Invest)**
  - *We estimate that clever NL meas. are the best way for SSPA 1st pass success*

A lot of research on RF NL topics (measurement, modeling, instrumentation…) is carried out in Europe. Here in Vienna it's the good place to thank again the TARGET Network of Excellence for its unvaluable support.