Design and Modeling Method of Package for Power GaN HEMTs to Limit the Input Matching Sensitivity

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***Abstract*— This paper proposes a packaged transistor modeling using lumped elements. This model allows studying the input impedance dispersion when a range of variation is applied to various package components. This dispersion is also highlighted when a load impedance variation is applied to the package transistor. It is demonstrated that this dispersion can be corrected using a specific input pre-matching and by having a very good information about input return loss contours. Moreover, this specific packaged transistor presents input impedance close to 50Ω over [3.0-3.8]GHz.**

Keywords-component; Packaged transistor modeling; GaN HEMT; pre-matching; power amplifiers; load-pull measurements

I. INTRODUCTION

Packaged GaN HEMTs are increasingly implemented in communication systems in S band. Reliability of its modeling is a key point for power amplifier design. Various approaches were proposed to extract package model. EM simulations were often used [1]. In this study, the package was modeled using lumped components. First part will be devoted to the model extraction and validation.

During the package making, uncertainties exist about physical characteristics of the package. Second part will expose the impact on performances of size uncertainties or electrical property uncertainties. This impact will be particularly analyzed on the packaged transistor input impedance. This study focuses on this input impedance because it is the most sensitive characteristic. Third part will also highlight the strong dispersion of the packaged transistor input impedance when a small load impedance variation is applied.

The last part presents a specific input pre-matching that allows desensitizing the packaged transistor to disruption. Moreover, input matching capability of this packaged transistor will be studied over a wide bandwidth in S band.

II. PACKAGED TRANSISTOR MODELING AND VALIDATION

A 2.4mm (6x400µm) GaN HEMT die from UMS foundry is used for this study. The package is chosen to ensure a good impedance transformation between on-wafer transistor and package access. The model is extracted from on-wafer and packaged transistor S-parameter measurements. To take into account the source bond wires when the transistor is packaged, a linear model of the on-wafer transistor is extracted for many bias points.

The metal ceramic package used in this study is modeled using lumped elements [2]. One physical component of the package is modeled by one electrical lumped element. Also, different electrical elements are set each side of the previous transistor linear model. Fig. 1 shows a package equivalent model for one package configuration. This packaged transistor is realized and modeled, and will be studied in part III and IV.

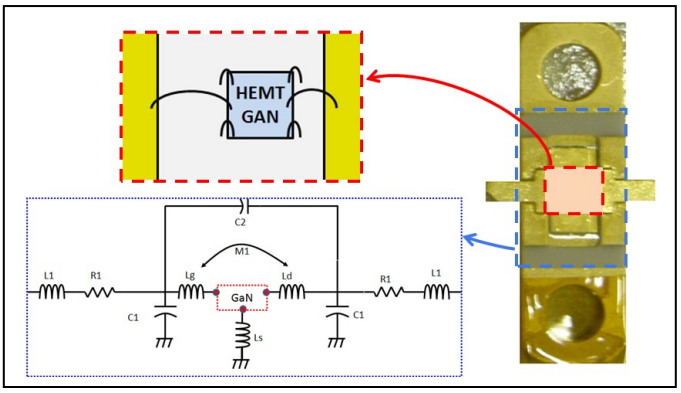

Figure 1. Equivalent circuit model of the metal-ceramic package.

Each bond wire is represented by an inductance L. Also, gate, drain and source bond wires are respectively modeled by equivalent inductance Lg, Ld and Ls. The four source bond

wires are far enough to consider them as only one equivalent inductance Ls without mutual.

However, mutual inductance [3] is accounted for the inductive coupling between gate and drain wires.

Capacitances (C1) represent package input and output metal ceramic, which are connected by a coupling capacitance (C2). R1 resistance is assimilated as global loss and L1 inductance represents parasitic effects between the package lead and the lines of the test fixture.

Measured S-parameters over the 1-7GHz range, and large-signal CW pulsed measurements were used to verify the reliability of the packaged transistor model. Fig. 2 presents S-parameter comparisons between packaged transistor measurements and electrical model simulations at the bias point Vds=50V and Id0=40mA.

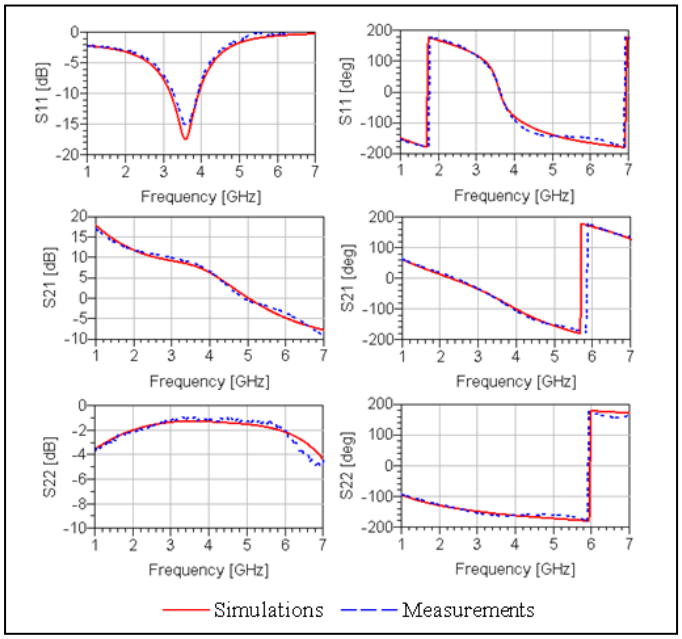

Figure 2. S-parameter comparisons between package measurements and electrical model simulations.

For large signal validation, a classic non linear electro thermal model [4] is performed. Now, the packaged transistor model associates the non linear electro-thermal model of the GaN die with the package elements. Following steps of this study focus on packaged transistor input impedance at 29dBm input power that corresponds to 2dB of gain compression. The input RF signal is pulsed using 10µs pulse width and 10% duty cycle, while biasing voltages are continuous. Gate bias voltage is close to pinch off and drain bias voltage is set to 50V. Moreover, input return loss contours will be often presented in next steps. Also, measured and simulated input return loss contours were compared as shown in Fig. 3. Input return loss contour measurements were calculated using IVCAD software [5].

This comparison reveals a very good agreement between measured and simulated input impedances and between input return loss contours.

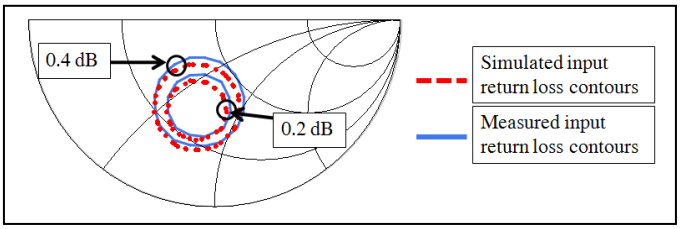

Figure 3. Comparison between measured and simulated input return loss contours for the optimal load impedances at 3.6GHz.

III. Impact of Package Element Variations on the Packaged Transistor Input Impedance

This part highlights the input impedance dispersion when variations are applied to package components. These variations can be characterized by modeling errors or package making uncertainties. Table 1 presents standard tolerances usually observed. In this study, a variation of 50µm is imposed on bond wire lengths and a variation of 0.25 is set on the dielectric constant of the ceramic. These physical variations are calculated and converted to lumped element variations. These results are presented in Table 1 (third column) and are used to simulate packaged transistor input impedances.

TABLE I. Applied Variations to Package Lumped Elements

	Standard tolerance	*Applied variations to lumped elements*
εr : dielectric constant of alumina ceramic	± 0.25	C1=(1.99 ± 0.05)pF
Length of gate bond wire	± 50µm	Lg=(1.15 ± 0.034)nH
Length of drain bond wire	± 50µm	Ld=(0.72 ± 0.034)nH
Lengths of source bond wires	± 50µm	Ls=(0.09 ± 0.01)nH

These variations can lead to very large dispersions of the input impedance which can reach 15% of the initial value.

The Fig. 4 presents results of simulated input impedances of the packaged transistor when variations (Table 1) are applied to package elements.

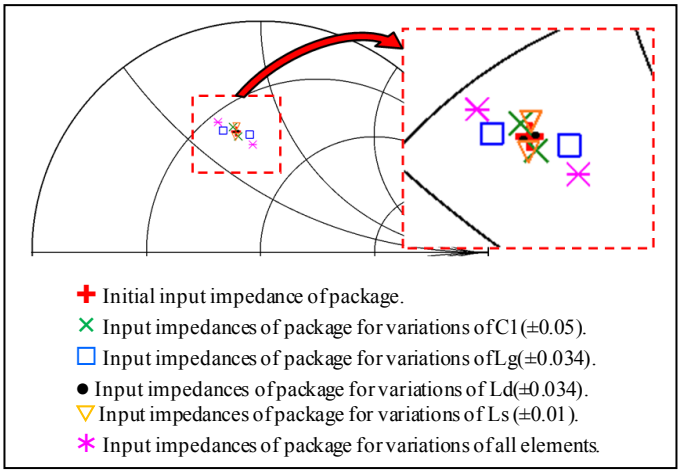

Figure 4. Simulated input impedances of the packaged transistor when variations are applied to package elements.

Applied variations to the drain and source bond wires and on the dielectric constant do not present significant impact on the packaged transistor input impedance. However, a small variation applied to the gate bond wire presents more significant impact. When variations are applied to all elements of the package, input impedances can be equal to (19+j*33)Ω and (31+j*36)Ω. The initial value of the packaged transistor input impedance is equal to (24+j*35)Ω.

To overcome intrinsic package variations, the previously modeling methodology allows us to obtain lumped elements that exactly correspond to physical elements of the package.

IV. Impact of Load Impedance Variations on the Packaged Transistor Input Impedance

This chapter presents consequences of a small variation of load impedances on the input impedance. Intrinsic package elements are frozen so that the variation is extrinsic to the packaged transistor. This variation may be characterized by a mismatch between simulated and measured output matching network.

First, load pull is performed on packaged transistor and input impedances are measured. The load variation does not exceed 15% of the reference load impedance. The same measurements are performed on the unpackaged die for a maximum load variation equivalent to 35% of the reference load impedance. For this study, the reference load impedance corresponds to a trade-off between high efficiency and output power. For each case, results are shown for the same input power at 2dB gain compression. Fig. 5 illustrates results at 3.6GHz.

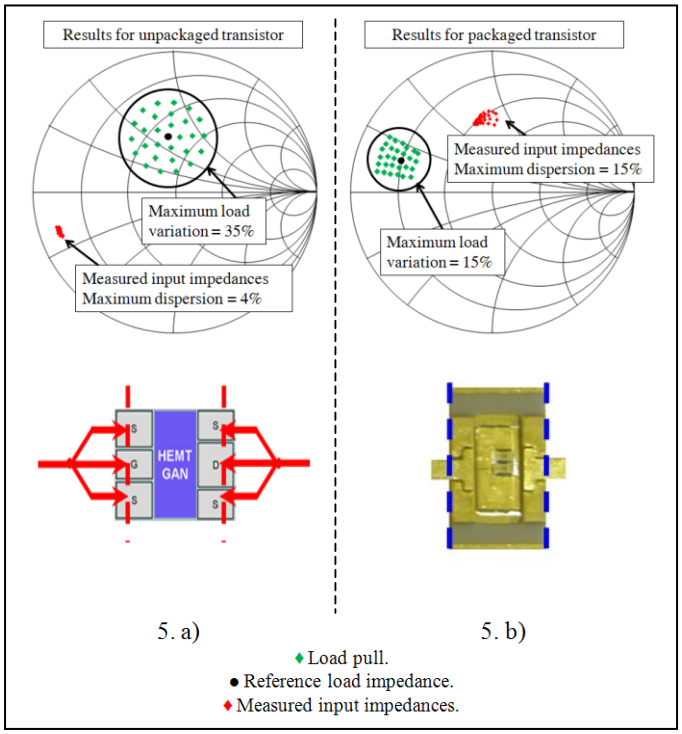

Figure 5. Impact of load impedance variations on input impedance for an unpackaged transistor 5.a) and for a packaged transistor 5.b).

Measurement results reveal a dispersion of around 15% of input impedances for the packaged transistor. This phenomenon is due to the low impedance characteristic of the metal ceramic. For a packaged power bar, this dispersion is even more important and generates significant drawbacks for high efficiency applications and broadband applications. For the unpackaged die, the input impedance dispersion is lower than 4%.

For a better illustration of these dispersions, input return loss contours are simulated and measured for five load impedances which variation does not exceed 5%. It reveals a great dispersion of these contours on the Smith Chart as shown on Fig. 6.

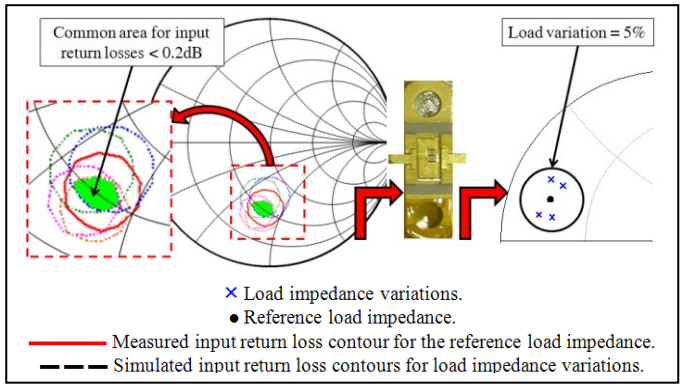

Figure 6. Impact of load impedance variations on input return loss contours.

A common area of input return loss contours lower than 0.2dB can be defined. An input matching network has to synthesize an impedance in this common area to overcome impedance load variations.

V. Input Matching Capability over a Wide Bandwidth

To improve the input pre-matching of the packaged transistor and to enhance the previous common area of return loss contours, a specific pre-matching using two chip capacitors and three bond wires are implemented in the package as shown on Fig. 7.

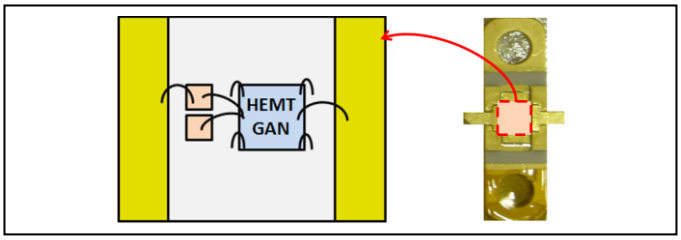

Figure 7. Packaged transistor using a specific input pre-matching.

This new packaged transistor is measured for the same five load impedances used in part IV. Also, five return loss contours lower than 0.2dB are measured and compared with the previous packaged transistor. The comparison is presented on Fig. 8.

Compared to the previous package transistor, this new device presents an input impedance close to 50Ω. Moreover,

input return loss contours and their common area are wider. Also, an input matching network is easier to synthesize and this packaged transistor is less sensitive to impedance load variations.

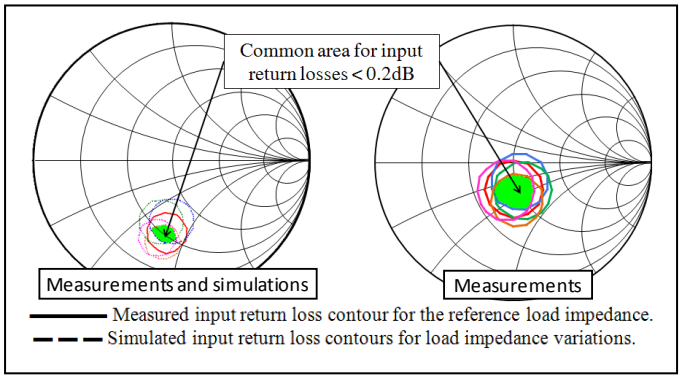

Figure 8. Comparison of input return loss contours between both input pre-matching configurations.

Input pre-matching of this packaged transistor is studied on wide bandwidth. For each frequency, the packaged transistor is loaded on its optimal impedance. Results are shown on Fig. 9 for a 29dBm available input power.

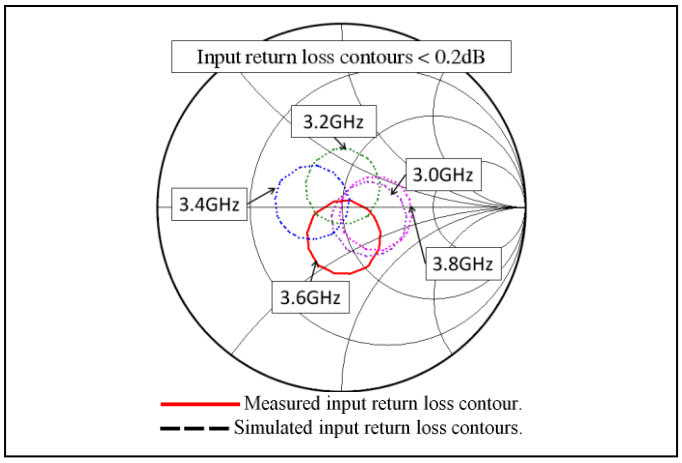

Figure 9. Input matching capability over [3.0-3.8]GHz.

This specific input pre-matching presents a very good potential over a wide bandwidth. For input return losses lower than 0.2dB, it is accepted that input impedance of this packaged transistor is matched on 50Ω over 800MHz bandwidth.

VI. CONCLUSION

This paper reveals the very good reliability of this package modeling using lumped components. When the transistor is packaged, it is demonstrated that input impedance is very sensitive to intrinsic and extrinsic package disruption. Small variations of the package components can generate damageable input impedance dispersions. The applied package modeling methodology overcomes these problems. Indeed, this extraction methodology allows us to know lumped elements that exactly correspond to physical elements of the package. It is also demonstrated that a specific input pre-matching limits input impedance dispersions when load impedance variations are applied. Moreover this packaged transistor presents an input impedance close to 50Ω on wide bandwidth [3.0-3.8]GHz.

ACKNOWLEDGMENT

The authors would like to acknowledge the French Defense Agency (DGA) for their financial support.

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