

Harmonic Control In Package of Power GaN Transistors for High Efficiency and Wideband Performances in S-Band

J.Chéron, M.Campovecchio, D.Barataud, T.Reveyrand
XLIM – UMR 6172, Université de Limoges/CNRS,
Limoges, France.
jerome.cheron@xlim.fr

M.Stanislawiak, P.Eudeline
THALES AIR SYSTEM,
Boos, France.

D.Floriot
UMS,
Orsay, France.

W.Demenitroux
AMCAD Engineering,
Limoges, France.

Abstract—This paper presents a method for synthesizing the package of power GaN transistors in order to achieve wideband matching at harmonics. The proposed method is applied to optimize the package of a 15W power GaN HEMT for high efficiency performance over 39% bandwidth (S-band). It is demonstrated that the internal pre-matching of package ensures that the impedance seen by the GaN die at the second-harmonic frequency remains confined inside a high-efficiency region over a wide bandwidth whatever loads presented to the output of the package. In fact, when the 2nd-harmonic frequency termination of the package is varied all over the entire Smith Chart, the packaged transistor demonstrates a limited variation of PAE ($70\pm3\%$) at 3.2GHz. Thereby, this method allows the designer to synthesize the external output matching of the packaged transistor only at the fundamental frequencies without imposing constraints on the 2nd harmonic loads.

Keywords—component; GaN HEMT; high-efficiency; pre-matching; harmonic load; packaged transistor.

I. INTRODUCTION

Modern radar applications are more and more confronted with the trade-off between high power-added efficiency (PAE) and wide-band operation of power amplifiers. High-efficiency classes [1-2] are defined by specific shapes of voltage and current waveforms across the transistor which are synthesized by controlling harmonic load impedances. Class-F and inverse class-F [3-4] are probably the most efficient techniques at microwave frequencies demonstrating very high PAE performances [5] for GaN transistors.

Many papers present hybrid GaN power amplifiers whose design is based on the specific control of load impedances presented outside of the package at harmonic frequencies. The main difficulty of such a design remains the control of harmonic loads over a wide bandwidth. Moreover, the designer is usually confronted to the problem that optimizing harmonic impedances presented to the package does not lead to the

expected enhancement of PAE because the transistor die does not see this variation which is hidden by the package.

This paper proposes a synthesis method of power package for GaN transistors in S-band in order to achieve an optimum control of harmonic load impedances over a wide bandwidth. The synthesis method starts from the extraction of an equivalent circuit model of the package. By using this parametric model, the synthesis method demonstrates that the two main effects of package configuration (i.e. capacitive & inductive effects) can be well dimensioned so that the impedances seen by the transistor-die at harmonic frequencies are confined into their optimum PAE region whatever the impedances presented to the package. Section II reports on-wafer load-pull measurements of a GaN HEMT die from UMS in order to define its optimal impedances at the fundamental and 2nd-harmonic frequencies. Equivalent circuit modeling of the package and its optimization for wideband 2nd-harmonic control are described in sections III and IV respectively. Then, in order to illustrate the synthesis method, two different package configurations (optimized & non-optimized) are compared using multi-harmonic load pull measurements at package reference planes. The comparison between non-optimized and optimized packages demonstrates that the maximum PAE is improved by 17 points. Finally, the last section highlights the great potential of the optimized packaged transistor over 1.3GHz bandwidth in S-band.

II. ON-WAFER LOAD-PULL MEASUREMENTS OF GAN HEMT

This section reports on-wafer pulsed RF load-pull measurements in S-band performed on a 2.4mm (6x400 μ m) GaN HEMT die from UMS foundry. The input RF signal is pulsed using 10 μ s pulse width and 10% duty cycle while biasing voltages are continuous. Gate bias voltage is close to pinch off and drain bias voltage is set to 50V. The output loads at 1st and 2nd harmonic frequencies are consecutively optimized to achieve maximum PAE.

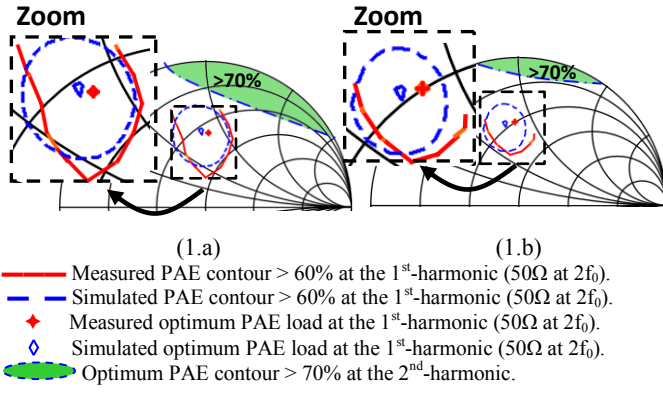


Figure 1. Measured and simulated optimum PAE contours of the GaN die at 1st and 2nd-harmonics at f_{min} (1.a) and f_{max} (1.b).

At 2.5dB compression gain, Fig. 1a and 1b show the comparison between on-wafer load-pull measurements and simulations of the GaN die at f_{min} and f_{max} , which are the frequency limits of the bandwidth. Simulated and measured results of optimum PAE contours at the 1st and 2nd-harmonic are in good agreement and allow the identification of high PAE regions at the 1st and 2nd-harmonic frequencies (Fig.1). The best PAE contours at 1st and 2nd harmonic are of prime importance to optimize the design of the package.

III. ELECTRICAL PACKAGE MODELING AND VALIDATION

A photograph of the ceramic-metal package of the GaN die and its equivalent circuit-model [6] are shown on Fig. 2. The packaged transistor model associates the non linear electro-thermal model of the GaN die with the package elements. The multiple wires connecting transistor pads (gate and drain) to package planes are modeled by the equivalent inductances (L_g and L_d) while L_s represents the wires connecting the source pads to ground. Mutual inductances ($M1$) are accounted for the coupling between gate and drain wires [7]. Package bonding areas and leads are modeled as transmission lines where $C1$ capacitance is due to the metal-ceramic area ($R1$ and $L1$ are quite negligible). The input/output coupling is modeled by a capacitance ($C2$). Such an electrical modeling is advantageous as it allows the main electrical parameters (L_g , L_d , $C1$) to be associated with the dimensions of bond wires and metal-ceramic pads.

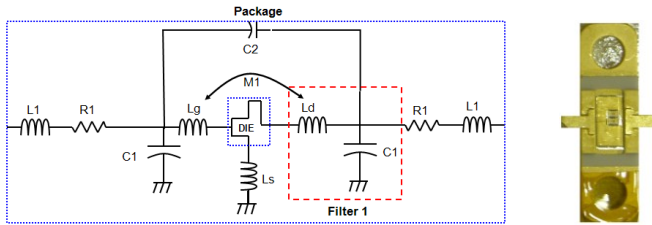


Figure 2. Equivalent circuit model of the metal-ceramic package.

Measured S-parameters over the 1-7GHz range, and large-signal CW pulsed measurements at 3.2GHz were used to verify the reliability of the packaged transistor model.

In order to illustrate the synthesis method explained in the next section, two different package configurations (optimized and non-optimized) were realized and compared. For the sake of simplicity, several load-pull results are grouped in Table II at the end of the paper. As shown in Table II, a good agreement is obtained between measured and simulated constant PAE contours at package reference planes.

IV. PACKAGE OPTIMIZATION METHODOLOGY

Starting from the initial package configuration (non-optimized) consisting of bond wires as short as possible for connecting drain pads to the metal-ceramic access, it appears that the packaged transistor is always in the worst case of 2nd harmonic termination whatever the impedances presented to the package (Table I). Therefore, the proposed synthesis method is dedicated to ensure that impedances seen by the GaN die at 2nd-harmonic are confined into their optimal PAE region whatever the impedances presented to the package.

In order to simplify the explanation of the synthesis method, the main effects of the metal-ceramic package between transistor drain pads and bonding areas may be modeled as shown on Fig.3 by the shunt capacitance $C1$ and the series inductance L_d . The values of $C1$ and L_d can be directly linked to the physical dimensions of the metal ceramic access and of the bond wires. Therefore, the synthesis can be explained in two simplified steps even if the optimization process makes use of all package parasitics.

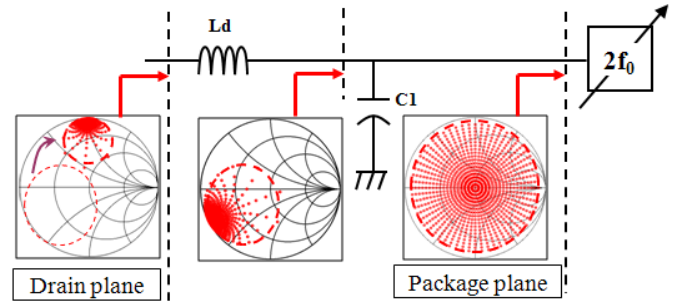


Figure 3. Simulation process to optimize the impedance transformation from the package access to the drain plane at $2f_0$. (Filter 1)

As a first step, a low value of metal-ceramic impedance Z_c makes the entire Smith Chart (package plane) to be transformed into a small region ($C1$ plane) of impedance values at $2f_0$ as shown in figure 3. Therefore, the value of $C1$ is initialized low enough to achieve the required reduction of the impedance variation seen at the 2nd-harmonic frequency. However, the value of $C1$ is not chosen too low so that to enable the external output matching at the 1st-harmonic

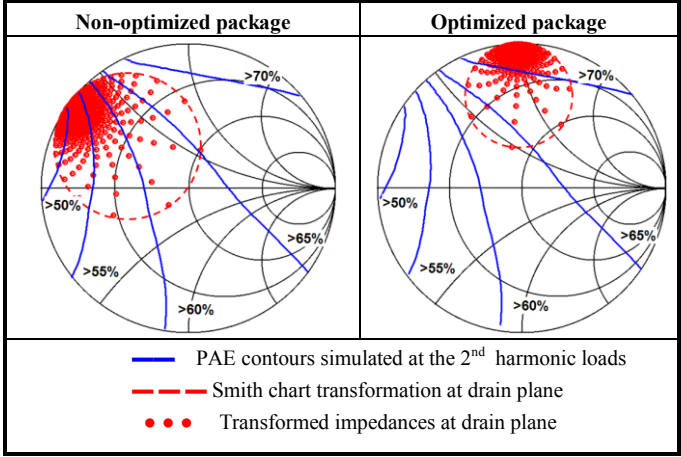
As a second step, the value of L_d is initialized so that the previously confined impedance region at $2f_0$ ($C1$ plane on Fig.3) is rotated clockwise towards the optimum PAE region of the transistor-die at $2f_0$ (Drain plane on Fig.1).

The preceding steps were used to initialize $C1$ and L_d for an optimized package of the considered GaN die in S-band. The equivalent shunt capacitance $C1$ was initialized to 2pF and the equivalent inductance L_d was initialized to 1.5nH. Note

that the equivalent values of C1 and Ld for the non-optimized package were equal to 2pF and 0.68nH respectively.

To illustrate the dramatic impact of 2nd-harmonic termination on PAE performances, the two package configurations were simulated at 3.2GHz. Table I compares the impedance locations obtained at drain plane when the package termination is varied over the entire Smith Chart 2nd-harmonic frequencies.

TABLE I
SIMULATED TRANSFORMATION OF THE ENTIRE SMITH CHART FROM PACKAGE PLANE TO DRAIN PLANE AT $2F_0$



As shown in Table I for the non-optimized package, the Smith Chart is well restricted by C1 but not enough rotated by Ld due to its low value (0.68nH). Therefore, the impedance area at the 2nd-harmonic lies in a low efficiency region whatever the impedances presented to the package at the 1st and the 2nd harmonic frequencies. Inversely, in the case of the optimized package, the same value of C1 but a higher value of Ld (1.5nH) show that the transformed impedance location at

drain plane lies in a high efficiency region (70%) at the 2nd harmonic frequency.

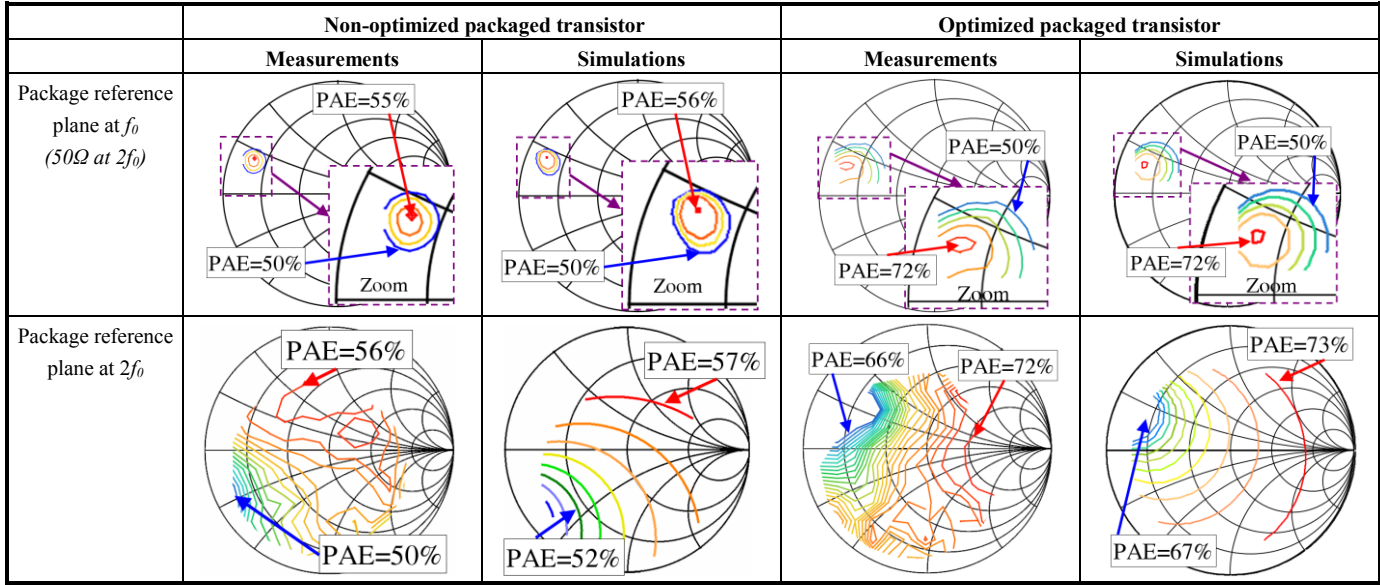
In order to better illustrate the synthesis method, two different package configurations were realized using the simplest configuration without internal pre-matching circuit. The initial S-band power package (non-optimized) of the 2.4mm GaN HEMT die is a metal-ceramic package using a 0.51mm thick alumina ceramic. Given the width of the metal-ceramic access (6.6mm) and the dielectric constant (9.6), the capacitance C1 is equivalent to a characteristic impedance of 8.3Ω. Note that C1 capacitance can be optimized by varying the width of the metalized ceramic access. Therefore, by using gold wires of 17 μm diameter, the equivalent inductances Ld is 0.68nH for the non-optimized package and 1.5nH for the optimized package.

V. PERFORMANCE COMPARISON BETWEEN TWO DIFFERENT PACKAGES OF GAN TRANSISTORS

A specific test fixture was built for load-pull measurements of packaged transistors using a TRL calibration. Measurement conditions were the same as described in part II. At 2nd harmonic, output reflection coefficients were limited to a maximum magnitude of 0.8 due to losses.

At first, the optimal PAE impedance at the 1st-harmonic was determined by load-pull technique at the package plane with 50Ω at 2nd and 3rd harmonics. Then, load pull measurements were performed at the 2nd-harmonic in order to evaluate PAE contours. Table II presents these different results at 3.2GHz and 2.5dB gain compression. The non-optimized package achieves a maximum PAE of 55% when the fundamental load is optimized. When the 2nd-harmonic termination is tuned, no PAE improvement is possible and PAE varies between 50% and 56%. These results are due to inappropriate locations of 2nd-harmonic loads at the drain plane.

TABLE II
IMPACT OF SECOND HARMONIC CONTROL FOR 2 DIFFERENT PACKAGES OF THE SAME GAN TRANSISTOR AT 3.2GHz



Following the same approach, the optimized packaged transistor achieves a maximum PAE of 72% associated with 42.6dBm output power and 13.3dB gain. Moreover, load pull measurements at the 2nd-harmonic demonstrate a PAE variation limited to only 6 points. Such a result is due to the fact that 2nd-harmonic impedances at the drain plane are confined in a high PAE region whatever the impedances presented to the package. Therefore, only by optimizing the wire length, PAE is improved by 17 points. Note that a very good agreement is achieved between simulations and measurements.

VI. PERFORMANCE EVALUATIONS OF OPTIMIZED PACKAGED TRANSISTORS ON WIDE BANDWIDTH

As outlined in the preceding sections, the good accuracy obtained for the non linear electro thermal model of the GaN-die and for the package model allows a reliable study over a wide bandwidth. Table III presents simulated performances of the optimized packaged transistor and the on wafer transistor from 2.7GHz to 4GHz.

TABLE III
PERFORMANCES OF OPTIMIZED PACKAGED TRANSISTOR OVER 1.3GHz
BANDWIDTH AND COMPARISON BETWEEN ON WAFER TRANSISTOR

Frequency [GHz]	2.7	2.9	3.2	3.5	3.8	4
Optimized Packaged Transistor						
Max PAE[%] (Zh2=50Ω)	72	71	72	71	68	65
PAE variation at H2 (Γ=0.8)	62-74	64-73	67-73	68-72	66-69	64-66
Output Power [dBm]	42.6	42.6	42.6	41.8	41.2	41.5
Gain [dB]	13.2	13.2	13.3	12.4	11.5	11.3
On Wafer Transistor						
Max PAE[%] (Zh2=50Ω)	67	65	64	63	62	60
PAE variation at H2 (Γ=0.8)	57-72	56-71	56-71	53-71	53-70	53-68
Comparison between Optimized Packaged Transistor and On Wafer Transistor						
PAE improvement (Zh2=50Ω)	+5	+6	+8	+8	+6	+5

 Measurements  Simulations

At present time, the measurement results of the GaN die are available all over the bandwidth and at 3.2GHz for the optimized package. It can be observed on Table III that unlike the GaN die, the PAE of the packaged transistor remains high

over a wide bandwidth [3.2-4GHz] with a limited variation when sweeping the 2nd-harmonic load. From 3.2GHz to 4GHz, the PAE variation of the packaged transistor is lower than 6 points with a minimum of 2 points at 4GHz, while the PAE variation of the GaN die is about 15 points all over the bandwidth. This is due to the fact that the optimized package always presents the optimum termination at the 2nd-harmonic. Thereby, the PAE variation of the optimized packaged transistor is very limited when sweeping the 2nd-harmonic load.

In addition, from 2.7GHz to 4GHz, the PAE of the optimized package is 5 to 8 points higher than that of the GaN die when their load impedances are optimized at the 1st-harmonic and are fixed to 50ohms at the higher harmonics.

VII. CONCLUSION

In the proposed method for synthesizing power packages of GaN HEMTs, load impedances seen by the transistor-die at the 2nd-harmonic are confined into their optimal PAE region whatever the impedances presented to the package. Therefore, the packaged transistor is desensitized to impedance variations at the 2nd-harmonic. It has been demonstrated that such an optimum packaged transistor is capable of meeting high efficiency conditions (65-72% PAE) over a wide bandwidth (1.3GHz) in S band. Thereby, this method allows the designer to synthesize the external matching of the package without controlling the 2nd-harmonic termination.

ACKNOWLEDGMENT

The authors would like to acknowledge the French Defense Agency (DGA) for their financial support.

REFERENCES

- [1] F. Raab, P. Asbeck, S. Cripps, P. Kenington, Z. Popovic, S.J. Potheary, N. Sokal. "Power amplifiers and transmitters for RF and microwave," IEEE Trans. on MTT, vol. 50, no 3, pp. 814-826, March 2002.
- [2] S. C. Cripps, "RF Power Amplifiers for Wireless Communications", 2nd Edition, Artech House Publishers, 2006.
- [3] Y. Y. Woo, Y. Yang, and B. Kim. "Analysis and experiments for high-efficiency class-F and inverse class-F power amplifiers," IEEE Trans. Microwave Theory & Tech., vol. 54, no. 5, pp. 1969-1974, May 2006.
- [4] F. H. Raab. "Maximum efficiency and output of class-F power amplifiers," IEEE Trans. on MTT, vol. 49, no. 6, pp. 1162-1166, May 2001.
- [5] D. Schmelzer, and S. I. Long "A GaN HEMT Class F Amplifier at 2 GHz with >80% PAE," Compound Semiconductor Integrated Circuit Symposium, pp. 96-99, Nov. 2006.
- [6] Liang, J. A. Pl'a, P. H. Aaen, and M. Mahalingam, "Equivalent-circuit modeling and verification of metal-ceramic packages for RF and microwave power transistors," IEEE Trans. on MTT, vol. 47, no. 6, pp. 709-712, Jun. 1999.
- [7] K. Mouthaan, and all, "Microwave modelling and measurement of the self- and mutual inductance of coupled bond," in Proc. Bipolar/BiCMOS Circuits Meeting, 1997, pp. 166-169.